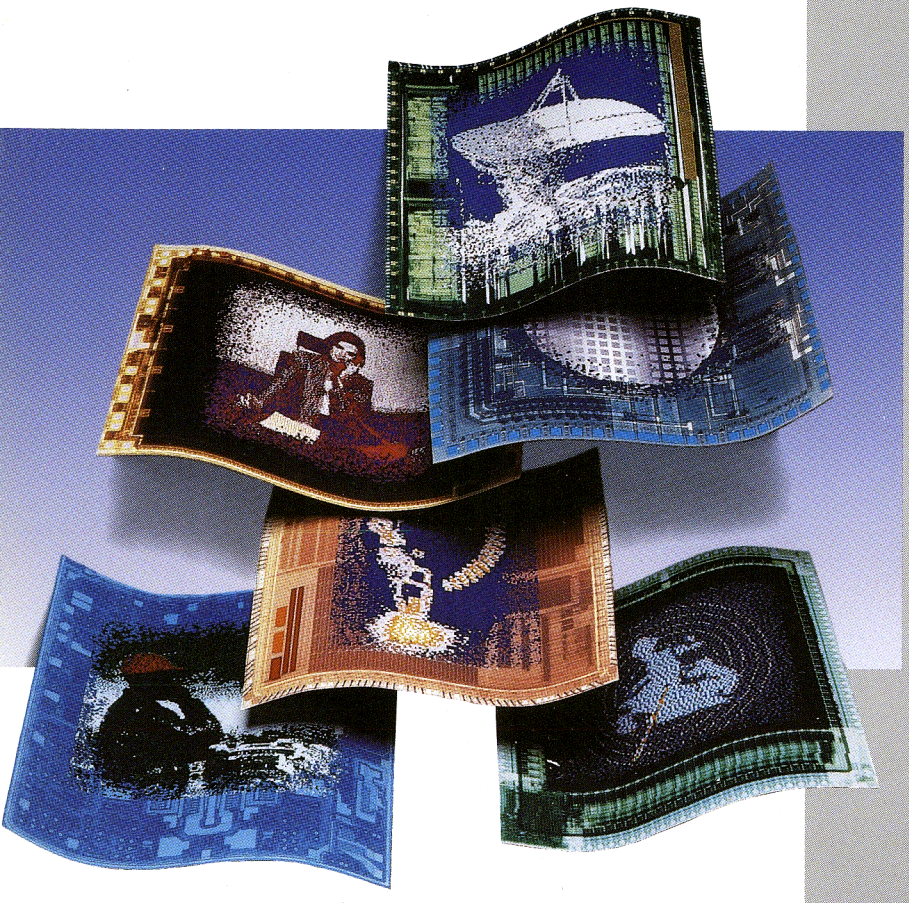
Databus Products

Handbook

January 1992



GEC PLESSEY

SEMICONDUCTORS

DATABUS PRODUCTS

Handbook

MIL-STD-1553
MIL-STD-1397
Fibre Optics

GEC PLESSEY
SEMICONDUCTORS

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Foreword

This handbook brings together for the first time in one document, data on the MIL-STD-1553 and associated bus standard components, manufactured by the former MEDL Hybrid and IC groups, along with those from the former MCTC (CTI) organisation.

For over 12 years the organisation has been a world leader in data bus products, pioneering one of the first LSI Silicon implementations of the protocol function, and introducing the first Transceivers to the market as standard products.

In addition the databook contains information on a unique range of MIL-STD-1397 (STANAG 4153) Products, including fibre optic implementations.

Our current range contains products to fulfil a whole range of different applications. If your needs are not met by our products, let us know!

Please Note:

1. Certain earlier products which are still available are not listed for space reasons.
2. Radiation Hard SOS MIL-STD-1553 products from GPS are listed in sister publication SOS Radiation Hard Handbook (S00000FDB Issue 1).

Please consult your nearest Service Centre or representative for information on either of the above.

Product List - Complete Terminals

Type No.	Description	Package	Voltage	Page
CT2525	R.T/B.C. MIL-STD-1553B Dual Transceiver	90 Pin Plug-In* 2.4" x 1.6"	+5V, ±15V	1-3
CT2526	R.T/B.C. MIL-STD-1553B Dual Transceiver	90 Pin Plug-In* 2.4" x 1.6"	+5V, ±12V	1-3
CT2527	R.T/B.C. MIL-STD-1553B Dual Transceiver	90 Pin Plug-In* 2.4" x 1.6"	+5V	1-3
CT2528	R.T/B.C. MIL-STD-1553B	90 Pin Plug-In*	+5V	1-3
CT2529	R.T/B.C. MIL-STD-1553B Small outline package.	100 Pin Quad Flat Pack 1.54" x 1.32"	+5V	1-3
CT2553	R.T./B.C. MIL-STD-1553B Pin compatible to BUS61553.	78 Pin Quad Plug-In 2.1" x 1.87"	+5V, -15V	1-35
CT2554	R.T./B.C. MIL-STD-1553B Pin compatible to BUS61554.	78 Pin Quad Plug-In 2.1" x 1.87"	+5V, -12V	1-35
CT2555	R.T./B.C. MIL-STD-1553B Pin compatible to BUS61555.	78 Pin Quad Plug-In 2.1" x 1.87"	+5V	1-35
MCT83102/3/5	R.T.U. with sub system interface and dual port double buffered RAM.	90 Pin Plug-In* 2.4" x 1.6"	+5V, ±15V† ±12V†	1-47
MCT83910	R.T.U. with interface, 4K RAM, +5V/±15V transceiver. Similar to MCT83100 Series but for use in STANAG 3910 applications, along with HS data link chip.	90 Pin Plug-In* 2.4" x 1.6"	+5V, ±15V†	1-47
MCT83911	As MCT83910 but with +5V/±12V supply option.	90 Pin Plug-In* 2.4" x 1.6"	+5V, ±12V†	1-47
MCT83912	As MCT83911 but with single +5V supply option.	90 Pin Plug-In* 2.4" x 1.6"	+5V	1-47

* Available in Flat Pack for Surface Mounting.
† Options deleting +15V(+12V) rail requirement to be introduced shortly.

Product List - Transceivers

Type No.	Description	Package	Voltage	Page
CT1487M	MIL-STD-1553A/B Single Transceiver.	24 Pin Plug-In* 1.4" x 0.81"	+5V, ±15V	2-3
CT1487MI	As CT1487M but with inverted receiver data outputs.	24 Pin Plug-In* 1.4" x 0.81"	+5V, ±15V	2-3
CT1487MP	MIL-STD-1553A/B Single Transceiver.	24 Pin Plug-In 1.28" x 0.78"	+5V, ±15V	2-3
CT1487D	MIL-STD-1553A/B Dual Transceiver.	36 Pin Plug-In* 1.91" x 0.79"	+5V, ±15V	2-3
CT1487DI	As CT1487D but with inverted receiver data outputs.	36 Pin Plug-In* 1.91" x 0.79"	+5V, ±15V	2-3
CT1589M	±12V version of CT1487M.	24 Pin Plug-In* 1.4" x 0.81"	+5V, ±12V	2-3
CT1589MI	As CT1589M but with inverted receiver data outputs.	24 Pin Plug-In* 1.4" x 0.81"	+5V, ±12V	2-3
CT1589MP	±12V version of CT1487MP.	24 Pin Plug-In 1.28" x 0.78"	+5V, ±12V	2-3
CT1589D	±12V version of CT1487D.	36 Pin Plug-In* 1.91" x 0.79"	+5V, ±12V	2-3
CT1589DI	As CT1589D but with inverted receiver data outputs.	36 Pin Plug-In* 1.91" x 0.79"	+5V, ±12V	2-3
CT2520	MIL-STD-1553A/B Dual Transceiver	36 Pin Plug-In* 1.91" x 0.79"	+5V	2-11
CT2521	MIL-STD-1553A/B Dual Transceiver	36 Pin Plug-In* 1.91" x 0.79"	+5V	2-11
CT2522	MIL-STD-1553A/B Single Transceiver	24 Pin Plug-In* 1.4" x 0.81"	+5V	2-11
CT2523	MIL-STD-1553A/B Single Transceiver	44 Pin Quad Plug-In 0.65" x 0.65"	+5V	2-11

* Available in Flat Pack for Surface Mounting.

Product List - Transceivers (continued)

Type No.	Description	Package	Voltage	Page
CT3231M	MIL-STD-1553A/B Single Transceiver	24 Pin Plug-In* 1.27" x 1.27"	+5V, ±15V ±12V	2-19
CT3232M	MIL-STD-1553A/B and MAC Air Single Transceiver	24 Pin Plug-In* 1.27" x 1.27"	+5V,±15V ±12V	2-25
MMT30000	Compact MIL-STD-1553A/B Tx/Rx	18 Pin Plug-In 0.98" x 0.78"	+5V, ±15V	-
CT1816	H009 Bus Transceiver	24 Pin Plug-In 1.25" x 1.25"	+5V, ±12V - ±15V	-

* Available in Flat Pack for Surface Mounting.

Product List - Transceiver/Protocol

Type No.	Description	Package	Voltage	Page
CT2512	R.T. MIL-STD-1553B Dual Transceiver. Pin configurable to BUS65112/142.	78 Pin Plug-In* 2.1" x 1.87"	+5V, ±15V	3-3
CT2513	R.T. MIL-STD-1553B Dual Transceiver. Pin configurable to BUS64113.	78 Pin Plug-In* 2.1" x 1.87"	+5V, ±12V	3-3
CT1775	MIL-STD-1553A/B Transceiver/Encoder. S/P, P/S Connection. Pin configurable to BUS65101 & 65102	76 Pin Plug-In 1.86" x 1.60"	+5V, +12V - +15V, -12V - -15V	-

* Available in Flat Pack for Surface Mounting.

Product List - Protocol

Type No.	Description	Package	Voltage	Page
CT1602	MIL-STD-1553B B.C./R.T./P.M.	90 Pin Plug-In* 2.4" x 1.6"	+5V	4-3
CT1610	MIL-STD-1553B B.C./R.T./P.M.	90 Pin Plug-In* 2.4" x 1.6"	+5V	4-3
CT1612	MIL-STD-1553B B.C./R.T./P.M.	90 Pin Plug-In* 2.4" x 1.6"	+5V	4-29
CT1990	MIL-STD-1553B B.C./R.T./P.M.	90 Pin Plug-In* 2.4" x 1.6" 121 Pin Grid Array 1.32" x 1.32"	+5V	4-55
CT1991	MIL-STD-1553B B.C./R.T./P.M. With comprehensive self-test.	90 Pin Plug-In* 2.4" x 1.6" 121 Pin Grid Array 1.32" x 1.32"	+5V	-
CT2565	MIL-STD-1553B B.C./R.T./P.M.	78 Pin Plug-In* 2.1" x 1.87"	+5V	4-57
MA805	MIL-STD-1553B R.T./P.M.	40 Pin Plug-In 2.1" x 0.63" 40 Pin LCC 0.5" x 0.5"	+5V	4-87
MRTU53050	MIL-STD-1553B R.T. for full protocol handling at message level.	Plug-In 2.65" x 1.6"	+5V	See CT1602/10
MRTU53050S	Single Channel version of MRTU53050.	Plug-In 2.65" x 1.6"	+5V	See CT1602/10
MRTU53053	B.C./R.T./P.M. with Status bit control and Command illegalisation.	Plug-In 2.65" x 1.6"	+5V	See CT1612
MRTU53055	MIL-STD-1553B B.C./R.T./P.M.	Plug-In 2.65" x 1.6"	+5V	See CT1602/10
MRTU53055S	Single Channel version of MRTU53055.	Plug-In 2.65" x 1.6"	+5V	See CT1602/10
MRTU53042	MIL-STD-1553B B.C./R.T./P.M. with extended timeout option. Eg. For extra long buy lengths.	Plug-In 3.2" x 1.6"	+5V	-

* Available in Flat-Pack for Surface Mounting.

Product List - Sub-System Interfaces

Type No.	Description	Package	Voltage	Page
CT2566	MIL-STD-1553B to Microprocessor Interface Pin compatible to BUS66300.	78 Pin Plug-In* 2.1" x 1.87" Pin Grid Array 1.32" x 1.32"	+5V	5-3
CT1800	MIL-STD-1553B to Microprocessor Interface.	90 Pin Plug-In* 2.4" x 1.6"	+5V	-
CT1801	As CT1800 except does not contain 2k x 16 message RAM internally.	90 Pin Plug-In* 2.4" x 1.6"	+5V	-
CT1611	MIL-STD-1553B to Microprocessor Interface.	90 Pin Plug-In* 2.4" x 1.6"	+5V	-

* Available in Flat-Pack for Surface Mounting.

Product List - Encoder/Decoders

Type No.	Description	Package	Voltage	Page
MA15530	MIL-STD-1553A/B and MAC Air B.C./R.T. Manchester Encoder/Decoder. Pin compatible with HD15530.	24 Pin Plug-In 1.21" x 0.63"	+5V	6-3
CT1555-3	MIL-STD-1553A/B and MAC Air B.C./R.T.	56 Pin Plug-In* 2.16" x 1.16"	+5V	6-19
CT1820	MIL-STD-1553A/B and MAC Air B.C./R.T.	56 Pin Plug-In* 2.16" x 1.16"	+5V	6-19
CT1820-2	As CT1820 except has internal buffers on the data lines.	56 Pin Plug-In* 2.16" x 1.16"	+5V	6-19

* Available in Flat-Pack for Surface Mounting.

Product List - Cards

Type No.	Description	Package	Voltage	Page
CT2600	MIL-STD-1553/1773 to PC Card.			7-3
CT2605	MIL-STD-1553 to MIL-STD-1773 Fibre Optic Gateway Card.		+5V, ±12V	7-21

Product List - Mil-Std-1397

Type No.	Description	Package	Voltage	Page
CT1698	MIL-STD-1397 Type 'E' Tx/Rx. With internal transformer.	34 Pin Plug-In* 1.81" x 1.41"	±5V	8-3
CT1750	1/10MHz MIL-STD-1397 'J' or MIL-STD-1773 Transmitter - Fibre Optic.	8 Pin	+5V	8-11
CT1760	10MHz MIL-STD-1397 'J' Receiver - Fibre Optic.	12 Pin	±5V	8-15
CT1815	10MHz MIL-STD-1397 Type 'D' Low Level Serial Interface.	34 Pin Plug-In* 1.81" x 1.41"	±5V	8-19
CT2500	MIL-STD-1397 Type 'E' Protocol.	84 Pin Ceramic Pin Grid Array 1.12" x 1.12"		8-27
CT2500-1	As CT2500.	84 Pin LLCCC 1.17" x 1.17"		8-27
CT2505	10MHz MIL-STD-1397 Type 'E' Low Level Serial Interface.	30 Pin Flat-Pack 1.56" x 1.36"	+5V	-

* Available in Flat-Pack for Surface Mounting.

Product List - Mil-Std-1773 Fibre Optic

Type No.	Description	Package	Voltage	Page
CT1763	1MHz MIL-STD-1773 Receiver - Fibre Optic.	12 Pin	+5V	9-3

Section 1
Complete Terminals

3032-1.4 November 1991

CT2525-29 Series

SINGLE PACKAGE SOLUTION, DUAL TRANSCEIVER, PROTOCOL, SUBSYSTEM

The CT2525 Series provides a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The hybrid provides all data buffers and control registers to function as a Bus Controller or Remote Terminal. Control of the hybrid by the subsystem is through simple I/0 port commands. Internal hybrid logic removes all critical timing imposed on a typical subsystem, thereby simplifying the implementation of this interface.

FEATURES

- Incorporates Transceivers, Protocol, and System Interface components into a single Hybrid package
- Functions as a Remote Terminal or Bus Controller
- Interfaces to uP as a simple peripheral unit
- Available with several options for transceivers: ±15V, ±12V, and ±5V
- Provides 2k by 16 of Double Buffered RAM storage for transmit and receive subaddresses
- Pin programmable for 8-bit or 16-bit microprocessors

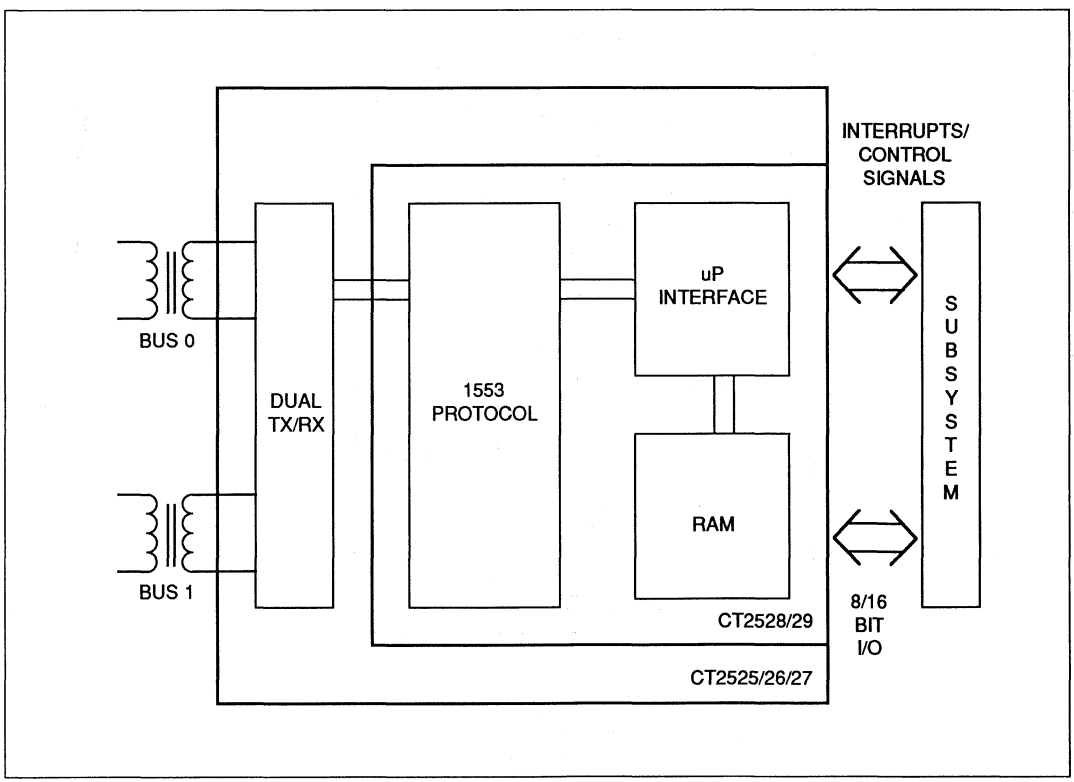


Figure 1: CT252X Block Diagram

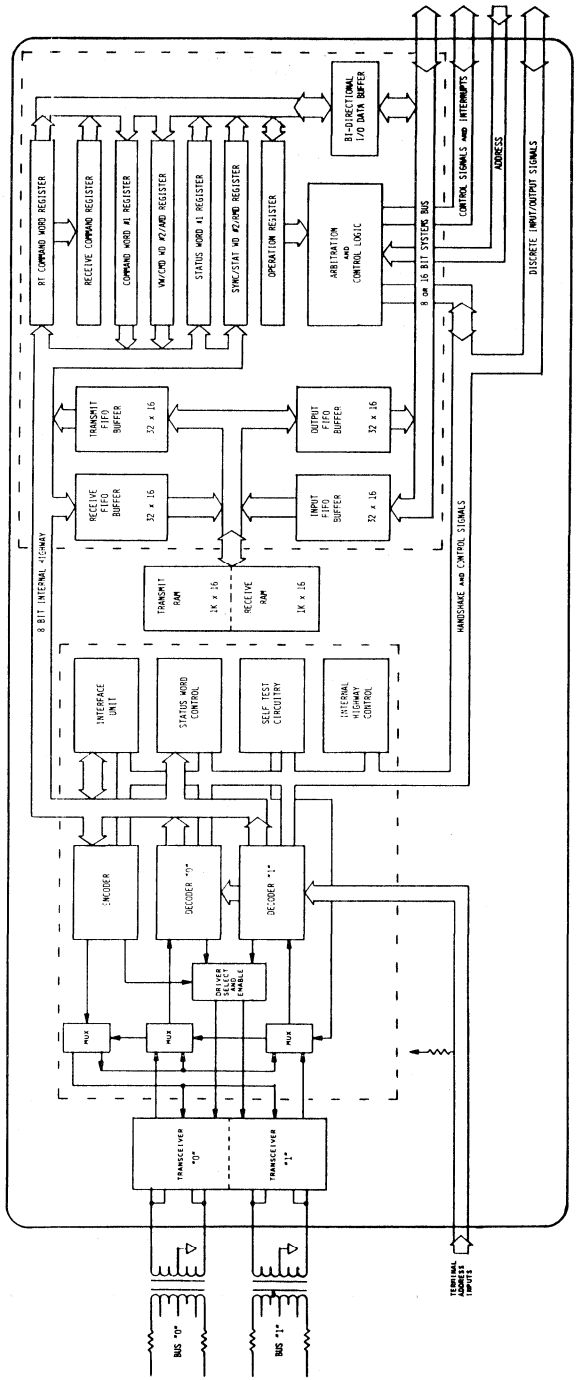


Figure 2: CT2525/26/27 Functional Diagram

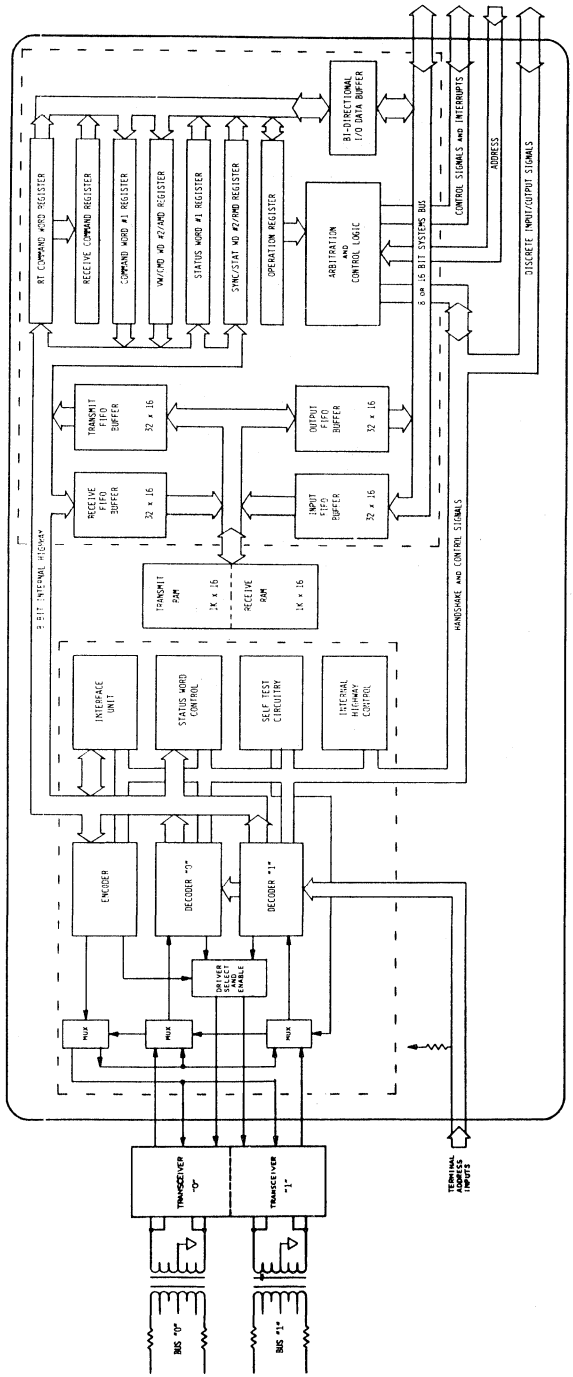


Figure 3: CT2528/29 Functional Diagram

ABSOLUTE MAXIMUM RATINGS	DEVICE	LIMITS
Power Supply Voltage (Vcc)	CT2525 CT2526 CT2527 CT2528 CT2529	-0.3V to +18V -0.3V to +18V -0.3V to +7V N/A N/A
Power Supply Voltage (Vee)	CT2525 CT2526 CT2527 CT2528 CT2529	-0.3V to +18V -0.3V to +18V N/A N/A N/A
Power Supply Voltage (VccL and VDD)	ALL	-0.3V to +7V
Receiver Differential Input (DATA CH A/B / DATA- CH A/B)	CT2528 CT2529	±20V (40V p-p) Subject to Ext Transceiver Used
Receiver Input Voltage (DATA CH A/B or DATA- CH A/B)	CT2528 CT2529	±15V Subject to Ext Transceiver Used
Transmission Duty Cycle at Tc=125°C	CT2528 CT2529	100% Subject to Ext Transceiver Used
Operating Case Temperature Range (Tc)	ALL	-55 to +125°C

Table 1: CT2525/26/27/28/29 Characterisics

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
CT2525 Power Supply Voltages	Vcc	14.25	15	14.75	V
	Vee	-14.25	-15	-15.7	V
	VccL	4.5	5	5.5	V
CT2526 Power Supply Voltages	Vcc	11.4	12	12.6	V
	Vee	-11.4	-12	-12.6	V
	VccL	4.5	5	5.5	V
CT2527 Power Supply Voltages	Vcc	4.5	5	5.5	V
Total supply current 'standby' mode or transmitting at less than 1% duty cycle (e.g. 20us of transmission every 2ms or longer interval)	CT2525/26				
	Icc		30	50	mA
	Iee	Note 1	50	70	mA
	IccL	Note 1	64	90	mA
	CT2527				
	Icc		110	140	mA
Total supply current transmitting at 1MHz into a 35 ohm load at point A in Figure 1.	CT2525				
	Icc@25%	Note 2	70	100	mA
	Icc@100%	Note 2	200	260	mA
	CT2526				
	Icc@25%	Note 2	85	120	mA
	Icc@100%	Note 2	240	315	mA
	CT2527				
	Icc@25%	Note 2	225	270	mA
	Icc@100%	Note 2	535	610	mA

Note 1: Iee and IccL limits do not change with mode of operation or duty cycle. Transceiver section only.
Note 2: Decreases linearly to applicable "standby" values at zero duty cycle.

Table 2: CT2525/26/27 Transceiver Characteristics Power Supply Data (Transceiver Section)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Differential input impedance DC to 1MHz	Zin	9K			ohms
Differential voltage range	Vdir	±20V			Vpeak
Input common mode voltage range	Vicr	±10V			Vpeak
Common mode rejection ratio (from point A, Figure 4)	CMRR	40			dB
Threshold characteristics (sine wave at 1MHz) NOTE: Threshold voltages refer to point A, Figure 4.	Vth1	0.8		1.1	V p-p
Filter Characteristics	Vth2 Vth3	1.5 5		8	V p-p V p-p

Table 3: CT2525/26/27 Transceiver Characteristics
Electrical Characteristics (Receiver Section All Devices)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Differential output level at point B, Figure 4 (145 ohm load)	CT2525/26 Vo CT2527 Vo	26 25	28 27	35 35	V p-p V p-p
Rise and Fall times (10% to 90% of p-p output)	Tr	100	160	300	ns
Output offset at point A in Figure 4 (35 ohm load) 2.5us after mid-bit crossing of parity bit of last word of a 660us message	Vos		±20	±75	mV peak
Differential output noise	Vnoi			10	mV p-p
Differential output impedance (inhibited) at 1MHz	Zoi	8K			ohms

Table 4: CT2525/26/27 Transceiver Characteristics
Electrical Characteristics (Transmitter Section All Devices except as noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic Supply	4.5	5.0	5.5	VDC	
V_{IH}	Input "1"	2.0			VDC	
V_{IL}	Input "0"			0.8	VDC	
I_{IL}	Input I	-450		-900	uA	Note 1A
I_{IH}	Input I	-600			uA	Note 1B
I_{IL}	Input I	-50		-800	uA	Note 1C
I_{IH}	Input I	-500			uA	Note 1D
I_{IL}	Input I	-25		-400	uA	Note 2A
I_{IH}	Input I	-250			uA	Note 2B
V_{OH}	Output "1"	2.4			VDC	Note 3A
V_{OL}	Output "0"			0.4	VDC	Note 3B
V_{DD}	Static I		40		mA	Note 4A
V_{DD}	Dynamic I			170	mA	Note 4B

Conditions: Operating Temperature Range (T_C) -55° to +125°C

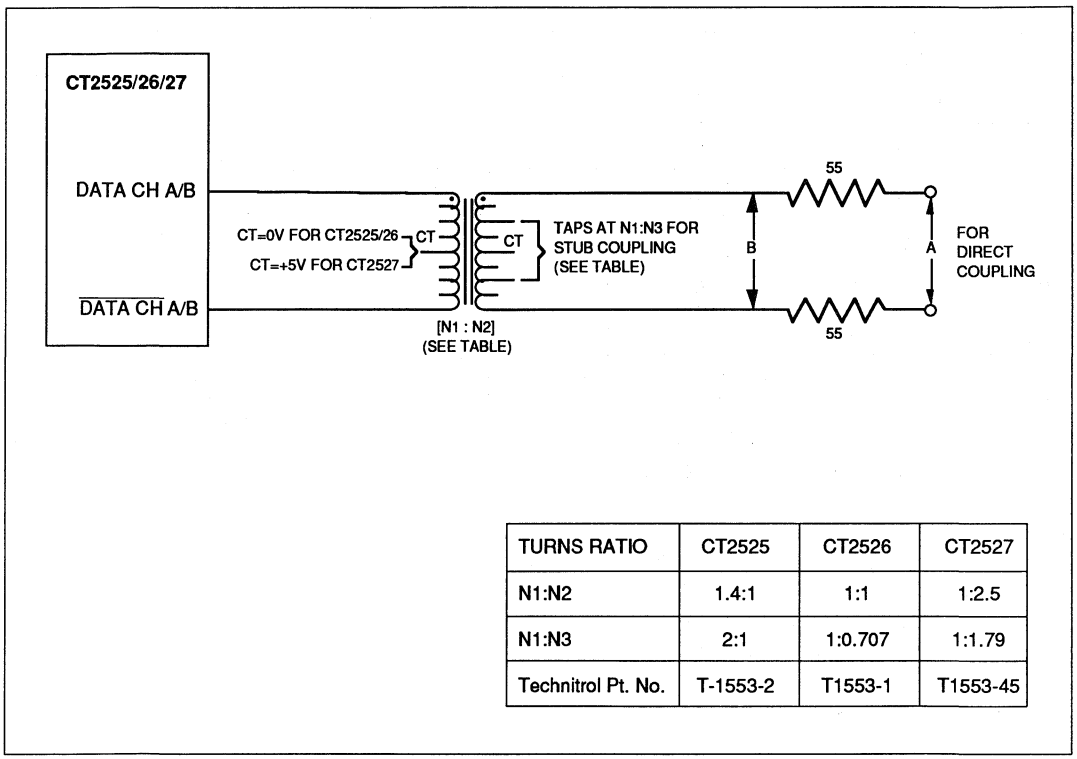
Notes: 1. V_{DD} = 5.5V
A. For RTAD0/1/2/3/4 and RTADPAR with V_{IL} = 0.4V
B. For RTAD0/1/2/3/4 and RTADPAR with V_{IH} = 2.4V
C. FOR BCSTEN WITH V_{IL} = 0.4V
D. FOR BCSTEN WITH V_{IH} = 2.4V

2. All remaining inputs and I/O
V_{DD} = 5.5V
A. V_{IL} = 0.4V
B. V_{IH} = 2.4V

3. A. V_{DD} = 4.5V and I_{OH} = 3mA
B. V_{DD} = 5.5V and I_{OL} = 3mA

4. V_{DD} = 5.5V
A. Clock Input = 6MHz (40-60% Duty Cycle / TTL Levels)
All remaining Inputs = V_{DD}
All Outputs = Open Circuit
B. During a 32 word FIFO to RAM or RAM to FIFO block Move.

Table 5: CT2525/26/27/28/29 Logic Characteristics



TURNS RATIO	CT2525	CT2526	CT2527
N1:N2	1.4:1	1:1	1:2.5
N1:N3	2:1	1:0.707	1:1.79
Technitrol Pt. No.	T-1553-2	T1553-1	T1553-45

Figure 4: Transformer Configurations

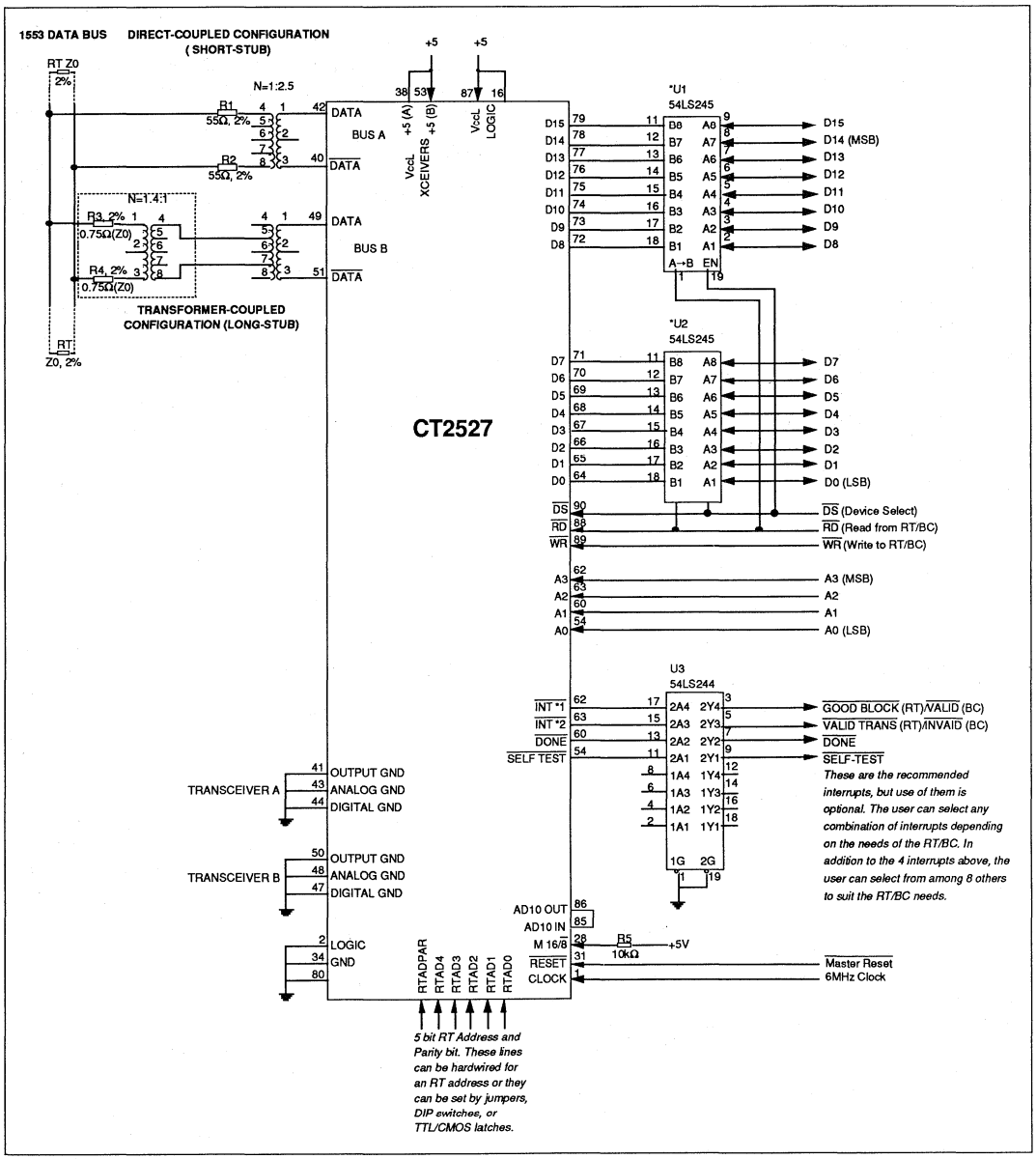


Figure 5: Typical Interface Connections

SINGLE HYBRID PROTOCOL SUBSYSTEM INTERFACE

Key Features

- Functional Superset of CT1800
- Downward compatible with existing designs base of CT1800
- Incorporates Transceivers, Protocol and Interface Hybrids into a single package
- Functions as a Remote Terminal or Bus Controller

General

The CT25XX Series provides a complete interface between the MIL-STD-1553 bus and any micro-processor system. Functioning as a superset of the CT1800 interface, the hybrid provides all data buffers and control registers necessary to implement RT and BC functions. Internal arbitration and data transfer control circuitry eliminates subsystem response requirements. All data written into or read from this interface are double buffered on a message basis. Only valid and complete receive messages are transferred into the receive RAM.

The CT25XX Series supports all 15 mode codes and all types of data transfers allowed by MIL-STD-1553B. All circuitry (excluding transceiver drivers) are CMOS, which results in very low power requirements.

Interfacing to the subsystem is simplified through the use of tri-stated input/output buffers onto the subsystem bus. Control signals basically consist of four address lines, a device select input, read strobe, write strobe, and several interrupts, the use of which are optional. The Hybrid is accessed as a memory mapped I/O port of a microprocessor system. Valid transmission and reception of data are indicated to the subsystem through the use of interrupts. This frees up the system processor from actively monitoring the port until a valid message is received.

OPERATION

The CT25XX Series (Single Package Solution) resides between a microprocessor interface and a MIL-STD-1553 data bus. The addition of two transformers and fault isolation resistors are the only external components required to complete the interface. Information on the bus is received or transmitted through the transceiver (converted from Manchester II to complimentary TTL signals and visa versa) to the protocol section. The type transceiver employed determines the actual part number. The CT2525 Series incorporates a +5VDC and ±15VDC transceiver, while the CT2526 is a +5VDC and ±12VDC type. The CT2527 is a single +5VDC only transceiver, and the CT2528 contains no transceiver allowing external single or dual transceiver use.

The protocol section internally interfaces to the transceivers. Control of the transceivers is provided by the protocol section. This is determined by which bus the command word was received on in the remote terminal mode; or in the bus controller mode, which bus was selected for transmission by the state of a bit in the operation register. The protocol section is very similar to our CT1600 series of protocol devices, with the exception that it is a single chip implementation with an extensive self-test function. An autonomous self-test can be performed either off-line or on-line through the transceivers This self-test is controlled by the operation register and will be discussed thoroughly in the self-test section. The other test function is that in addition to the protocol criteria that is tested during every transmission; i.,e., proper sync character, 16 data bits, Manchester II coded, contiguous words, and odd parity, a bit per bit comparison of the contents of the parallel data will insure a higher degree of functionality of this section of the hybrid.

Data received by the protocol section will be placed in the receive FIFO buffer. Transmitted data will be taken from the transmit FIFO buffer. Other than the remote terminal address and parity, the discretes to control the resetting of the terminal flag and subsystem error bits, and a few discrete interrupts and error signals, control over the protocol section resides in the operation register of the subsystem interface section.

The subsystem interface section has primary control of the data that resides in the 2k of RAM. The RAM is segregated into two 1 k blocks of data, one contains 30 blocks of transmit data messages and the other one contains 30 blocks of receive data messages. This is not absolute since the subsystem has control of the A10 bit. Data entries to or from the RAM are arbitrated by the control logic residing in this function, and is buffered via FIFO's on the input from the protocol section and on the output to the subsystem's data bus. This guarantees that only current and valid data blocks will reside in RAM. This is true for remote terminal and bus controller applications.

Seven dedicated registers are provided to ease the interfacing with the subsystem. These will be discussed in the Register Operation section of this document. The register of primary concern to a subsystem designer is the operation register. This provides the means to accomplish data transfers to/from the RAM, as well as control of remote terminal or bus control modes of operation. All registers are accessed via simple I/O commands, utilizing A0 through A3, $\overline{\text{Device Select}}$, and Read or Write strobes.

Receive Commands

When a valid receive command is received, it is first loaded into the Command Word Register. The data words associated with this command are received, validated, and loaded one by one into the RCV FIFO buffer. Once the entire message is received, and only if the complete block of data is valid, will the command word be transferred to the RCV Command Register. This block of data is then burst (by the internal controller) into the corresponding internal RAM location, which is memory mapped by the subaddress contained in the RCV Command Register. Once this operation is complete, a discrete interrupt pulse called INT #1 is sent the subsystem.

If this interrupt is used, the subsystem would read the command word from the RCV Command Register. The data could then be transferred to the OUTPUT FIFO buffer, and read by the subsystem. Each receive subaddress section of the internal RAM will contain only the most recent, valid, and complete block of data to that subaddress. This is true for Remote Terminal and Bus Controller operations.

Transmit Commands

If a valid transmit command is received, the command word is first loaded into the Command Word Register. The block of data corresponding to the subaddress of the transmit command is then transferred from the internal RAM to the XMIT FIFO buffer. Upon completion of this transfer, INT #2 is sent to the subsystem.

The transmit section of the internal RAM is generally initialized at power up and periodically updated as required.

Appropriate subsystem response to INT #2 for an RT implementation would be to read the command word from the Command Word Register. The data to this subaddress could now be refreshed in preparation for the next time it was requested to be transmitted across the 1553 bus.

Mode Codes

All 15 mode codes are serviced by the protocol section, and most do not require subsystem intervention. Discrete interrupt signals are available for each of the Synchronize (with and without data), Vector Word, Reset, and Dynamic Bus Control Acceptance mode codes. Mode command words are loaded into the Command Word Register. Separate registers are provided for the synchronize data word and the vector data words.

Bus Control Operation

Upon initialization of power to the CT25XX Series, all registers are reset. The operation register is reset to FF80H; this setting defaults to the remote terminal mode of operation with the Busy Bit set. To enter into the Bus Control Mode of operation, bit 8 of the operation register must be asserted low. While in this mode, the upper byte (8 bits) of the operation register controls Bus Control functionality. This includes TEST/ NORMAL operation, RT to RT commands, BUS selection and RETRY initialization of a faulty transaction.

A typical Bus Control transaction would operate as follows: All areas of internal RAM that will be used for transmission are initialized by the subsystem with the desired data. To accomplish this, the subsystem will first WRITE to the INPUT buffer the number of words to be transferred. This information is now transferred to the internal RAM under control of the OPERATION register by specifying the subaddress bits 0-4, setting the T/R bit (bit 5) and I/O bit (bit 6) high. This will be executed by issuing an EXECUTE operation I/O command. When the transfer has been completed, the DONE interrupt will pulse low, and valid data will now reside in this RAM location. Next, the subsystem will write the command word to COMMAND WORD #1 register. If it were an RT-to-RT transfer, the transmitting RT command word would be written into COMMAND WORD #2 register. The next register to be intitialized would be the OPERATION register, which controls which bus to transmit on and if retry will be an option. This information will be enacted upon when the subsystem issues a TRIGGER I/O command. The return status word from the remote terminal or status words for RT-to-RT transfers will reside in their appropriate registers upon the issuance of INT #1. If the RETRY option had been selected and a valid transfer had not occurred, the RETRY interrupt would have occurred instead of INT #1. Three retrys are the maximum number allowed. The retrys can be accomplished on the primary or secondary bus determined by proramming bits in the operation register.

A retry will be initiated if the retry bits are set in the OPERATION register. The criteria for attempting a retry is the the lack of a returned status word or returned mode data, or that 768usec has transpired since the start of the data transfer. A retry will not be executed if bits are set in the return status word(s); this is up to the subsystem to interpret the statuswword contents and to reinitiate the transfer if desired.

Discrete Interrupts

Twelve discrete interrupt output signals are available for the subsystem interface. Any or all of these may be used depending on subsystem requirements. Excluding the signal $\overline{\text{BUFF EF}}$, all interrupts are low going pulse signals. Interrupt and status signals RESET, DBCREQ, and NBGT are 500ns wide nominally, and VECTOR is typically 1.5us wide. All remaining interrupts are nominally 160ns.

The output buffer empty flag ($\overline{\text{BUFF EF}}$), which is a level, is also made available for subsystem use. When low, it indicates the output buffer is empty. See Table 6 for additional information.

REGISTER SUMMARY

Remote Terminal Command Word Register: This Register is utilized in the RT mode and is read only. It contains all valid received command words, i.e. transmit, receive, and mode command.

Receive Command Word Register: After the reception of a valid receive message, and the GOOD BLOCK interrupt has been issued, the Receive Command word will be transferred from the Remote Terminal Command Word Register to this register. The purpose of double buffering receive command words is to maximize the time a subsystem has to read this command since GOOD BLOCK comes at the end of the data transfer, and the next command word could overwrite the contents of the Remote Terminal Command Word Register. This is a READ ONLY register in RT mode.

Command Word #1 Register: This register contains the *first* command word to be transmitted during an RT to RT transfer, or the command word for a BC to RT, or RT to BC transfer. This register is a read or write register.

Vector Word/Command Word #2/ Associated Mode Data Register: This register is used to accomplish multiple functions in Bus Controller and Remote Terminal Modes. In BC Mode it will contain the *second* command word for (RT to RT) transfers, or Associated Mode Data that is required by certain mode codes; i.e., Sync (with data). When operated in the RT Mode, this register contains the Vector Word required by mode code Transmit Vector Word Command.

STATUS Word #1 Register: The utilization of this register in the BC mode is read only. It contains the returned status word for BC to RT, RT to BC mode, or the first returned status in RT to RT mode. At reset or the initiation of a bus transfer, the contents of this register will be set to all high, FFFFH.

Synchronize/Status Word #2/ Return Mode Data Register: In Bus Controller mode this register will either contain the second returned status word for RT to RT transfers or the returned mode data; i.e., BIT word or Vector word, Last Status word, or Last Command word. In BC mode this register is initialized to all highs, FFFFH . Unlike the other status word register, this does function in the RT mode, but is still read only in either mode. In RT mode it will contain the SYNC data word received in association with the Synchronize with Data Mode Code.

Operation Register: This register contains information provided by the subsystem to control the interface. This register sets up the mode of operation for the interface (BC or RT), selects the available options (BUS Select and Auto Retry), and contains information for reading or writing data to the Internal RAM. (See note below.) This register also provides software control of the DBCACC, SERVREQ, and SSERR bits of the status word. Following power-up master reset, bit 7 of this register will be set high. This bit corresponds to the busy bit of the Remote Terminal Status Word. The subsystem reads and writes to this register under I/O commands. The transfer functions defined by this register are executed by either of the two I/O EXECUTE Commands.

Note: The Internal RAM is divided into transmit or receive sections. In general, data is written to the transmit section and read from the receive section. However, either section may be read from or written to via the T/R bit in this register.

SELF TEST

The inclusion of simple wraparound selftest circuitry in the protocol section insures that a high percentage of coverage is attainable. Testing requires simple subsystem intervention. A word is first placed in the VECTOR WORD Register. Test bit 9 in the OPERATION Register is asserted low and the I/O TEST TRIGGER address is written. The LT LOCAL (Bit 10 of the Operation Register) determines if this will be an ON/OFF line test. OFF line tests are performed by the inclusion of digital multiplexers in front of the encoder, bypassing the transceiver, providing a path to the decoder. The ON line tests are accomplished when not connected to a bus network, such as a maintenance test station, since this test utilizes the transceiver to provide the loop back path instead of the internal multiplexers. In this mode test words would appear on the bus. First, the primary bus will be tested with the data that resides in the VECTOR WORD Register. It is encoded then looped back, decoded and presented to the subsystem as a normal data transfer would be accomplished. This word will be stored in the RT Command Word Register. The secondary bus is sequentially tested after the primary bus is completed, utilizing the word residing in the VECTOR WORD Register. Upon successful completion of the test, the PASS interrupt will be asserted low.

In addition to this test of the protocol section, the subsystem data handling capability is also testable via the OPERATION Register. This is accomplished by writing a message to the INPUT FIFO Buffer; this data can be placed in any location determined by the SA0 through SA4 Bits, or in either the transmit or receive section (T/R Bit). This same data can now be transferred from this RAM location to the OUTPUT FIFO Buffer and compared with the data originally written to the INPUT FIFO Buffer. Providing this type of testing provides a high degree of functional verification .

This test implementation not only verifies MIL-STD-1553 protocol compliance (proper sync character, 16 data bits, Manchester 11 coding, odd parity, and contiguous word checking), but also the inclusion of a bit by bit comparison of transmitted data has been added. The added circuitry is used to insure that the internal functional blocks, encoder, decoder, and internal control circuitry are functioning properly. The internal data path can be verified as fault free by comparing the returned data word with the supplied data. The most effective data pattern to accomplish this is HEX AA55, since each bit is toggled (8 bit internal highway) on a high/low byte basis. Total time to complete the test is 89 microseconds. TEST ENABLE (bit 9) must remain low this entire time to ensure proper operation of the self test.

USE OF A10 AND A10IN

The standard configuration of the CT25XX Series divides the INTERNAL RAM into separate RECEIVE and TRANSMIT sections. For this configuration A10 is connected to A10IN. When A10 is high, it addresses the TRANSMIT section; when low, the RECEIVE sections. A10IN is the address input to the INTERNAL RAM.

The interface may be configured with one common section for both RECEIVE and TRANSMIT data. To configure this, A10 is not connected, and A10IN is fixed at either a logic high or low. This bit can also be controlled by the subsystem to provide double buffering of the contents of common RAM section for receive and transmit data. If A10 and A10IN are not directly connected together but gated together, then no more than 100 nsec of propogation delay should be introduced.

NON-REGISTER OPERATIONAL COMMANDS

There are six operational commands that are not register read or write operations. These commands are summarized in Table 8. The two execute operations are dependent on the contents of the OPERATION register. The address codes for all the operational commands are summarized in the 8 bit and 16 bit I/O OPERATIONAL tables.

Name	Use
$\overline{\text{INT \#1}}$	
$\overline{\text{GOOD BLOCK}}$ (RT)	Indicates reception of a valid block of data. The RECEIVE COMMAND WORD is loaded in RCV CMD WD Register. This interrupt is issued after the new block of data is moved into the Internal RAM.
$\overline{\text{VALID}}$ (BC)	Indicates that the Bus Controller has initiated and observed a valid message transfer on the 1553 data bus.
$\overline{\text{INT \#2}}$	
$\overline{\text{VALID TRANS}}$ (RT)	Indicates reception of a valid TRANSMIT COMMAND WORD. The TRANSMIT COMMAND WORD is loaded in CMD WD Register. Note: This interrupt does not necessarily indicate that the transmitted data was received by the bus controller.
$\overline{\text{INVALID}}$ (BC)	Indicates that the Bus Controller has initiated a message transfer on the data bus, but the message traffic has been deemed invalid.
$\overline{\text{SYNC NO DATA}}$	Indicates recption of a valid mode command SYNCHRONIZE WITHOUT DATA.
$\overline{\text{SYNC W/DATA}}$	Indicates reception of a valid mode command SYNCHRONIZE WITH DATA. The synchronize data word is loaded into the SYNC/STAT WD #2/RMD REGISTER. This interrupt will not be issued if a word count high or low error occurs.
$\overline{\text{DONE}}$	This interrupt is issued in response to an I/0 command from the subsystem. In response to an I/0 load OUTPUT buffer command, it indicates that the complete 32 word message block (SUBADDRESS) has been loaded into the OUTPUT FIFO buffer. In response to an I/0 load internal RAM from INPUT FIFO buffer command, it indicates the full message (1 to 32 WORDS) has been loaded. TIMING a. In response to an I/0 load OUTPUT buffer: 16.5 to 33 usec.* b. In response to an I/0 load RAM from INPUT buffer: 16.5 to 33 usec for 32 WORDS*, for SHORTER LOAD OPERATIONS SUBTRACT 0.5 usec per (16 bit) word, i.e., 17 usec to 0.5 usec for single word. *NOTE: In the unusual case where a superceding transmit command on the redundant bus occurs at the returned status time for a valid 32 word receive, simultaneously with an I/0 transfer request, the DONE interrupt may be delayed for an additional 16.5 usec.

Table 6: Discrete Interrupts Summary

Name	Use
$\overline{\text{BUFFEF}}$	This flag may be used to speed up read data operation in response to an I/0 load OUTPUT FIFO buffer command. The $\overline{\text{BUFF EF}}$ flag will go high when the first word is loaded into the OUTPUT FIFO buffer. The word may be read at that time. Please see Figure 6.
$\overline{\text{MODERESET}}$	Indicates reception of a valid RESET mode command.
$\overline{\text{VECTOR}}$	Indicates that a transmit VECTOR mode command has been received. VECTOR DATA is transmitted from VW/CMD WD #2/AMD Register.
$\overline{\text{DBCREQ}}$	Indicates acceptance of DYNAMIC BUS CONTROL COMMAND REQUEST. Note: RTU will not accept valid DBC mode command unless DBCACC bit is set low in the OPERATION Register.
$\overline{\text{RETRY}}$	Indicates that an error has occurred in the data transfer and that a retry will be performed if the retry option is selected. If all retries that were selected fail, INVALID TRANSFER INTERRUPT would be asserted on the final failure.
$\overline{\text{SELF TEST}}$	Indicates that the INITIATE SELF TEST mode command is being serviced.
$\overline{\text{PASS}}$	Active low pulse output signal which indicates that a sub-system initiated self-test (on- or off-line) operation has been sucessfully completed. This interrupt will be issued approximately 90us after the self-test operation has been triggered.

Table 6: Discrete Interrupts Summary (continued)

Bit	Name	Function
0-4	SA BITS	SUBADDRESS BITS Define SUBADDRESS MESSAGE BLOCK in INTERNAL RAM. BIT SUBADDRESS BIT 0 SA0 (LSB) 1 SAI 2 SA2 3 SA3 4 SA4 (MSB) These bits correspond directly to 1553B definition in the command word. Although SUBADDRESSES 00000_B and 11111_B are illegal in 1553B, message blocks specified by them are both READABLE and WRITABLE by the SUBSYSTEM. They are not accessible from the 1553B BUS.
5	T/$\overline{\text{R}}$ BIT	TRANSMIT/RECEIVE BIT points INPUT/OUTPUT OPERATIONS to either the TRANSMIT SECTION or RECEIVE SECTION of the INTERNAL RAM.

Table 7: Operation Register

Bit	Name	Function
6	I/$\overline{O}$ BIT	INPUT/OUTPUT BIT DEFINES DIRECTION OF DATA TRANSFER 1. SET HIGH: INPUT OPERATION An EXECUTE operation will transfer the Data currently loaded in the input FIFO buffer to the specified message block (SUBADDRESS) in the internal RAM. IF EXECUTE WITH RPT OPTION COMMAND is used, previously loaded data (i.e. data for which a load operation was previously executed) will be loaded to a new message block. Between 1 and 32 data words must be loaded in the input FIFO buffer when using an EXECUTE command with this bit set. 2. SET LOW: OUTPUT OPERATION EXECUTE operation will transfer a complete block of data (32 words) to the output FIFO buffer from the specified subaddress of internal RAM.
7	BUSY BIT	RTU BUSY HIGH- BUSY LOW - NOT BUSY MASTER RESET SETS BIT HIGH
8	RT/$\overline{BC}$	Remote Terminal/Bus Controller Bit. This line, when set HIGH, causes the hybrid to function as a Remote Terminal. When set LOW, it will function as a Bus Controller. Master reset sets this bit HIGH
9	Transaction/$\overline{Test}$	Transaction/Test Mode Bit. When this bit is set high, normal transactions will be handled, eg., BC to RT, RT to BC, RT to RT. If this bit is set low and a trigger transaction is issued, the self-test will be performed for the MIL-STD-1553 protocol chip.
10	$\overline{LT\ Local}$	Loop Test Local Bit (Used in conjunction with BIT 9). This signal selects the self test path. When set LOW, the internal digital path is selected. When set HIGH, the external path, including transceivers, is selected.
11	Bus Select	Bus Select (Bus Controller Only). When set high, Bus 1 is selected. When set LOW, the opposite bus, Bus 0 is selected.
12	Normal/$\overline{RT\text{-}RT}$	Normal/Remote Terminal-Remote Terminal Bit. When set HIGH, BC to RT and RT to BC transfers are performed. When set LOW RT to RT transfers are performed. Two command words are required and two returned status words will be expected.
13	$\overline{SERV\ REQ}$/ Auto-Retry (LSB)	Service Request/Auto-Retry (LSB) Bit. **RT MODE:** A LOW in this bit will cause the service request bit in the status word to be set. **BC MODE:** This is the LSB of the Auto-Retry options. See table on page 15, Bit 14

Table 7: Operation Register (continued)

Bit	Name	Function
14	$\overline{\text{SERR}}$ Auto-Retry (MSB)	Subsystem Error/Auto-Retry (MSB) Bit. **RT MODE:** A LOW in this bit will cause a Subsystem Error Bit in the status word to be set. **BC MODE:** This is the MSB of the Auto-Retry options. **AUTO-RETRY OPERATIONS** **Options selected:** / **If transaction initiated on bus:** **Bit 14** / **Bit 13** / **Primary** / **Secondary** 0 / 0 / No Retry / No Retry 0 / 1 / S / P 1 / 0 / P/S / P/P 1 / 1 / P/S/S / P/P/P
15	$\overline{\text{DBCACC}}$/ Auto-Retry Other Bus	Dynamic Bus Control Accept/Auto-Retry Bus Bit. **RT MODE:** This bit should be LOW if the subsystem is able to accept control of the bus, if offered. **BC MODE:** This bit should be HIGH if an invalid transfer is to be retried according to the selected auto-retry option listed above.

Table 7: Operation Register (continued)

Operation	Function
RESET	RESET INPUT/OUTPUT BUFFERS This command clears both the input and output FIFO buffers. The $\overline{\text{BUFF EF}}$ flag will go low indicating the output buffer is empty.
READ OUTPUT DATA BUFFER	READ OUTPUT FIFO READS the data moved from the INTERNAL RAM in response to an UNLOAD execute operation. The order of the data words corresponds to the same order that they would be received on the 1553B bus. That is the first data word read is the first data word following the COMMAND word. In the 8 bit mode the HIGH BYTE is read FIRST.
WRITE INPUT DATA BUFFER	WRITE INPUT FIFO WRITES the data that will be moved into the INTERNAL RAM in response to a LOAD execute operation. The order of the data words corresponds to the same order that they would be transmitted on the 1553B bus. That is the first data word written is the first data word transmitted following the status word. In 8 bit mode the HIGH BYTE is written FIRST.
EXECUTE OP.	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER 1. I/O BIT HIGH Data currently in INPUT FIFO BUFFER is loaded into the INTERNAL RAM block specified by the T/R BIT and SUBADDRESS FIELD of the OPERATION REGISTER. The INPUT BUFFER must have at least one data word. The $\overline{\text{DONE}}$ interrupt is pulsed when the operation is completed. 2. I/O BIT LOW An entire block of data (32 words) specified by the T/R and the SUBADDRESS field of the OPERATION REGISTER is unloaded from the INTERNAL RAM into the OUTPUT FIFO BUFFER. The $\overline{\text{BUFF EF}}$ Flag goes high when the first data word is moved into the OUTPUT BUFFER. The $\overline{\text{DONE}}$ interrupt is pulsed when the complete message has been moved.

Table 8: Non-Register Operational Commands

EXECUTE OP. WITH RPT OPTION	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER WITH REPEAT OPTION 1. I/O BIT HIGH Data previously written into the INPUT BUFFER is loaded into a new INTERNAL RAM block specified by the T/R and SUBADDRESS field of the OPERATION REGISTER. This operation allows a block of data loaded in the INPUT BUFFER to be repeatedly copied into multiple subaddresses of the INTERNAL RAM without the subsystem having to reload the data. The $\overline{\text{DONE}}$ interrupt is pulsedwwhen the operation is completed. The intent of the operation is to minimize the time required to initialize the INTERNAL RAM. 2. I/O BIT LOW Operation identical to EXECUTE OP. WITHOUT RPT opion.
TRIGGER TRANSACTION TRIGGER TEST	TRANSACTION/TEST TRIGGER This signal executes the desired Bus Controller Function or test of the protocol section determined by the Operation Register.

Table 8: Non-Register Operational Commands (continued)

Operation	$\overline{\text{RD}}$	$\overline{\text{WT}}$	$\overline{\text{DS}}$	AD3	AD2	AD1	AD0
BC AND RT MODE							
No Operation-I/O Bus Tri-stated	x	x	1	x	x	x	x
Read Operation Reg. High Byte	*P	1	0	0	0	0	1
Read Operation Reg. Low Byte	P	1	0	0	0	0	0
Write Operation Reg. High Byte	1	P	0	0	0	0	1
Write Operation Reg. Low Byte	1	P	0	0	0	0	0
Read Output FIFO (High Byte First)	P	1	0	1	1	1	0
Write Input FIFO (High Byte First)	1	P	0	1	1	1	0
Execute Operation (Load/Unload RAM)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Output FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFOS	1	P	0	1	1	0	0
Trigger Test	1	P	0	1	0	0	1
RT MODE ONLY							
Read RT Command Word Reg. High Byte	P	1	0	0	1	0	1
Read RT Command Word Reg. LowByte	P	1	0	0	1	0	0
Read Receive Command Reg. High Byte	P	1	0	0	0	1	1
Read Receive Command Reg. LowByte	P	1	0	0	0	1	0
Read SYNC Data Reg. High Byte	P	1	0	0	1	1	1
Read SYNC Data Reg. Low Byte	P	1	0	0	1	1	0
Write Vector Word Reg. High Byte	1	P	0	0	1	1	1
Write Vector Word Reg. Low Byte	1	P	0	0	1	1	0

*P = Active Low Strobe

Note: When operating in 8-bit mode it is recommended that FIFO access be confined to *even* numbers of Read or Write operations *only*. Failure to conform to this can result in incorrect data being transffered to internal RAM.

Table 9: CT2525/26/27 8-Bit Mode I/O Operations

BC MODE ONLY							
Read Status Word #1 Reg. High Byte	P	1	0	0	0	1	1
Read Status Word #1 Reg. Low Byte	P	1	0	0	0	1	0
Read Status Word #2/RMD Reg. High Byte	P	1	0	0	1	1	1
Read Status Word #2/RMD Reg. Low Byte	P	1	0	0	1	1	0
Write Command Word #1 Reg. High Byte	1	P	0	0	0	1	1
Write Command Word #1 Reg. Low Byte	1	P	0	0	0	1	0
Write Command Word #2/AMD Reg. High Byte	1	P	0	0	1	1	1
Write Command Word #2/AMD Reg. Low Byte	1	P	0	0	1	1	0
Trigger Transaction	1	P	0	1	0	0	1

Table 9: CT2525/26/27 8-Bit Mode I/O Operations (continued)

Operation	$\overline{RD}$	$\overline{WT}$	$\overline{DS}$	AD3	AD2	AD1	AD0
RT AND BC MODE							
No Operation - I/O Bus Tri-Stated	x	x	1	x	x	x	x
Read Operation Register	*P	1	0	0	0	0	0
Write Operation Register	1	P	0	0	0	0	0
Execute Operation (Load/Unload Ram)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Read Output FIFO	P	1	0	1	1	1	0
Write Input FIFO	1	P	0	1	1	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Output FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFO	1	P	0	1	1	0	0
Trigger Test	1	P	0	1	0	0	1
RT MODE ONLY							
Read RT Command Word Register	P	1	0	0	1	0	0
Read Receive Command Register	P	1	0	0	0	1	0
Read SYNC Data Register	P	1	0	0	1	1	0
Write Vector Word Register	1	P	0	0	1	1	0
BC MODE ONLY							
Read Status Word #1 Register	P	1	0	0	0	1	0
Read Status Word #2/RMD Register	P	1	0	0	1	1	0
Write Command Word #1 Register	1	P	0	0	0	1	0
Write Command Word #2/AMD Register	1	P	0	0	1	1	0
Trigger Transaction	1	P	0	1	0	0	1

*P = Active Low Strobe

Table 10: CT2525/26/27 16-Bit Mode I/O Operations

Flat Pack	Plug In	Signal Name	Description
16	16	V_{DD}	Digital Supply Voltage
85	87	V_{DD}	Digital Supply Voltage
2	2	GND	Digital Grounds
34	34	CASE	Case Connection
78	80	GND	Digital Grounds
38	38	VccL (A)	Transceiver A +5VDC Supply Voltage
44	44	VEE (A)	Transceiver A -15VDC Supply Voltage
43	43	Vcc (A)	Transceiver A +15VDC Supply Voltage
39	39	GND (A)	Transceiver A Analog Ground
41	41	GND (A)	Transceiver A Digital Ground
51	53	VccL (B)	Transceiver B +5VDC Supply Voltage
45	47	VEE (B)	Transceiver B -15VDC Supply Voltage
46	48	Vcc (B)	Transceiver B +15VDC Supply Voltage
50	52	GND (B)	Transceiver B Analog Ground
48	50	GND (B)	Transceiver B Digital Ground
79	81	AD_0	Address Inputs
80	82	AD_1	AD_0 - LSB
81	83	AD_2	AD_3 - MSB
82	84	AD_3	These four signals provide the address codes that control the operation of the interface.
83	85	A10 IN	A10IN is the address input to the internal RAM.
84	86	A10 OUT	A10 OUT buffered TX/RX bit when tied to A10IN segregates the 2k by 16 RAM into two 1k by 16 blocks of memory: one for Receive, the other for Transmit Data.
23	23	BCSTEN	Broadcast Enable. When low, the recognition of Broadcast Command is prevented on the specified bus.
25	25	$\overline{\text{BIT DECODE}}$	Built-In Test Decode. When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the Bit Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
57	59	$\overline{\text{BUFF EF}}$	Buffer Empty Flag - goes low when the output FIFO Buffer is empty. Will transition to the high state when the first word appears in the Buffer.

Table 11: Pin Numbers - CT2525

Flat Pack	Plug In	Signal Name	Description
1	1	CLOCK	6 MHz Master Clock.
42	42	DATA CHA	DATA CHANNEL A. (BUS 0). This is the combined signals, RX Data In and TX Data Out, that connect to the IN phase primary terminal of the Bus Transformer.
40	40	$\overline{\text{DATA CHA}}$	$\overline{\text{DATA CHANNEL A}}$. (BUS 0) This is the combined signals $\overline{\text{RX Data In}}$ and $\overline{\text{TX Data Out}}$, that connect to the OUT of phase primary terminal of the Bus Transformer.
47	49	DATA CHB	Same as DATA CHA, except for Channel B. (BUS 1).
49	51	$\overline{\text{DATA CHB}}$	Same as $\overline{\text{DATA CHA}}$, except for Channel B. (BUS 1).
62	64	DB_0	I/O DATA BUS. Data Bus for all SUBSYSTEM READ and WRITE OPERATIONS.
63	65	DB_1	
64	66	DB_2	
65	67	DB_3	**16 BIT MODE** **8 BIT MODE**
66	68	DB_4	
67	69	DB_5	DB_0 = LSB DB_0/DB_8 = LSB
68	70	DB_6	DB_{15} = MSB DB_7/DB_{15} = MSB
69	71	DB_7	
70	72	DB_8	When used in 8 BIT MODE the data bus must be
71	73	DB_9	connected as follows:
72	74	DB_{10}	
73	75	DB_{11}	DB_0 TO DB_8 DB_4 TO DB_{12}
74	76	DB_{12}	DB_1 TO DB_9 DB_5 TO DB_{13}
75	77	DB_{13}	DB_2 TO DB_{10} DB_6 TO DB_{14}
76	78	DB_{14}	DB_3 TO DB_{11} DB_7 TO DB_{15}
77	79	DB_{15}	
54	56	$\overline{\text{DBCREQ}}$	Dynamic Bus Control Request. If OPERATION Register bit i5 is set LOW, this line will pulse LOW in response to a Valid Dynamic Bus Control Mode Command, indicating ACCEPTANCE of Bus Control Function.
88	90	$\overline{\text{DS}}$	Device Select. This signal must be low before the interface can be selected for an I/O Read or Write function. The I/O Data Bus will remain tri-stated, no operations will be executed when this signal is high.

Table 11: Pin Numbers - CT2525 (continued)

Flat Pack	Plug In	Signal Name	Description
58	60	$\overline{\text{DONE}}$	Interrupt (See Interrupt Table for description.)
24	24	$\overline{\text{ENABLE}}$	Enable. When held low, enables $\overline{\text{Bit Decode}}$, $\overline{\text{Next Status}}$, and $\overline{\text{Status Update}}$ program lines.
60	62	$\overline{\text{INT \#1}}$	Good Block (RT) / VALID (BC) Interrupt (See Interrupt Table for description).
61	63	$\overline{\text{INT \#2}}$	VALID Transaction (RT) / INVALID (BC) Interrupt (See Interrupt Table for description).
33	33	$\overline{\text{LTFAIL}}$	Loop Test Fail. This line goes low if any error in the terminal's own transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
3	3	$\overline{\text{MEREQ}}$	To set the Message Error bit in the Status Word, this signal must go low within 650 nsec of $\overline{\text{INCMD}}$ going low and remain valid for the DURATION of $\overline{\text{INCMD}}$.
55	57	$\overline{\text{MODEREST}}$	Mode Reset. This line pulses low for 500 ns on completion of the servicing of a valid Reset Remote Terminal Mode Command.
28	28	M16/$\overline{8}$	Programs Interface for 8 Bit or 16 Bit Data Buses. 16/$\overline{8}$ = LOW (0) 8 BIT MODE 16/$\overline{8}$ = HIGH (1) 16 BIT MODE
53	55	$\overline{\text{NBGT}}$	New Bus Grant. Pulses low whenever a new command is accepted.
26	26	$\overline{\text{NEXT STATUS}}$	Next Status. When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
56	58	$\overline{\text{PASS}}$	Pass. Interrupt indicates that the protocol self-test has completed with no faults.
86	88	$\overline{\text{RD}}$	Read Strobe. Must GO LOW together with $\overline{\text{DS}}$ to perform a READ OPERATION. Note: $\overline{\text{WT}}$ STROBE MUST BE HIGH.
59	61	$\overline{\text{RETRY}}$	Retry Interrupt (See Interrupt Table for description)
31	31	$\overline{\text{RESET}}$	System MASTER Reset. When low resets all registers and INPUT/OUTPUT FIFO buffers. Minimum Low Time for reset 0.5 usec.
17	17	RTADPAR	RT Address Parity. This must be hardwired by the user to give odd parity.

Table 11: Pin Numbers - CT2525 (continued)

Flat Pack	Plug In	Signal Name	Description
22 21 20 19 18	22 21 20 19 18	$RTAD_0$ $RTAD_1$ $RTAD_2$ $RTAD_3$ $RTAD_4$	RT Address Lines. These should be hardwired by the user. $RTAD_4$ is the most significant bit.
32	32	$\overline{RTADER}$	Remote Terminal Address Error. This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
11 13 15 14 12	11 13 15 14 12	SA_0 SA_1 SA_2 SA_3 SA_4	Subaddress. These five lines are a label for the data being transferred. Valid when $\overline{INCMD}$ is low. SA_4 is the most significant bit.
52	54	$\overline{SELFTEST}$	Self Test Interrupt indicates that the Initiate Self Test Mode Command is being served.
27	27	$\overline{STATUSUPDATE}$	Status Update. When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence.
36	36	$\overline{SYNCND}$	Synchronize No Data Interrupt (See Interrupt Table for description).
37	37	$\overline{SYNCWD}$	Synchronize with Data Interrupt (See Interrupt Table for description).
29	29	TEST #I	Test #1 Factory Test Point (Do not connect).
30	30	TEST #2	Test #2 Factory Test Point (Do not connect).
8	8	TX/$\overline{RX}$	Transmit/$\overline{Receive}$. The state of this line informs the subsystem whether it is to transmit or receive data. The signal is valid while $\overline{INCMD}$ is low.
35	35	$\overline{VECTOR}$	Vector Interrupt (See Interrupt Table for Description).
4 5 7 9 10	4 5 7 9 10	WC_0 WC_1 WC_2 WC_3 WC_4	Word Count. These Five lines specify the requested number of Data Words to be received or transmitted. Valid when $\overline{INCMD}$ is low. WC_4 is the most significant bit.
87	89	$\overline{WT}$	Write Strobe. Must GO LOW together with $\overline{DS}$ to perform a write operation. NOTE: $\overline{RD}$ must be high.
6	6	$\overline{INCMD}$	IN COMMAND. Goes low when the interface is servicing a valid command. Can be utilized to enable external firm-ware to illegalize subaddresses and mode command not allowed by some subsystem designs. NOTE: Refer to $\overline{MEREQ}$ signal description for details.

Table 11: Pin Numbers - CT2525 (continued)

	FP	DIP	SIGNAL CT2525	2526	2527	2528
	[1]	1	6MHZCLOCK INPUT	*	*	*
	[2]	2	GND [LOGIC]	*	*	*
	[3]	3	MEREQ-	*	*	*
	[4]	4	WC0	*	*	*
	[5]	5	WC1	*	*	*
	[6]	6	INCMD-	*	*	*
	[7]	7	WC2-	*	*	*
	[8]	8	T/R-	*	*	*
	[9]	9	WC3	*	*	*
	[10]	10	WC4	*	*	*
	[11]	11	SA0	*	*	*
	[12]	12	SA4	*	*	*
	[13]	13	SA1	*	*	*
	[14]	14	SA3	*	*	*
	[15]	15	SA2	*	*	*
	[16]	16	+5V [V_{DD}]	*	*	*
	[17]	17	RTADPAR	*	*	*
	[18]	18	RTAD4	*	*	*
	[19]	19	RTAD3	*	*	*
	[20]	20	RTAD2	*	*	*
	[21]	21	RTAD1	*	*	*
	[22]	22	RTAD0	*	*	*
	[23]	23	BCSTEN	*	*	*
	[24]	24	ENABLE-	*	*	*
	[25]	25	BITDECODE-	*	*	*
	[26]	26	NEXTSTATUS-	*	*	*
	[27]	27	STATUSUPDATE-	*	*	*
	[28]	28	MODE 16/8-	*	*	*
	[29]	29	TEST1	*	*	*
	[30]	30	TEST2	*	*	*
	[31]	31	RESET- [MASTER]	*	*	*
	[32]	32	RTADER-	*	*	*
	[33]	33	LTFAIL-	*	*	*
	[34]	34	CASE	*	*	GND [LOGIC]
	[35]	35	VECTOR-	*	*	*
	[36]	36	SYNCND-	*	*	*
	[37]	37	SYNCWD-	*	*	*
	[38]	38	V_{CC}L [TX/RX/LOGIC]	*	*	RXDATA0
	[39]	39	GNDA	*	N/C	N/C
	[40]	40	DATA CHA-	*	*	RXDATA0-
BUS 0	[41]	41	GNDA	*	OUTPUT GND A	N/C
	[42]	42	DATA CHA	*	*	TXINHIBIT0
	[43]	43	+15V V_{CC} (A)	*	ANALOG GND A	N/C
	[44]	44	-15V V_{EE} (A)	*	DIGITAL GND A	TXDATA
		45	N/C	*	*	*

[XX] = FLAT PACK
XX = DIP PACKAGE

Table 12: CT2526-28 Series Pinout

	FP	DIP	SIGNAL CT2525	2526	2527	2528
	[88]	90	DS-	*	*	*
	[87]	89	WT-	*	*	*
	[86]	88	RD-	*	*	*
	[85]	87	+5V [V_{DD}]	*	*	*
	[84]	86	A10 [OUT]	*	*	*
	[83]	85	A10 [IN]	*	*	*
	[82]	84	AD3	*	*	*
	[81]	83	AD2	*	*	*
	[80]	82	AD1	*	*	*
	[79]	81	AD0	*	*	*
	[78]	80	GND [LOGIC]	*	*	*
	[77]	79	DB15	*	*	*
	[76]	78	DB14	*	*	*
	[75]	77	DB13	*	*	*
	[74]	76	DB12	*	*	*
	[73]	75	DB11	*	*	*
	[72]	74	DB10	*	*	*
	[71]	73	DB9	*	*	*
	[70]	72	DB8	*	*	*
	[69]	71	DB7	*	*	*
	[68]	70	DB6	*	*	*
	[67]	69	DB5	*	*	*
	[66]	68	DB4	*	*	*
	[65]	67	DB3	*	*	*
	[64]	66	DB2	*	*	*
	[63]	65	DB1	*	*	*
	[62]	64	DB0	*	*	*
	[61]	63	VALIDXMIT-/INVLDTXFR-	*	*	*
	[60]	62	GOODBLK-/VALIDTXFR-	*	*	*
	[59]	61	RETRY-	*	*	*
	[58]	60	DONE-	*	*	*
	[57]	59	BUFFEF-	*	*	*
	[56]	58	PASS-	*	*	*
	[55]	57	MODERESET-	*	*	*
	[54]	56	DBCREQ-	*	*	*
	[53]	55	NBGT-	*	*	*
	[52]	54	SELFTEST-	*	*	*
	[51]	53	V_{CC}L (B) [TX/RX/LOGIC]	*	*	RXDATA1-
	[50]	52	GND (B)	*	N/C	N/C
	[49]	51	DATA CHB-	*	*	TXINHIBIT1
BUS 1	[48]	50	GND (B)	*	OUTPUT GND (B)	N/C
	[47]	49	DATA CHB-	*	*	RXDATA1
	[46]	48	+15V (B) V_{CC} (B)	*	ANALOG GND(B)	N/C
	[45]	47	-15V (B) V_{EE} (B)	*	DIGITAL GND (B)	TXDATA-
		46	N/C			

Table 12: CT2526-28 Series Pinout (continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	N/C	26	ENABLE	51	N/C	76	DS
2	N/C	27	BITDECODE	52	DB2	77	N/C
3	6MHz [IN]	28	N/C	53	DB3	78	N/C
4	GND [LOGIC]	29	N/C	54	DB4	79	N/C
5	MEREQ	30	NEXTSTATUS	55	DB5	80	GND [LOGIC]
6	WC0	31	STATUSUPDATE	56	DB6	81	RETRY
7	WC1	32	MODE 16/8	57	DB7	82	RX DATA [IN] BUS 1
8	INCMD	33	TEST1 [FACTORY T.P. DO NOT CONNECT]	58	DB8	83	N/C
9	WC2			59	DB9	84	RX DATA [IN] BUS 1
10	T/R			60	DB10	85	PASS
11	WC3	34	RESET [MASTER]	61	DB11	86	TX INHIBIT BUS 1
12	WC4	35	RTADER	62	DB12	87	+5V [LOGIC]
13	SA0	36	LTFAIL	63	DB13	88	GND [LOGIC]
14	SA4	37	SYNCND	64	DB14	89	TX DATA
15	SA1	38	SYNCWD	65	DB15	90	N/C
16	SA3	39	N/C	66	GND [LOGIC]	91	TX DATA
17	SA2	40	SELFTEST	67	AD0	92	N/C
18	+5V [LOGIC]	41	NBGT	68	AD1	93	TX INHIBIT BUS 0
19	RTADPAR	42	DBCREQ	69	AD2	94	N/C
20	RTAD4	43	MODERESET	70	AD3	95	VECTOR
21	RTAD3	44	BUFFEF	71	AD10 IN	96	RX DATA [IN] BUS 0
22	RTAD2	45	DONE	72	AD10 OUT	97	N/C
23	RTAD1	46	GOODBLK/ VALIDTXFR	73	+5V [LOGIC]	98	RX DATA [IN] BUS 0
24	RTAD0	47	VALIDXMIT/ INVLDTXFR	74	RD	99	TEST2 [FACTORY T.P. DO NOT CONNECT]
25	BCSTEN	48	DBO	75	WT	100	N/C
		49	DB1				
		50	N/C				

Table 13: CT2529 Quad Flatpack Pinout

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{WPW}	Write Pulse Width	50			nsec	1, 2
t_{RPW}	Read Pulse Width	50			nsec	3
t_{AS}	Address Set Up Time	5			nsec	
t_{AH}	Address Hold Time	5			nsec	
t_{DS}	Write Data Set Up Time	5			nsec	
t_{DH}	Write Data Hold Time	0			nsec	2
t_{DA}	Read Data Access Time			50	nsec	
t_{IPW}	Interrupt Pulse Width	140	160	180	nsec	4
t_{REC}	Recovery Time	100			nsec	

Conditions: ($-55°C \leq T_A \leq +125°C$) $V_{CC} = +5.0V \pm 10\%$

Notes: 1. Write pulse width t_{WPW} is the time when both $\overline{DS}$ and $\overline{WT}$ are simultaneously low. Either $\overline{DS}$ or $\overline{WT}$ may go low or return high first.

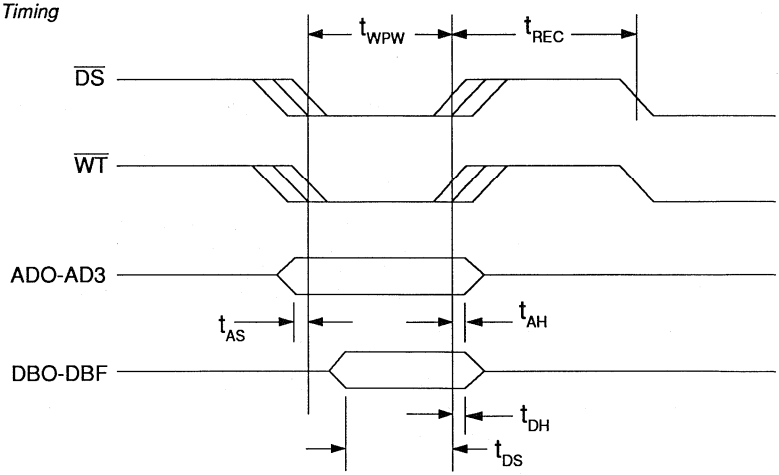
2. Write hold time: $t_{DH} = 0$ for $t_{WPW} \geq 450nsec$
   $t_{DH} = 10nsec$ for $50nsec < t_{WPW} < 450nsec$

3. Read pulse time t_{RPW} is the time where both $\overline{DS}$ and $\overline{RD}$ are simultaneously low. Either $\overline{DS}$ or $\overline{RD}$ may go low or return high first.

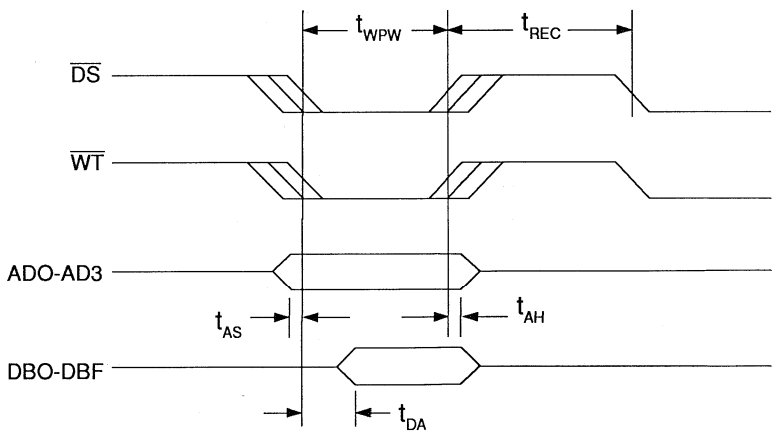
4. Refer to "Discrete Interrupt" text for further information.

Table 14: CT2525/26/27/28 AC Electrical Characteristics

I/O Write Timing



I/O Read Timing



Output Interrupts

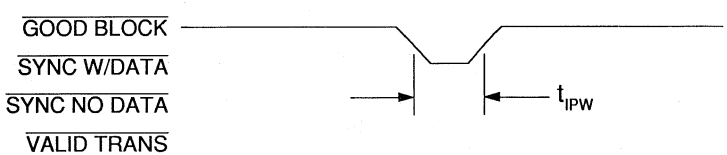


Figure 6: CT2525/26/27/28 Subsystem Interface Timing

Signal Name	Function
A0 - A3	INPUT ADDRESS A0 = LSB A3 = MSB These four signals provide the address codes that control the operation of the interface.
$\overline{DS}$	$\overline{DEVICE\ SELECT}$ Used in conjunction with the address signals. The input/output interface data bus will remain tri-stated and no operation will be executed when this signal is high, regardless of the state of the address signals. $\overline{DS}$ = LOW (0) INTERFACE SELECTED $\overline{DS}$ = HIGH (1) INTERFACE NOT SELECTED
DB0-DB15	I/O DATA BUS Data Bus for all SUBSYSTEM READ and WRITE OPERATIONS. **16 BIT MODE** **8 BIT MODE** DB0 = LSB DB0/DB8 = LSB DB15 = MSB DB7/DB15 = MSB When used in 8 BIT MODE the data bus must be connected as follows: DB0 TO DB8 DB4 TO DB12 DB1 TO DB9 DB5 TO DB13 DB2 TO DB10 DB6 TO DB14 DB3 TO DB11 DB7 TO DB15
16/$\overline{8}$	PROGRAMS INTERFACE FOR 8 BIT OR 16 BIT DATA BUSES 16/$\overline{8}$ = LOW (0) 8 BIT MODE 16/$\overline{8}$ = HIGH (1) 16 BIT MODE
$\overline{MASTER\ RESET}$	SYSTEM RESET When low resets all registers and INPUT/OUTPUT buffers. Minimum Low Time for reset = 0.5 usec.
$\overline{WT}$	WRITE STROBE Must GO LOW together with $\overline{DS}$ to perform a WRITE OPERATION. NOTE: RD MUST BE HIGH.
$\overline{RD}$	READ STROBE Must GO LOW together with DS to perform a READ OPERATION. NOTE: WT STROBE MUST BE HIGH.
INTERRUPTS	Refer to DISCRETE INTERRUPT TABLE.

Table 15: CT2525/26/27 Subsystem Interface Signals

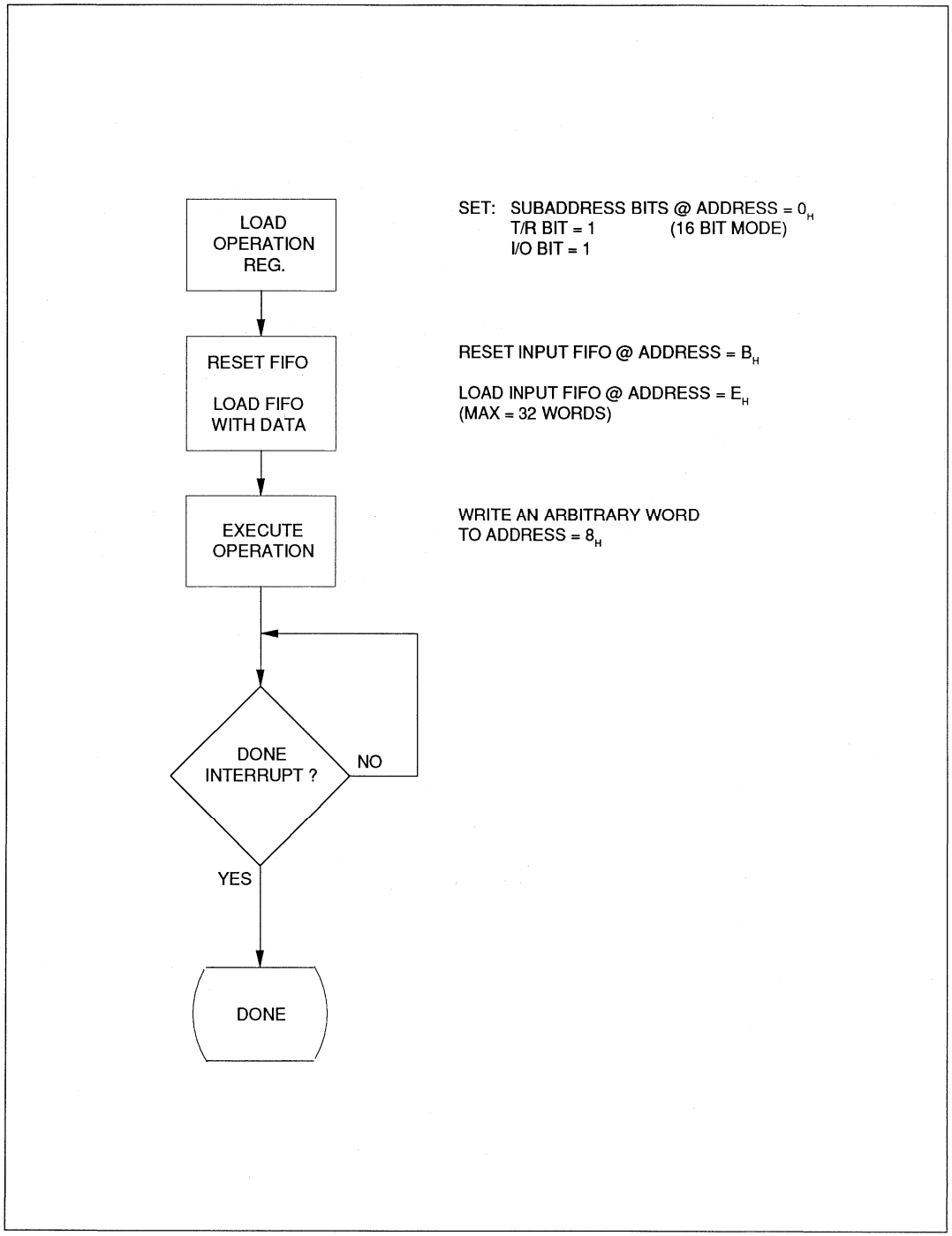


Figure 7: CT252X Flowchart # 1 - Load Data into Transmit RAM

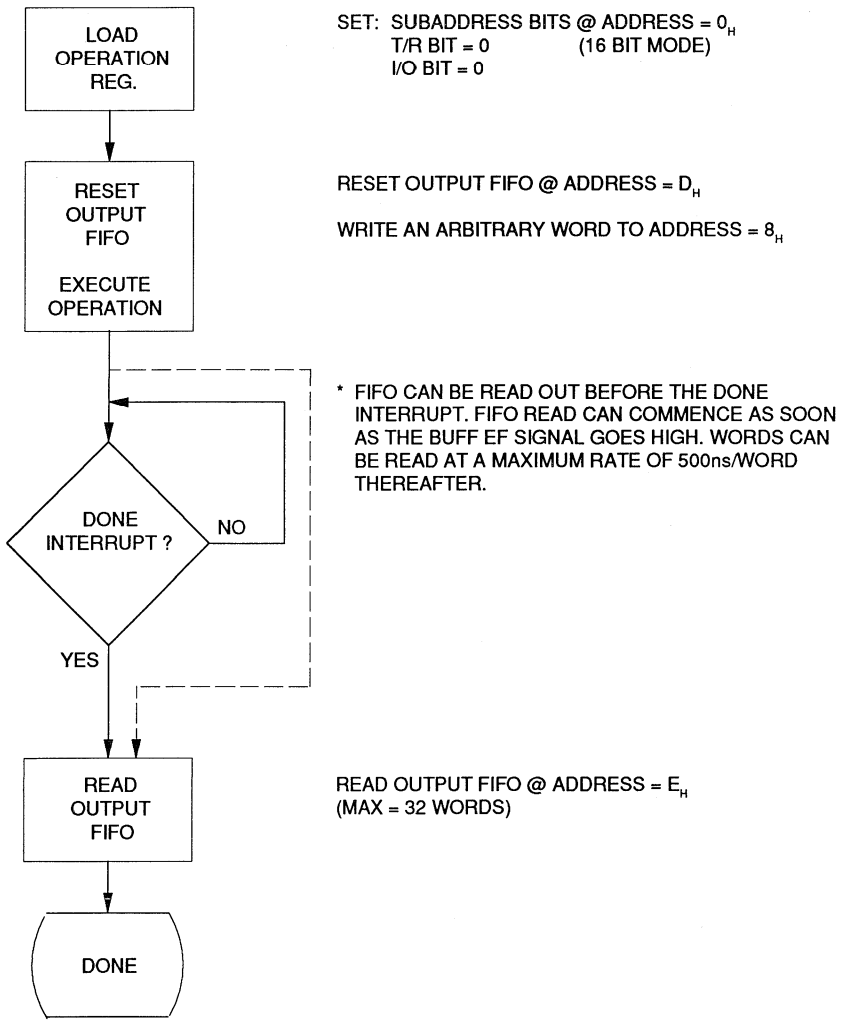


Figure 8: CT252X Flowchart # 2 - Unload Data from Receive RAM

PACKAGE OUTLINES

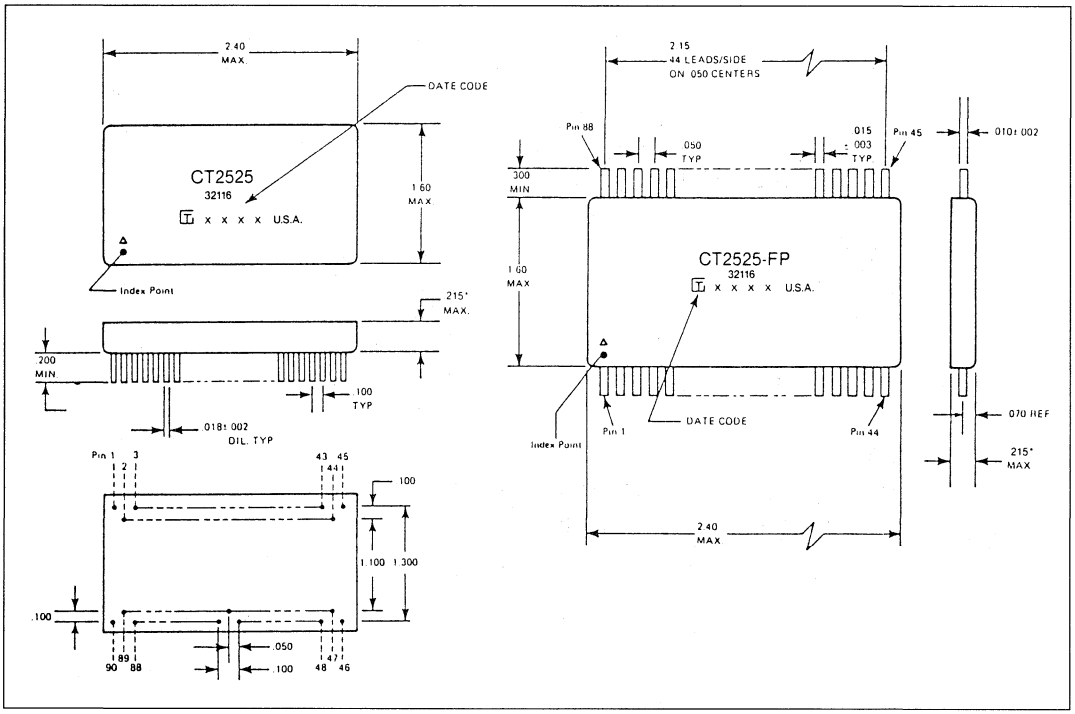


Figure 9: Package Outline for CT2525/26/27

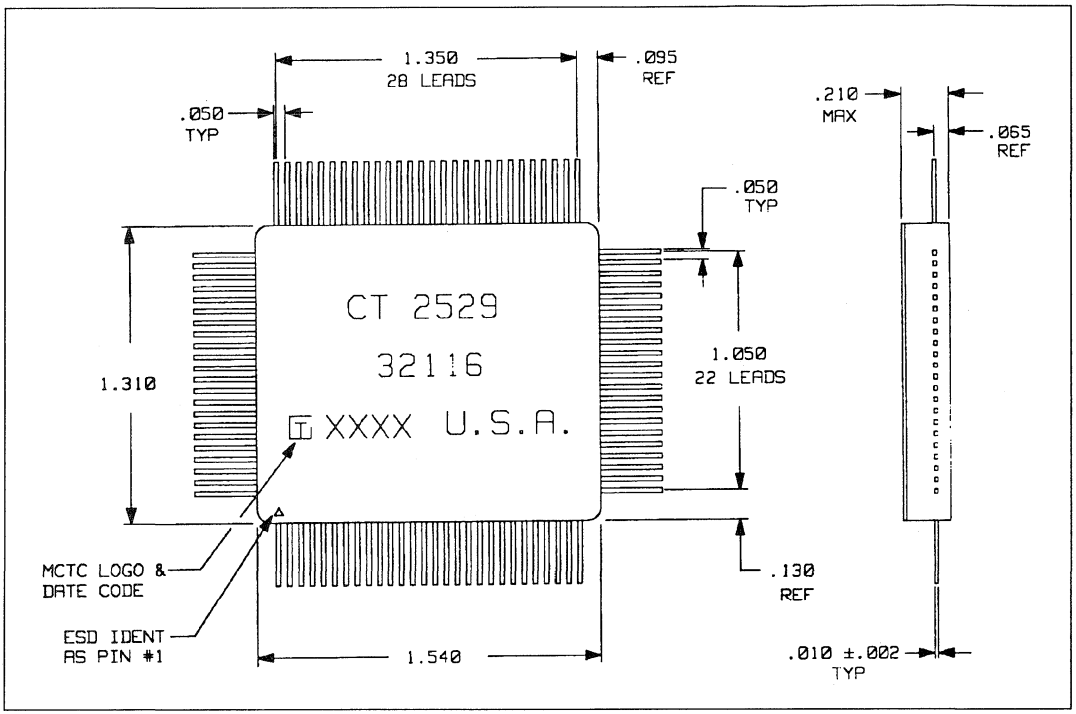


Figure 10: Package Outline for CT2529

CT2553 Series

MIL-STD-1553B INTERFACE UNIT

GENERAL DESCRIPTION

The CT2553 provides a complete dual redundant MIL-STD-1553B Bus Control Terminal, Remote Terminal and Bus Monitor mounted in a 78 pin quad in line package. This device provides an intelligent interface between either a single or dual redundant 1553B data highway, and most common microprocessors or microprocessor based systems.

The device is based on GPS's CMOS single chip BC/RT/BM device, only transformers and/or Isolation resistors are required for connection to a data bus. The device also includes two 8K x 8 bit RAMS, a pair of low power transceivers and a single chip subsystem interface gate array.

The interface appears to the host processor as an 8K x 16 bit (expandible to 64K x 16 bit) area of shared memory and a minimum of 3 (expandible to 7) register locations. Provision is made within the design of the interface to ensure that data integrity can be maintained at both word and message levels.

In its Remote Terminal mode of operation the device implements all of the RT options of MIL-STD-1553B; ie all message formats, all status bits and all mode commands. As a Bus Control Terminal the device can be programmed to autonomously perform up to 64 1553B transactions interrupting the host processor either on detection of an error condition or at the end of a message frame. As a Bus Monitor the device monitors both 1553B data buses and stores all received command, status and data words in a circular stack along with appropriate identification words.

FEATURES

- Single package device providing comprehensive Bus Control/Remote/Terminal/Bus Monitor MIL-STD-1553B Interface
- Integral dual redundant 1553B Low Power transceiver capable of meeting the requirements of both MIL-STD-1553B and MIL-STD-1760
- Integral 8K x 16 bit pseudo dual port RAM
- Integral custom gate array providing full memory confention resolution and control
- Provides comprehensive built in test features
- Utilizes co-fired ceramic technology, offering lighter weight and better reliability
- Low power dissipation
- 78 pin quad in line package
- Operates over the full military temperature range
- Pin for pin functional equivalent to DDC BUS61553

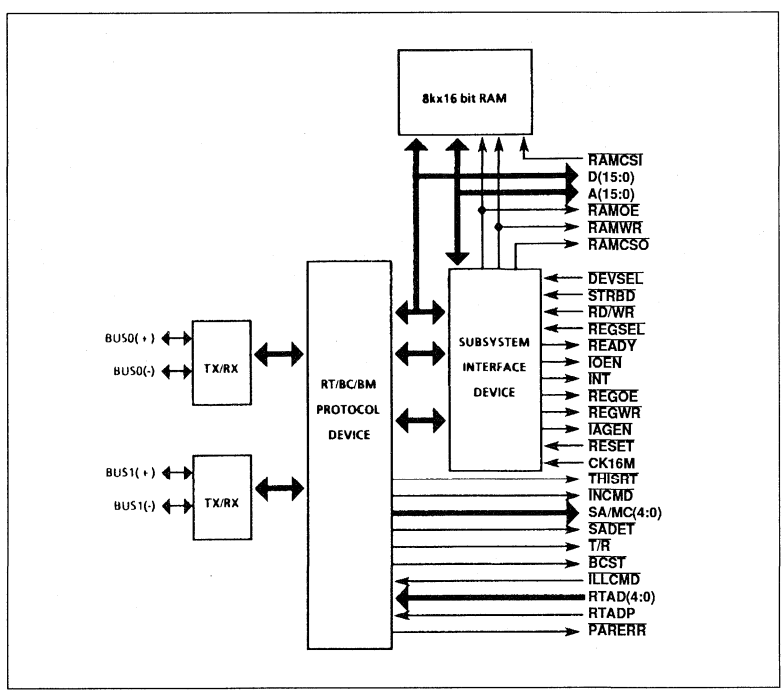


Figure 1: Block Diagram

REGISTERS

$\overline{REGSEL}$	A2	A1	A0	DIR	REGISTER
1	X	X	X	-	No Register Selected
0	0	0	0	R/W	Interrupt Mask Register
0	0	0	1	R/W	Configuration Register
0	0	1	0	-	No Register Selected
0	0	1	1	W	Start/Reset Register
0	1	0	0	R/W	External Register
0	1	0	1	R/W	External Register
0	1	1	0	R/W	External Register
0	1	1	1	R/W	External Register

Selection of internal/external registers is by asserting $\overline{REGSEL}$ low. The address inputs A2, A1 and A0 are used to specify a particular register. The device contains 3 internal registers, and also provides for 4 external registers to be implemented with the addition of external hardware.

Table 1: Register Address Definition

BIT	NAME	DESCRIPTION
0	EOM	Logic 1 allows $\overline{INT}$ output to go active at end of every transaction in both BC and R modes.
1	SPARE	Set to logic 1.
2	ERROR	Logic 1 allows $\overline{INT}$ output to go active at end of every transaction in BC mode in which any of the following errors occur: *Loop test fail *Invalid message *Response timeout *Status bit(s) set
3	EOF	Logic 1 allows $\overline{INT}$ output to go active at end of current message frame (Message count = FFFF).
4-15	SPARE	Set to logic 1.

This internal 16 bit read/write register is used to enable/mask interrupt conditions. If an interrupt condition occurs, and the relevant Interrupt Mask Register bit is set to a logic 1, then an active low interrupt pulse will be produced at the $\overline{INT}$ (pin 72) output at the end of the current transaction.

Table 2: Interrupt Mask Register

BIT	NAME	DESCRIPTION
0-7	SPARE	Set to logic 1.
3	$\overline{SSF}$	In RT mode set to logic 0 in order to set 1553B status word subsystem flag bit.
9	$\overline{SR}$	In RT mode set to logic 0 in order to set 1553B status word service request bit.
10	$\overline{BUSY}$	In RT mode set to logic 0 in order to set 1553B status word busy bit.
11	$\overline{DBAC}$	In RT mode set to logic 0 in order to set 1553B status word dynamic bus control accept bit.
12	SOE	In BC mode set to logic 1 in order to cause device to terminate a frame of transactions on detectionoof an error.
13	B/$\overline{A}$	In RT and BC mode selects either buffer A or buffer B as the current working area for the device.
14	BM	
15	RT/$\overline{BC}$	

BM	RT/$\overline{BC}$	Operation
0	0	BC
1	0	BM
0	1	RT
1	1	Invalid

This internal 16 bit read/write register is used to define the mode of operation of the device and to support the double buffering of information. In RT mode it is used to set selective 1553B status bits. In BC mode it is used to select the stop on error option.

Table 3: Configuration Register

BIT	NAME	DESCRIPTION
0	RESET	Set to logic 1 in order to reset device to power on state.
1	START	Set to logic 1 in order to either initiate transmission of a frame of transactions in BC mode or to allow reception of 1553B words in BM mode.
2-15	SPARE	Set to logic 1.

This internal 16 bit write only register can be used either to reset the device, or to initiate BC or BM operation.

Table 4: Start/Reset Register

MEMORY MANAGEMENT

The CT2553 memory area can be configured as two separate areas, each with its own sequential stack and pointer. The memory is a pseudo dual port shared memory area to which the host CPU has access to it all times. Word level data integrity is automatically implemented in such a manner as to be transparent to the host CPU. Message level data integrity can be maintained by ensuring that the device and host CPU never access the same area of shared memory at the same time - this can be achieved by the host CPU monitorina and altering the state of the Configuration Register B/$\overline{A}$ bit.

In RT and BC mode the memory is subdivided into Data Blocks and Descriptor Stacks, the Descriptor Stacks are mapped usinq a pair of Stack Pointers at pre-defined memory locations - Stack Pointer A at 0100 (hex) and Stack Pointer B at 0104 (hex).

In RT mode the Data Blocks are mapped using a pair of Look Up Tables at pre-defined memory locations 0140-017F (hex) and 01C0-01FF (hex) for areas A and B respectively. In BC mode the Data Blocks are mapped using pointers located within the Descriptor Stacks. Associated with each Stack Pointer in BC mode is a Messaae Count location at the fixed addresses 0101 (hex) and 0105 (hex) - these messaae counts define the number of transactions to be performed by the BC in a single frame. In BM mode the device writes 1553B information into one of two circular stacks dependinq on the level of the B/$\overline{A}$ bit, the first location of these stacks is defined by the two Stack Pointers - 0100 (hex) and 0104 (hex).

REMOTE TERMINAL OPERATION

In its RT mode of operation, receipt of a valid 1553 command wordwwill cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtaln the latest Descriptor Stack address.
- Write a Block Status Word and the received command word into the appropriate Descriptor Stack locations.
- Form a Look Up Table address using the received command word and the B/$\overline{A}$ bit, then read the relevant Data Block address value.
- Read from/write to the Data Block, the data words associated with the current transaction.
- Transmit into the 1553 data bus its 1553B status word followed by the required number of data words.
- At the end of the transaction, pulse the $\overline{INT}$ output active low if the relevant Interrupt Mask Register bit is set.
- Finally update the Block Status Word and the Time Tag location, then increment the Stack Pointer by 4 ready for the reception of the next valid command word.

BIT	NAME	DESCRIPTION
0-7	SPARE	Set to logic 1.
8	LTFAIL	Logic 1 indicates that the device has faiied its loop test.
9	RESPTO	Logic 1 indicates that the device, when operating in BGmode, has timed out an RT status response.
10	ERROR	Logic 1 indicates that the device has 1553B format error.
11	STATUS	Logic 1 indicates that the device, when operating in BC mode, has detected a bit set in an RT status response.
12	ERROR	Logic 1 indicates that the device has detected any of the error conditions identified by bits 8-11.
13	$\overline{BUS0}$	Logic 0 indicates latest transaction received on 1553 channel 0, logic 1 indicates latest transaction received on 1553 channel 1.
14	SOM	Logic 1 indicates device has started a message transfer.
15	EOM	Logic 1 indicates device has completed a message transfer.

Table 5: Block Status Word

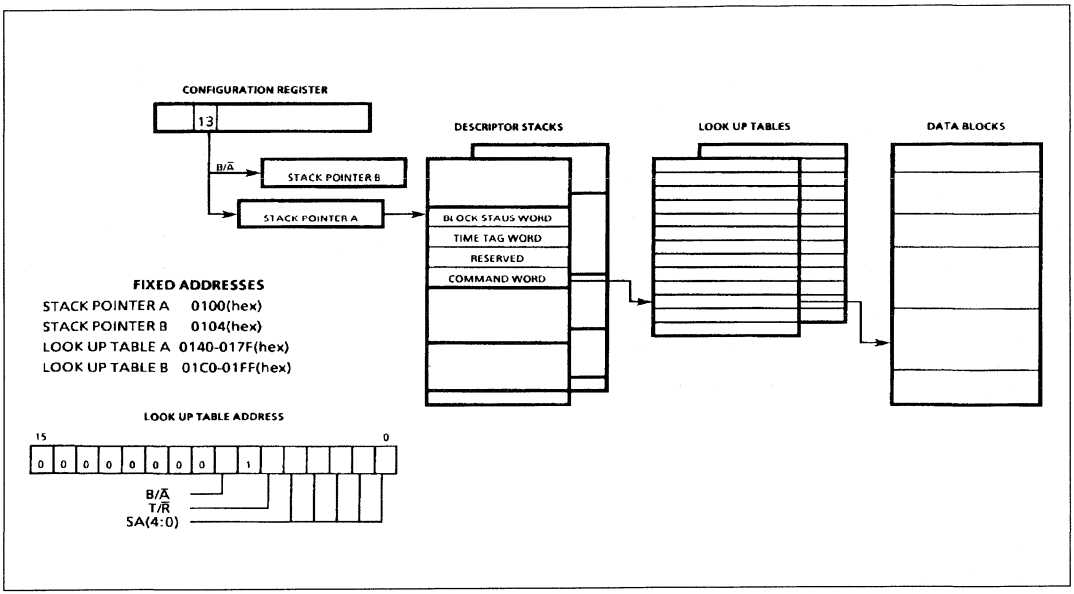


Figure 2: RT Mode Memory Operations

In its BC mode of operation, the action of the host CPU writing a logic 1 to the Start bit in the Start/Reset Register win cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtain the latest Descriptor Stack address.
- Write a Block Status Word into, and read the Message Block address from, the appropriate Descriptor Stack locations.
- Use the Message Block Address to read the relevant Data Block - thls will contain the BC Control Word the command word(s) and the data word(s) associated with the current transaction.
- Transmit the command word(s) and the data word(s), as required, on the 1553 data bus.
- Receive and check any status and data words associated with the current transaction then write them to the Data Block.
- At the end of the transaction pulse the $\overline{INT}$ output active low if the relevant Interrupt Mask Register bit is set.
- Finally update the Block Status Word, and increment the Stack Pointer by 4 and the appropriate Message Counter by 1.
- If the Message Counter contains a value of FFFF (hex) then the device waits for the next "Start" Instruction, otherwise it performs the next transaction in the Descnptor Stack.

BIT	NAME	DESCRIPTION
0	RT-RT	Logic 1 indicates current transaction is a RT-RT transfer.
1	BCST	Logic 1 indicates current transaction involves a Broadcast Command
2	MODE	Logic 1 indicates current transaction is a mode transfer.
3	SPARE	Set to logic 1.
4	SPARE	Set to logic 1.
5	MASKBCR	Logic 1 indicates that detection of the Broadcast Command Received bit in the RT Status Word associated with the current transaction will not result in an error being reported. If the BCR bit is not set then a Format Error will be reported.
6	OLTEST	Logic 1 indicates that the device is to perform an internal off line self test.
7	$\overline{BUS0}$	Logic 0 indicates latest transaction received on 1553 channel 0 logic 1 indicates latest transaction received on 1553 channel 1.
8-15	SPARE	Set to logic 1.

Table 6: BC Control Word

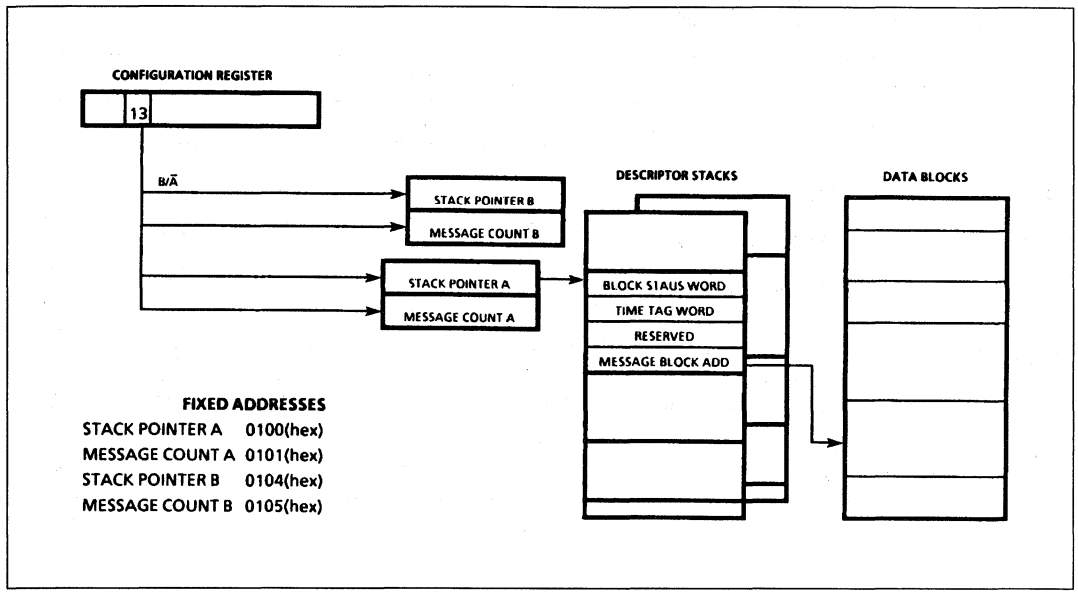


Figure 3: BC Mode Memory Operations

BUS MONITOR OPERATION

In its BM mode of operation, the action of the host CPU writing a logic 1 to the Start bit in the Start/Reset Register will cause the CT2553 to:

- Examine the state of the B/$\overline{A}$ bit in its Configuration Register.
- Read the appropriate Stack Pointer from the memory in order to obtain the first address of the Monitor Stack.

Upon reception of every 1553 word the device will:

- Write the word into the location addressed by its internal Monitor Stack Pointer register (not available to the host CPU).
- Increment its internal Monitor Stack Pointer register.
- Write a BM Identification word into the location addressed by its internal Monitor Stack Pointer register.
- Increment its internal Monitor Stack Pointer register.

BIT	NAME	DESCRIPTION
0	$\overline{\text{MODE}}$	Logic 0 indicates a mode command received.
1	$\overline{\text{GAP}}$	Logic 0 indlcates a greater than 2 microsec gap between the previous and current words.
2	CHA1B0	Logic 1 indicates the word was recelved on 1553 bus A. Logic 0 indicates the word was received on 1553 bus B.
3	$\overline{\text{DATA}}$	Logic 0 indicates the word was received had a data sync.
4	ERROR	Logic 1 indicates a Manchester, Parity, Sync or bit count error.
5	$\overline{\text{BCST}}$	Logic 0 indicates that the command/ status address field is set to 11111.
6	$\overline{\text{THISRT}}$	Logic 0 indicates that the command/ status address field matches the RT Address of the MCT81553.
7	SPARE	Set to logic 1.
8-15	GAP TIME	Indicates the time in 0.5 microsec increments between the previous and current words.

Table 7: Bus Monitor Identification Word

PRELIMINARY SPECIFICATIONS (CT2553)

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Power supply voltage		V_{CC}	4.5	5.0	5.5	V
		V_{EE}	-14.25	-15.0	-15.75	V
Power supply current	@ standby	I_{CC}	-	TBA	170	mA
		I_{EE}	-	TBA	80	mA
	@ 25% duty cycle	I_{CC}	-	TBA	170	mA
		I_{EE}	-	TBA	130	mA
	@ 100% duty cycle	I_{CC}	-	TBA	TBA	mA
		I_{EE}	-	TBA	TBA	mA
Power dissipation	@ standby	P_0	-	TBA	TBA	W
	@ 25% duty cycle	P_{25}	-	TBA	TBA	W
	@ 100% duty cycle	P_{100}	-	TBA	TBA	W
Operating temperature (case)		T_O	-55	-	+125	deg C
Storage temperature (case)		T_S	-65	-	+150	deg C

Table 8: Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Differential I/P impedance (DC to 1MHz)	Zin	10K	-	-	ohms
Differential I/P voltage	Vidr	-	-	+/-20	Vp-p
Input common mode rejection range	Vicr	-	-	+/-10	Vp-p
Common mode rejection ratio	CMRR	40	-	-	dB
I/P threshold - sinewave @ 1MHz *	Vth1	0.8	0.9	1.0	Vp-p
Filter characteristics @ 2MHz	Vth2	-	2.4	-	Vp-p
Filter characteristics @ 3MHz	Vth3	9.0	-	-	Vp-p

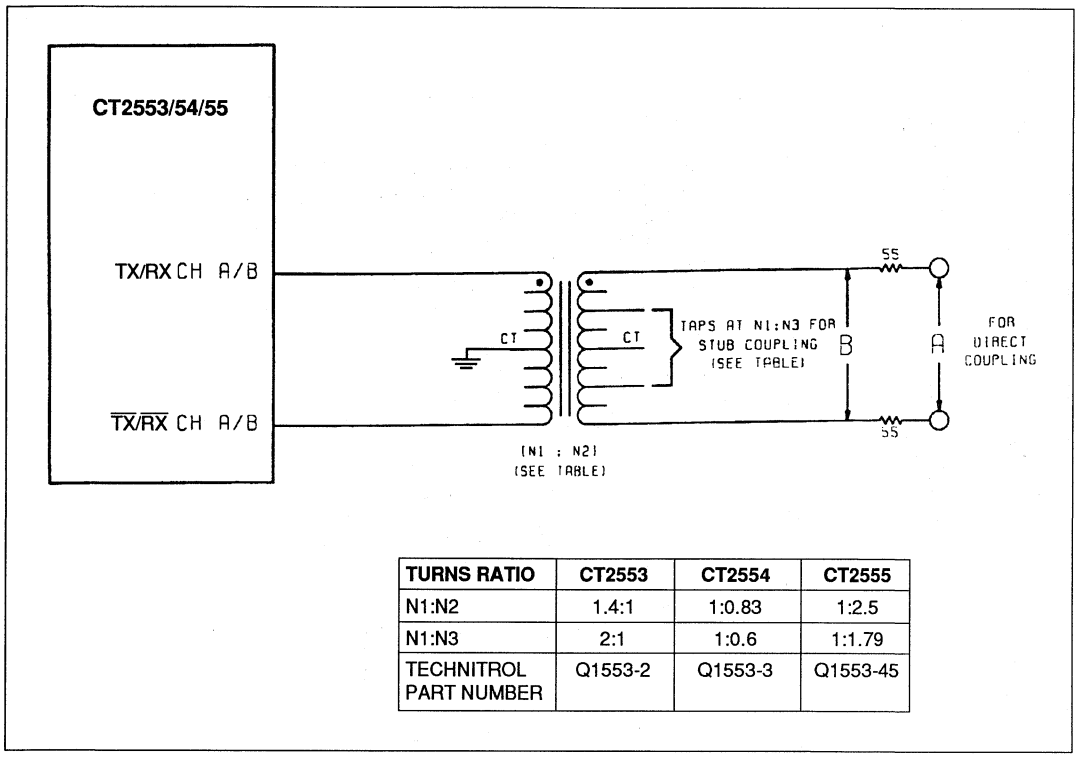
* Measured at point A, Figure 4.

Table 9: Receiver Characteristics - as measured in direct coupled configuration

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Differential O/P level †	Vo	28	32	35	Vp-p
Differential O/P noise	Vnoi	-	-	10	mVp-p
Differential O/P impedance @ 1MHz	Zoi	3K	-	-	ohms
O/P rise and fall times (10%-90%) *	Tr	100	160	300	nsec
O/P offset level *	Vos	-	±20	±90	mV

* Measured at point A, Figure 4.
† Measured at point B, Figure 4.

Table 10: Transmitter Characteristics - as measured in direct coupled configuration



TURNS RATIO	CT2553	CT2554	CT2555
N1:N2	1.4:1	1:0.83	1:2.5
N1:N3	2:1	1:0.6	1:1.79
TECHNITROL PART NUMBER	Q1553-2	Q1553-3	Q1553-45

Figure 4: Bus Interconnection Diagram

SIGNAL DESCRIPTIONS

MEMORY INTERFACE

PIN#	NAME	DIR	DESCRIPTION
60	A0	I/O	Internal/external RAM/Register address bit 0 (LSB)
22	A1	I/O	Internal/external RAM/Register address bit 1
61	A2	I/O	Internal/external RAM/Register address bit 2
23	A3	I/O	Internal/external RAM address bit 3
62	A4	I/O	Internal/external RAM address bit 4
24	A5	I/O	Internal/external RAM address bit 5
63	A6	I/O	Internal/external RAM address bit 6
25	A7	I/O	Internal/external RAM address bit 7
64	A8	I/O	Internal/external RAM address bit 8
26	A9	I/O	Internal/external RAM address bit 9
65	A10	I/O	Internal/external RAM address bit 10
27	A11	I/O	Internal/external RAM address bit 11
66	A12	I/O	Internal/external RAM address bit 12
28	A13	I/O	Internal/external RAM address bit 13
67	A14	I/O	Internal/external RAM address bit 14
29	A15	I/O	Internal/external RAM address bit 15 (MSB)
1	D0	I/O	Internal/external RAM/Register data bit 0 (LSB)
41	D1	I/O	Internal/external RAM/Register data bit 1
2	D2	I/O	Internal/external RAM/Register data bit 2
42	D3	I/O	Internal/external RAM/Register data bit 3
3	D4	I/O	Internal/external RAM/Register data bit 4
43	D5	I/O	Internal/external RAM/Register data bit 5
4	D6	I/O	Internal/external RAM/Register data bit 6
44	D7	I/O	Internal/external RAM/Register data bit 7
15	D8	I/O	Internal/external RAM/Register data bit 8
45	D9	I/O	Internal/external RAM/Register data bit9
6	D10	I/O	Internal/external RAM/Register data bit 10
46	D11	I/O	Internal/external RAM/Register data bit 11
7	D12	I/O	Internal/external RAM/Register data bit 12
47	D13	I/O	Internal/external RAM/Register data bit 13
8	D14	I/O	Internal/external RAM/Register data bit 14
48	D15	I/P	Internal/external RAM/Register data bit 15 (MSB)
30	$\overline{\text{RAMOE}}$	O/P	Internal/external RAM active low output enable
68	$\overline{\text{RAMWR}}$	O/P	Internal/external RAM active low write enable
31	$\overline{\text{RAMCSO}}$	O/P	Internal/external RAM active low chip select
69	$\overline{\text{RAMCSI}}$	I/P	Internal RAM active low chip select
33	$\overline{\text{REGSEL}}$	I/P	Logic 0 selects internal/external register transfer Logic 1 selects internal/external RAM transfer

HOST CPU INTERFACE

PIN#	NAME	DIR	DESCRIPTION
74	$\overline{\text{DEVSEL}}$	I/P	Active low device select input from host CPU which must be low during CT2553 memory/register accesses
34	$\overline{\text{STRBD}}$	I/P	Active low data strobe input used in conjunction with $\overline{\text{DEVSEL}}$, which must be low in order to initiate CT2553 memory/register accesses
36	RD/$\overline{\text{WR}}$	I/P	Input from the host CPU which defines the direction of data transfer in the current cycle
75	$\overline{\text{READY}}$	O/P	Active low indication that data has been received from, or is available to, the host CPU
73	$\overline{\text{IOEN}}$	O/P	Active low enable signal which may be used to enable the external buffers which are required on the host CPU data and address buses in order to isolate the device
72	$\overline{\text{INT}}$	O/P	Active low interrupt pulse signal to host CPU

EXTERNAL REGISTER INTERFACE

PIN#	NAME	DIR	DESCRIPTION
35	$\overline{\text{REGOE}}$	O/P	External register active low output
37	$\overline{\text{REGWR}}$	O/P	External register active low write enable
76	$\overline{\text{TAGEN}}$	O/P	External time tag register active low output enable

COMMAND/STATUS WORD INTERFACE

PIN#	NAME	DIR	DESCRIPTION
55	$\overline{\text{THISRT}}$	O/P	Active low pulse indicating that the latest Command/Status Word received by the device contained an RT address which matches that set on pins 10, 9, 50,49 & 11
70	$\overline{\text{INCMD}}$	O/P	Active low level which indicates that the device is performing a message sequence
13	SA/WC0	O/P	Latest valid command subaddress/mode code bit 0 (LSB)
15	SA/WC1	O/P	Latest valid command subaddress/mode code bit 1
52	SA/WC2	O/P	Latest valid command subaddress/mode code bit 2
54	SA/WC3	O/P	Latest valid command subaddress/mode code bit 3
53	SA/WC4	O/P	Latest valid command subaddress/mode code bit 4 (MSB)
17	$\overline{\text{SADET}}$	O/P	Active low level indication that pins 13,15, 52, 54, 53 contain a subaddress value
57	T/$\overline{\text{R}}$	O/P	Latest valid command transmit/receive bit
16	$\overline{\text{BCST}}$	O/P	Active low pulse indicating that the latest valid command contained the broadcast address
12	ILLCMD	I/P	Active low level input which can be used to illegalise 1553B commands when the device is operating in RT mode

REMOTE TERMINAL ADDRESS CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
10	RTAD0	UP	Remote Terminal Address bit 0 (LSB)
9	RTAD1	I/P	Remote Terminal Address bit 1
50	RTAD2	I/P	Remote Terminal Address bit 2
49	RTAD3	I/P	Remote Terminal Address bit 3
11	RTAD4	I/P	Remote Terminal Address bit 4 (MSB)
51	RTADP	I/P	Remote Terminal Address parity
56	$\overline{\text{PARERR}}$	O/P	Active low level indicating Remote Terminal Address parity error

RESET AND CLOCK

PIN#	NAME	DIR	DESCRIPTION
71	$\overline{\text{RESET}}$	I/P	Active low power-on reset input
32	CK16M	I/P	16MHz clock input

1553B DATA BUS CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
40	BUS0(+)	I/O	Positive threshoid exceeded on bus 0
78	BUS0(-)	I/O	Positive threshold exceeded on bus 0
20	BUS1(+)	I/O	Negative threshold exceeded on bus 1
59	BUS1(-)	I/O	Negative threshold exceeded on bus 1

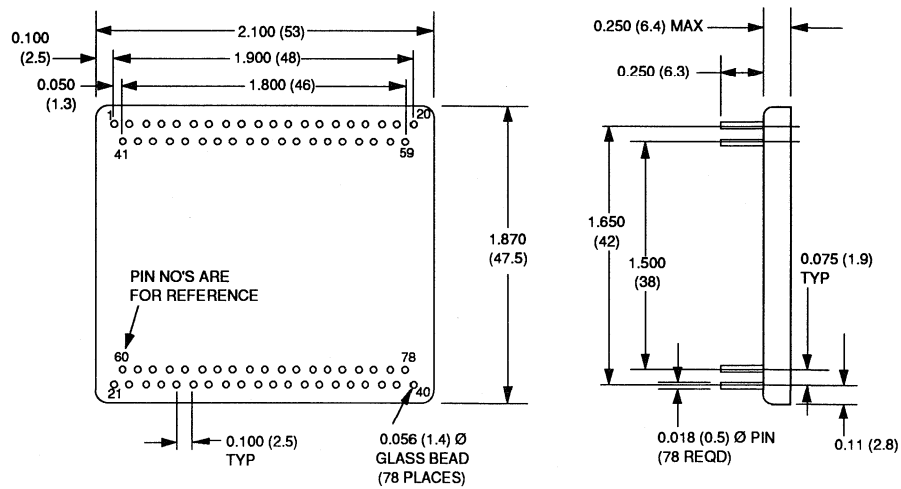
POWER SUPPLY CONNECTIONS

PIN#	NAME	DIR	DESCRIPTION
14	+5V	I/P	+5V Power supply input
77	+5V(0)	I/P	+5V Power supply input - channel 0
58	+5V(1)	I/P	+5V Power supply input - channel 1
38	GND(0)	I/P	Power supply return input - channel 0
19	GND(1)	I/P	Power supply return input - channel 1
39	-15V(0)	I/P	-15V Power supply input - channel 0
18	-15V(1)	I/P	-15V Power supply input - channel 1

PIN OUT

1 - DO	21 - GND		
2 - D2	22 - A1	41 - D1	60 - A0
3 - D4	23 - A3	42 - D3	61 - A2
4 - D6	24 - A5	43 - D5	62 - A4
5 - D8	25 - A7	44 - D7	63 - A6
6 - D10	26 - A9	45 - D9	64 - A8
7 - D12	27 - A11	46 - D11	65 - A10
8 - D14	28 - A13	47 - D13	66 - A12
9 - RTAD1	29 - A15	48 - D15	67 - A14
10 - RTAD0	30 - $\overline{\text{RAMOE}}$	49 - RTAD3	68 - $\overline{\text{RAMWR}}$
11 - RTAD4	31 - $\overline{\text{RAMCSO}}$	50 - RTAD2	69 - $\overline{\text{RAMCSI}}$
12 - $\overline{\text{ILLCMD}}$	32 - CK16M	51 - RTADP	70 - $\overline{\text{INCMD}}$
13 - SA/MCO	33 - $\overline{\text{REGSEL}}$	52 - SA/MC2	71 - $\overline{\text{RESET}}$
14 - +5V	34 - $\overline{\text{STRBD}}$	53 - SA/MC4	72 - $\overline{\text{INT}}$
15 - SA/MC1	35 - $\overline{\text{REGOE}}$	54 - SA/MC3	73 - $\overline{\text{IOEN}}$
16 - $\overline{\text{BCST}}$	36 - RD/$\overline{\text{WR}}$	55 - $\overline{\text{THISRT}}$	74 - $\overline{\text{DEVSEL}}$
17 - $\overline{\text{SADET}}$	37 - $\overline{\text{REGWR}}$	56 - $\overline{\text{PARERR}}$	75 - $\overline{\text{READY}}$
18 - 15v (1)	38 - GND (0)	57 - T/$\overline{\text{R}}$	76 - $\overline{\text{TAGEN}}$
19 - GND (1)	39 - -15V (0)	58 - + 5V (1)	77 - + 5V (0)
20 - BUS1 (+)	40 - BUS0 (+)	59 - BUS1 (-)	78 - BUS0 (-)

PACKAGE OUTLINE



Note: Dimensions are in inches (millimetres)

ORDERING INFORMATION:

CT2553: -15V/+5V SUPPLY
CT2554: -12V/+5V SUPPLY
CT2555: +5V SUPPLY

3033-1.3 November 1991

MCT83100 Series

MIL-STD-1553B STANAG 3838 REMOTE TERMINAL UNIT

(Supersedes H10401FUG all versions)

The MCT83100 series is a range of complete dual redundant MIL-STD-1553B (STANAG 3838) Remote Terminal Units with an easy to use processor interface. Each device comprises two low power transceivers, a monolithic Remote Terminal (RT) protocol device, a memory control device, and a 4K x 16 bit double buffered dual port RAM, all in a single co-fired ceramic package. Additionally four MSI devices buffer the Initialise Word and make available the 1553B Command Word.

The MCT83910 thru MCT83912 are identical to the MCT83100 series except that the four MSI devices are omitted. This makes available the internal highway (HD0-15) allowing STANAG 3910 Action and Status Words to be transferred. A number of control lines are also available to provide a means of interfacing to the internal highway.

FEATURES

- Single package device providing comprehensive remote terminal 1553B interface compatibility with most processing systems/devices
- Integral Transceivers
- Integral 4K x 16 Bit Fully Double Buffered Dual Port Static RAM Devices
- All MIL-STD-1553B Data Words are Memory Mapped, so providing a minimum of Software and Hardware overheads
- Separate Data Buffering for Broadcast Commands (in accordance with MIL-STD-1553B Notice 2)
- Contains full memory contention resolution and control
- Provides powerful built in test features initiated either by Host Subsystems or via the 1553B Data Highway
- Integral Illegal Command Monitoring
- Low Power Dissipation
- 90 Pin Quad In Line or Flat Pack Package 2.4 x 1.6 Inches (61 x 41mm)
- Can be configured to operate in either 16 Bit or 8 Bit Mode
- Operates over the full Military Temperature Range (-55°C to +125°C)

Device	Transceiver Voltages	RAM Options (k)
MCT83102	-15, +5	4
MCT83102-3	±15, +5	
MCT83103	-12, +5	4
MCT83103-3	±12, +5	
MCT83105	+5	4
MCT83910	-15, +5	4+3910 I/F
MCT83910-3	±15, +5	
MCT83911	-12, +5	4+3910 I/F
MCT83911-3	±12, +5	
MCT83912	+5	4+3910 I/F

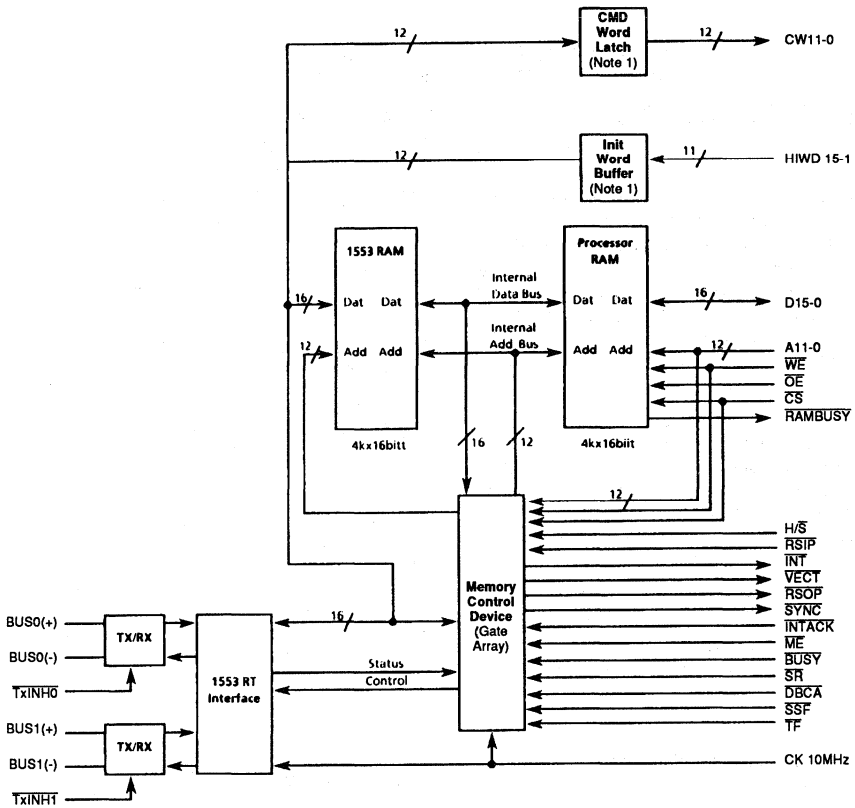
Notes:
1. Package size: 2.4"x1.6" (61mmx41mm)
2. RAM Access Time: 100ns
3. Refer to Customer Services for availability of MCT83102, 83103, 83910, 83911

Table 1: MCT83100 Series

GENERAL DESCRIPTION

Each of the MCT83100 series of devices provides an intelligent, fully double buffered interface between either a single or a dual redundant 1553B data bus and any 16-bit or 8-bit based CPU. The interface appears to a host CPU as a 4kx16-bit area of static RAM into which all 1553B transfers are memory mapped. A host CPU has access to the memory at all time. Only complete, valid messages will be presented to, or transmitted from the CPU.

All of the 1553B RT options are implemented by the MCT83100 series of devices. These along with a number of software and hardware programmable interface options provide a high degree of operational flexibility. A Message Error input is provided in order that any number of broadcast-T/R-subaddress-word count combinations may be declared illegal. The devices also allow a host CPU to make use of the 1553B reserved status bits and mode commands if required in specialist applications.



Notes:
1. See appendix A for details of MCT83910/1/2 operation.
2. Refer to factory for 2k RAM Versions.

Figure 1: MCT83102 Block Diagram

1. FUNCTION

Figure 1 is a block diagram of the MCT83102 (4k x 16-bit RAM version), the device can be seen to contain the following functions:-

1. Two 1553B transceivers.
2. A 1553B RT protocol device.
3. A 4k x 16-bit area of dual port RAM accessed by the host CPU referred to as the "Processor RAM".
4. A 4k x 16-bit area of dual port RAM accessed by the 1553B protocol device referred to as the "1553 RAM".
5. A gate array responsible for memory contention resolution and control.
6. Two output latches which contain the latest Command Word.
7. Two input buffers which buffer the devices Initialise Word.

Mil-Std-1553B Command and Data words are received by the transceivers and validated by the 1553 RT protocol device. The 1553 protocol device accesses the left hand side (LHS) of the "1553 RAM". The host CPU has access to the right hand side (RHS) of the "Processor RAM". The gate array performs data transfers between the RAMs.

After reception of a 1553 receive Command Word followed contiguously by receive data, the 1553 protcol device stores the data in the "1553 RAM". The data is memory mapped using the 1553 Command Word subaddress bits. Upon message validation the 1553 protocol device transmits a Status Word then instructs the gate array to transfer the data from the "1553 RAM" to the "Processor RAM". This transfer may be prevented by the host CPU writing the subaddress value of the data into location 405 (hex) - the Receive Access Control word (RACWd).

The 1553 protocol device will always store receive data in the "1553 RAM" irrespective of the RACWd contents. The gate array compares the RACWd value with the subaddress in the command word after message validation. If the RACWd value matches the subaddress then the "1553 RAM" to "Processor RAM" data transfers will be delayed until the RACWd contents are altered. If the RACWd value does not match the subaddress then the "1553 RAM" to "Processor RAM" data transfer takes place immediately.

In order to read a receive message, the host CPU merely writes the appropriate subaddress value of the data into the RACWd, then reads the data in ascending order, before clearing the RACWd to zero.

Transmit data is stored in the "Processor RAM" by the host CPU. Once the message is complete the host CPU instructs the gate array to transfer the message to the "1553 RAM". The transfer is initiated by the host CPU writing the expected transmit Command Word into either location 406 (hex) or location 407 (hex) - Transfer Control Words 0 and 1 (TCWd). When the 1553 protocol device decodes a transmit Command Word it transmits a Status Word followed by the required number of Data Words - which it reads from the "1553 RAM".

Upon completion of a "Processor RAM" to the "1553 RAM" data transfer the gate array clears the relevant TCWd. The host CPU must not write to a TCWd that has not been cleared. The "Processor RAM" to the "1553 RAM" data transfer may be delayed by up to 640µs if the 1553 protocol device is performing a transmit command using the same subaddress value as contained in the TCWd. Hence a second TCWd is provided.

In order to update a transmit message, the host CPU writes the transmit data into the "Processor RAM". When the message is complete the host CPU interrogates the TCWds in order to ascertain which is clear, before writing the expected transmit command word value into that TCWd.

It is intended that the host CPU views the 83100 interface merely as a block of RAM, hence all Command, Control, Status and Data Words are memory mapped within the 4k boundary. 4k RAM is provided in order that Data Words associated with broadcast commands may be stored independently of non-broadcast data. Figure 5 details the MCT83102 memory architecture.

A 12-bit latched Command Word output and a message error Status Word input are provided in order to allow Command Words to be illegalised with the minimum of external hardware. All 1553B defined illegal commands are automatically illegalised without the addition of external hardware. Four interrupt outputs and six 1553 Status Word inputs are provided should they be required. A further group of eleven inputs is also provided in order to allow the host CPU designer to hard-wire the Hybrid Initialise word.

2. SIGNAL DESCRIPTIONS

Pin	Name	Dir	Logic	Description
1	BUS1(+)	I/O	1553B	Positive threshold exceeded bus 1
2	BUS1(-)	I/O	1553B	Negative threshold exceeded bus 1
3	V_{EE}(1)	I/P	-	-15V/-12V supply to bus 1 transceiver (see note 3) (HIGH CURRENT)
4	V_{DD}(1)	I/P	-	+15V/+12V/+5V supply to bus 1 transceiver (see note 4) (HIGH CURRENT)
5	0V	I/P	-	0V return for all supplies
6	V_{CC}	I/P	-	+5V supply (see note 5)
7	TP1	O/P	-	Factory use only
8	TP2	O/P	-	Factory use only
9	$\overline{TXINHI}$	I/P	T2	Active low bus 1 transmitter inhibit (open circuit enables transmitter) (note 3)
10	H/$\overline{S}$	I/P	C2	Connecting this input to logic 0 will cause the HIWd to be defined by location 401 (hex) of the 1553B RAM. Leaving this input open circuit will cause the HIWd to be defined by the HI15-1 inputs.
11	10MHz	I/P	C3	10MHz clock input. Note: clock must have a mark/space ratio of 1:1±10%
12	$\overline{RSIP}$	I/P	C2	This input must be held to a logic 0 for 1.0µs after power up ie V_{CC} = 4.5V
13	$\overline{RSOP}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Reset RT mode command.
14	$\overline{VECT}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Transmit Vector Word mode command.
15	$\overline{SYNC}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Synchronise Without Data mode command and after reception of a valid Synchronise With Data mode command if bit 14 of the HCWd is set.
16	$\overline{INT}$	O/P	C1	Upon reception of a valid command (if the relevant HCWd bit is set) this output will go low until $\overline{INTACK}$ is taken to logic 0. If $\overline{INTACK}$ is connected directly to $\overline{INT}$ then $\overline{INT}$ will pulse low for nominally 300ns.
17	$\overline{INTACK}$	I/P	C2	Setting this input to a logic 0 will cause the $\overline{INT}$ output to return to a logic 1. Note: Minimum $\overline{INT}$ pulse width is nominally 300ns.
18	HI15	I/P	T2	RTAD4
19	HI14	I/P	T2	RTAD3
20	HI13	I/P	T2	RTAD2
21	HI12	I/P	T2	RTAD1
22	HI11	I/P	T2	RTAD0
23	HI10	I/P	T2	RTADPAR
24	HI9/8	I/P	2xT2	BCST
25	HI7	I/P	T2	$\overline{FLAGOP}$
26	HI3	I/P	T2	TM1
27	HI2	I/P	T2	TM0
28	HI1	I/P	T2	$\overline{ABR}$
				These inputs define the device's HIWd if the H/$\overline{S}$ input is open circuit or at logic 1. The HIWd is only loaded into the 1553 RT Interface device either on the low-to- high transition of the RTON bit in the HCWd or upon reception of a valid Reset RT mode command. The bit allocation of the HIWd is detailed in table 3
29	$\overline{RAMWEH}$	I/P	RA	Pulsing this input with $\overline{RAMCS}$ low will cause the most significant eight bits of the "Processor RAM" (D 15-8) to be written to. Note: The address will be defined by the A11-0 inputs.
30	$\overline{RAMWEL}$	I/P	RW	Pulsing this input low with $\overline{RAMCS}$ low will cause the least significant eight bits of the "Processor RAM" (D7-0) to be written to. Note: in 8 bit mode a pulse on this pin must precede a pulse on $\overline{RAMWEH}$.

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions

Pin	Name	Dir	Logic	Description
31	$\overline{\text{RAMOE}}$	I/P	RW	Setting this input low whilst $\overline{\text{RAMCS}}$ is low will allow the device's "Processor RAM" to be read.
32	$\overline{\text{RAMCS}}$	I/P	C2	Setting this input low will allow access to the "Processor RAM".
33	A11	I/P	RA	These inputs form the address bus of the "Processor RAM"
34	A10	I/P	RA	
35	A9	I/P	RA	
36	A8	I/P	RA	
37	A7	I/P	RA	
38	A6	I/P	RA	
39	A5	I/P	RA	
40	A4	I/P	RA	
41	A3	I/P	RA	
42	A2	I/P	RA	
43	A1	I/P	RA	
44	A0	I/P	RA	
45	0V	I/P	-	0V return for all supplies
46	CASE	I/P	-	Case connection
47	$\overline{\text{RAMBUSY}}$	O/P	RB	This output will go active low if both the host CPU and the gate array attempt to access the same location in the "Processor RAM". Note: The host CPU must not access the MCT83100 RAM whilst this output is active.
48	D15	I/O	RD	These 16 bi-directional lines form the data bus connections to the "Processor RAM".
49	D14	I/O	RD	
50	D13	I/O	RD	
51	D12	I/O	RD	
52	D11	I/O	RD	
53	D10	I/O	RD	
54	D9	I/O	RD	
55	D8	I/O	RD	
56	D7	I/O	RD	
57	D6	I/O	RD	
58	D5	I/O	RD	
59	D4	I/O	RD	
60	D3	I/O	RD	
61	D2	I/O	RD	
62	D1	I/O	RD	
63	D0	I/O	RD	

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions (continued)

Pin	Name	Dir	Logic	Description
64	CW11	O/P	T1	These 12 outputs hold the last valid Command Word received by the device. These lines are updated 2.5µs before the on-board 1553B Status Word latch is up dated prior to transmission. CW11 will be a logic 1 after reception of a broadcast command and a logic 0 after a non-broadcast command. Note: these outputs allow the host CPU to decode the Command Word and then set the 1553B Message Error bit by driving the $\overline{ME}$ input to logic 0, so illegalising the command .
65	CW10	O/P	T1	
66	CW9	O/P	T1	
67	CW8	O/P	T1	
68	CW7	O/P	T1	
69	CW6	O/P	T1	
70	CW5	O/P	T1	
71	CW4	O/P	T1	
72	CW3	O/P	T1	
73	CW2	O/P	T1	
74	CW1	O/P	T1	
75	CW0	O/P	T1	
76	$\overline{ME}$	I/P	C2	Setting this input to a logic 0 will cause the Message Error bit to be set in subsequent 1553B Status Word transmissions. Note: Data transfers will be prevented.
77	$\overline{SR}$	I/P	C2	Setting this input to a logic 0 will cause the Service Request bit to be set in subsequent 1553B Status Word transmissions
78	$\overline{BUSY}$	I/P	C2	Setting this input to a logic 0 will cause the Busy bit to be set in subsequent 1553B Status Word transmissions. Note: Data Transfers will be prevented.
79	$\overline{SSF}$	I/P	C2	Setting this input to a logic 0 will cause the Subsystem Flag bit to be set in subsequent 1553B Status Word transmissions.
80	$\overline{DBCA}$	I/P	C2	Setting this input to a logic 0 will cause the Dynamic Bus Control Accept bit to be set in response to Dynamic Bus Control mode commands.
81	$\overline{TF}$	I/P	C2	Setting this input to a logic 0 will cause the Terminal Flag bit to be set in subsequent 1553B Status Word transmissions.
82	$\overline{TXINH0}$	I/P	T2	Active low bus 0 transmitter inhibit. Open circuit enables transmitter) (Note 3).
83	TP4	O/P	-	Factory use only
84	TP3	O/P	-	Factory use only
85	V_{CC}	I/P	-	+5V supply (see note 5)
86	0V	I/P	-	0V return for all supplies
87	$V_{DD}(0)$	I/P	-	+15V/+12V/+5V supply to bus 0 transceiver. (See note 4) (HIGH CURRENT)
88	$V_{EE}(0)$	I/P	-	-15V/-12V supply to bus 0 transceiver. (See note 3) (HIGH CURRENT)
89	BUS0(-)	I/O	1553B	Negative threshold exceeded bus 0.
90	BUS0(+)	I/O	1553B	Positive threshold exceeded bus 0.

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions (continued)

3. RECOMMENDED OPERATING CONDITIONS

3.1 MCT83102, MCT83910 -15V Device

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VEE	-14.25	-15.0	-15.75	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IEE	-	1	3	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 25% duty cycle (Note 2 applies)	IEE25	-	41	45	mA
Supply current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 100% duty cycle (Note 2 applies)	IEE100	-	166	185	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	155	160	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range (case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.38	3.17	W
Power Dissipation at 100% duty cycle	P100	-	1.96	4.20	W

Notes:
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle.

Table 3: Recommended Operating Conditions - MCT83102, MCT83910

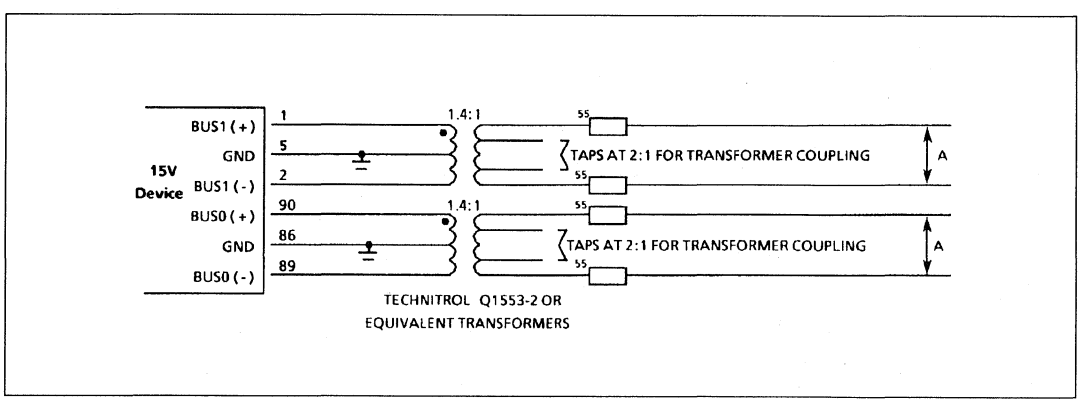


Figure 2: Bus Connections for 15V Devices

3.2 MCT83102-3, MCT83910-3 ±15V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VDD	+14.25	+15.0	+15.75	V
	VEE	-14.25	-15.0	-15.75	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IDD	-	30	44	mA
	IEE	-	50	70	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 25% duty cycle (Note 2 applies)	IDD25	-	70	100	mA
Supply current transmitting at 1MHz into 35Ω load at point A of Fig.2- 100% duty cycle (Note 2 applies)	IDD100	-	200	260	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	350	500	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range (case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	2.40	4.75	W
Power Dissipation at 25% duty cycle	P25	-	2.60	5.25	W
Power Dissipation at 100% duty cycle	P100	-	4.35	6.90	W

Notes:
1. I_{CC} and I_{EE} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 4: Recommended Operating Conditions - MCT83102-3, MCT83910-3

3.3 MCT83103, MCT83911 -12V Device

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VEE	-11.4	-12.0	-12.6	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie.less than 1% duty cycle (Note 1 applies)	IEE	-	1	3	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 25% duty cycle (Note 2 applies)	IEE25	-	64	68	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 100% duty cycle (Note 2 applies)	IEE100	-	231	254	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	230	250	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.56	3 23	W
Power Dissipation at 100% duty cycle	P100	-	2.24	4.6	W

Notes:
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 5: Recommended Operating Conditions - MCT83103, MCT83911

3.4 MCT83103-3, MCT83911-3 ±12V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VDD	+11.4	+12.0	+12.6	V
	VEE	-11.4	-12.0	-12.6	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IDD	-	30	44	mA
	IEE	-	50	70	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 25% duty cycle (Note 2 applies)	IDD25	-	85	120	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 100% duty cycle (Note 2 applies)	IDD100	-	240	315	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	350	500	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	2.15	4.40	W
Power Dissipation at 25% duty cycle	P25	-	2.40	4.90	W
Power Dissipation at100% duty cycle	P100	-	3.06	7.20	W

Notes:
1. I_{CC} and I_{EE} limits do not change with duty cycle or mode of operation
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 6: Recommended Operating Conditions - MCT83103-3, MCT83911-3

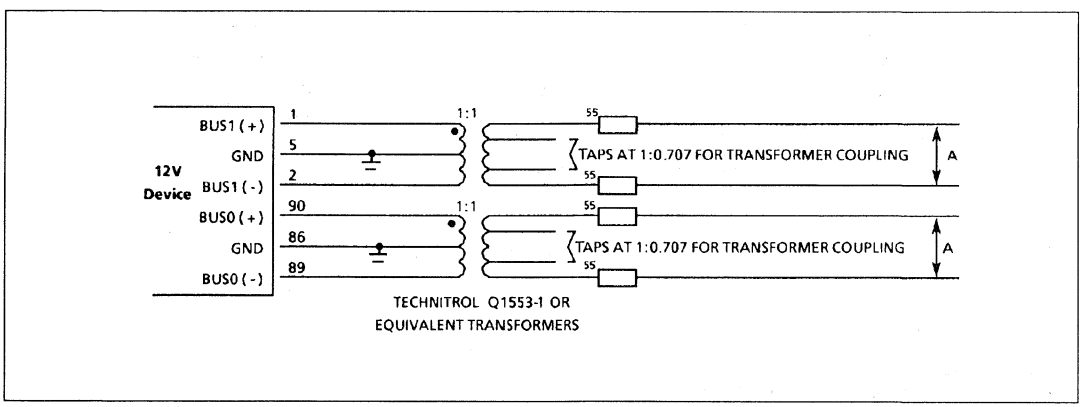


Figure 3: Bus Connections for 12V Devices

3.5 MCT83105, MCT83912 +5V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power supply voltages	VDD	4.5	5 0	5 5	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode(ie. less than 1% duty cycle (Note 1 applies)	IDD	-	100	150	mA
	ICC	-	137	390	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.4 - 25% duty cycle (Note 2 applies)	IDD25	-	230	293	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.4 - 100% duty cycle (Note2 applies)	IDD100	-	620	720	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	260	320	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1%duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.45	3.28	W
Power Dissipation at 100% duty cycle	P100	-	2.24	4.50	W

Notes
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 7: Recommended Operating Conditions - MCT83105, MCT83912

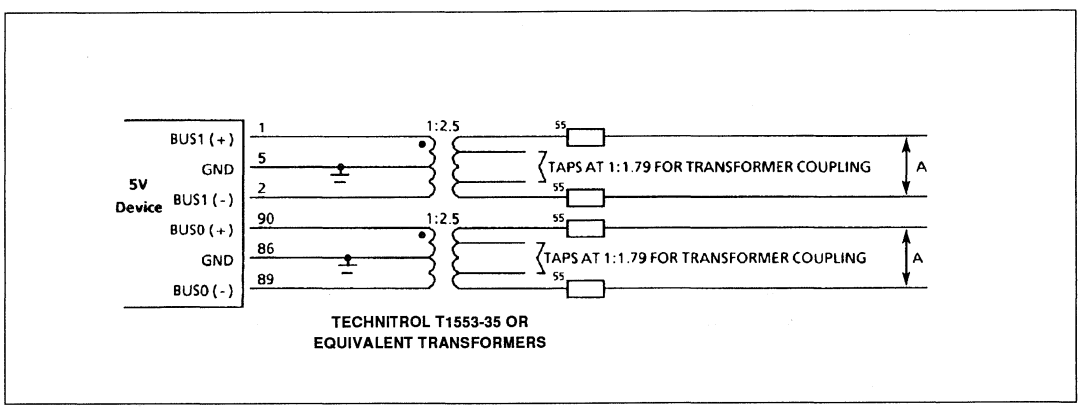


Figure 4: Bus Connections for +5V Device

GUIDELINES FOR USE

A) Decoupling

Decouple V_{DD} to ground close to the hybrid.
A parallel capacitor combination of a 100nF ceramic and a 10μF (or greater) tantalum is recommended.
Note: The peak transmission current drawn from V_{DD} is of the order of 650mA.

B) Board Layout

- Full PCB ground-planing is recommended.
- The connections between the Bus lines and the transformer should be balanced in terms of length, shape and area, and designed to:
  (i) Withstand peak transmission current at worst case operational duty cycle.
  (ii) Minimise added series inductance.
  (iii) Ensure that the input impedance of the hybrid with its associated transformer does not fall below the minimum requirements of MIL-STD-1553B.

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Device	Limits
Power Supply Voltage (V_{EE})	All except MCT83105 MCT83912	+0.3V to -18V
Power Supply Voltage (V_{CC})	All	-0.3V to +7V
Power Supply Voltage (V_{DD})	MCT83102-3 MCT83103-3 MCT83910-3 MCT83911-3	-0.3V to +18V
	MCT83105 MCT83912	-0.3V to +7V
Receiver Differential Input Pin 1 or Pin 2, and Pin 90 or Pin 89	All	±20V (40V p-p)
Receiver Input Voltage Pin 1 or Pin 2, and Pin 90 or Pin 89	All	±15V
Logic Input Voltages	All	-0.3V to +5.5V
Transmitter Output Peak Current Pin 1 to Pin 2, and Pin 90 to Pin 89	MCT83102 MCT83102-3 MCT83910 MCT83910-3	200mA
	MCT83103 MCT83103-3 MCT83911 MCT83911-3	300mA
	MCT83105 MCT83912	800mA
Transmission Duty Cycle at T_{CASE} = 125°C	All	100%
Operating Case Temperature Range (T_{OP})	All	-55°C to +125°C
Storage Temperature Range (T_{ST})	All	-65°C to +150°C

Table 8: Absolute Maximum Ratings

5. ELECTRICAL CHARACTERISTICS

Note: All max/min values are for worst case operating conditions, where appropriate. at -55°C to +125°C

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage(IOH=-1μA)	4.0	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.4	V

Table 9a: Output Type - C1

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage(IOH= -20μA)	4.0	-	-	V
VOL	Output Low Level Voltage(IOL = 4mA)	-	-	0.4	V

Table 9b: Output Type - T1

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage (IOH = -4mA)	2.4	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.5	V

Table 9c:0utput Type - RB

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage (IOH = -4mA)	2.4	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.5	V
VIH	Input High Level Voltage	2.2	-	-	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	30.0	μA
ILO	Output Leakage Current	-	-	30.0	μA

Table 9d: Input/Output - *RD*

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
IIH	Input High Level Current	-	-	-20	μA
IIL	Input Low Level Current	-	-	200	μA

Table 9e: Input Type - C2 (CMOS I/P with 50kΩ pull up)

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
IIH	Input High Level Current	-	-	100	μA
IIL	Input Low Level Current	-	-	1.5	mA

Table 9f: Input Type - T2 (CTTL I/P with 10KΩ)

Label	Description	min	Typ	max	unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	20	µA

Table 9g: Input Type - C3

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	60	µA

Table 9h: Input Type - RA

Label	Description	min	Typ	max	unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	40	µA

Table 9i: Input Type - RW

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Differential input impedance DC to 1 MHz (Transmitter Inhibited)		Zin	2K	-	-	Ω
Input differential voltage range		Vidr	±20	-	-	Vpeak
Input common mode voltage range up to 2MHz (line to ground)		Vicr	±10	-	-	Vpeak
Common mode rejection ratio		CMRR	40	-	-	dB
Threshold characteristics - sinewave at 1MHz		Vth1	0.75	1.0	1.2	Vp-p
Filter characteristics	2MHz	Vth2	1.5	-	8.0	Vp-p
	3MHz	Vth3	5	-	-	Vp-p
Differential output noise		Vnoi	-	-	10	mVp-p
Differential output level (e.g. at point A of Fig.2)		Vo	6	-	9	Vp-p
Rise and fall times (10-90%)		Tr	100	160	300	ns
Output Offset at 2.5µs after mid-bit crossing of the parity bit of the last word of a 660µs message (e.g. at point A of Fig.2)		Vos	-	±20	±75	mVpk

Table 9j: Transceiver Characteristics - For Direct Coupled Operation

6. MEMORY ARCHITECTURE

The memory can be divided into eight distinct areas:-

1. Command Word Stack.
2. Receive Data Buffer.
3. Receive Mode Data Buffer.
4. Control and Status Area.
5. Transmit Data Buffers.
6. Transmit Mode Data Buffers.
7. Broadcast Receive Data Buffer.
8. Broadcast Mode Receive Data Buffer.

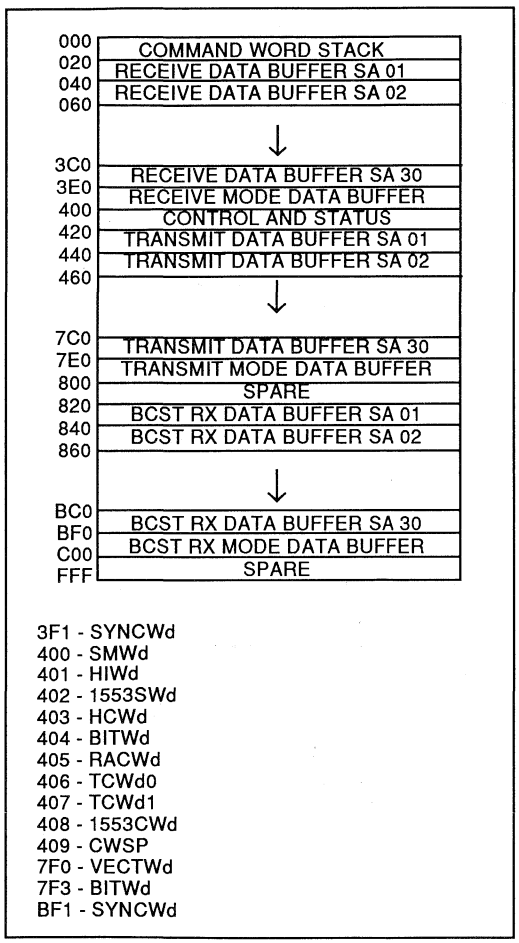


Figure 5: Memory Architecture

6.1 Command Word Stack

Locations 000 - 01F(hex) form the 32 word Command Word Stack. The device will store every valid, legal, logical command (except Transmit Status Word and Transmit Last Command Word mode commands) received in this circular stack. The bit allocation of the words on the Command Word Stack is listed on Table 10.

Bit	Name	Description
0	WC0	Word Count bit 0
1	WC1	Word Count bit 1
2	WC2	Word Count bit 2
3	WC3	Word Count bit 3
4	WC4	Word Count bit 4
5	SA0	Subaddress 0
6	SA1	Subaddress 1
7	SA2	Subaddress 2
8	SA3	Subaddress 3
9	SA4	Subaddress 4
10	T/$\overline{R}$	Transmit/Receive bit
11	BCST	Broadcast Command Detected - Logic 1 indicates reception of a Broadcast command
12	ZERO	Logic 0
13	ZERO	Logic 0
14	ZERO	Logic 0
15	NEWCMD	New Stack Command Word - This bit may be cleared by the host CPU after servicing the command

Table 10: Stack Command Word

6.2 Receive Data Buffers

Locations 020 - 3DF (hex) form the 30 Receive Data Buffers. Each buffer consists of 32 sixteen bit words and is allocated to each of the receive subaddress values excluding 00 and 1F (hex). Upon validation of a non-mode receive command and message the device will store the Data Words in the Receive Data Buffer indicated by the subaddress bits in the Command Word. The host CPU is able to delay this storing process by writing the appropriate subaddress value into the Receive Access Control Word (RACWd) in the Control and Status Area.

6.3 Receive Mode Data Buffer

Locations 3E0 - 3FF (hex) form the Receive Mode Data Buffer. This buffer is used to store the Data Words associated with receive mode commands irrespective of the subaddress bits being set to 00 or 1F (hex) e.g. Location 3F1 (hex) will contain the Data Word associated with a Synchronise with Data Word mode command.

6.4 Transmit Data Buffers

Locations 420-7DF (hex) form the Transmit Data Buffers. Each of these 30 buffers contains 32 sixteen bit words. As in the Receive Data Buffers each buffer is allocated a subaddress value. After the host CPU writes to either of the Transfer Control Words (TCWds) the gate array will transfer the indicated number of data words from the appropriate Transmit Data Buffer in the "Processor RAM" to the "1553 RAM". Upon reception of a non-mode transmit command the device will transmit the Data Words stored in the buffer indicated by the Command Word subaddress value.

6.5 Transmit Mode Data Buffers

Locations 7E0-7FF (hex) form the Transmit Mode Data Buffers. This buffer is used to store the Data Words associated with Transmit Mode Commands eg: Location 7F0 (hex) contains the 1553B Vector Word Location 7F3 (hex) contains the BITWd set up by the host CPU if bit 1 of the HIWd is set.

Note: Use of a TCWd is required to transfer these words from the "Processor RAM" to the "1553 RAM".

6.6 Broadcast Receive Data Buffer

Locations 820-BFF (hex) form the Broadcast Receive Data Buffers. These data buffers are used to store the Data Words associated with broadcast receive commands. As in the Receive Data Buffers each buffer is allocated a subaddress value.

6.7 Broadcast Receive Mode Data Buffer

Locations BE0-BFF (hex) form the Broadcast Receive Mode Data Buffers. This buffer is used to store the Data Words associated with broadcast mode receive commands irrespective of the subaddress bits being set to 00 or 1F (hex) eg: Location BF1 (hex) will contain the Data Word associated with a broadcast Synchronise with Data Word mode command.

6.8 Control and Status Area

Locations 400 - 41F form the Control and Status area. This area consists of ten words associated with the host CPU's monitoring and control of the device's operation.

6.8.1 Status Modifier Word

The Status Modifier Word (SMWd) is located at address 400 (hex), it allows the host CPU a high degree of control over the 1553B Status Word bits. In order to alter the state of the 1553B Status Word this word must be set to the appropriate, value then 0400 (hex) must be written into either of the Transfer Control Words. The bit allocation of the Status Modifier Word is listed in Table 11.

The 1553B Status Word Bits are set as a result of a logical 'OR' of the Status Modifier Word bits and the hardware status inputs (pins 76, 77, 78, 79, 80, 81).

In order to set a 1553B Status Word bit (eg Service Request) either set pin 77 to logic zero or write BFFF (hex) into address 400 (hex) then write 0400 (hex) into either of the Transfer Control Words.

Bit	Name	Description
0	Not Used	Set to one
1	Not Used	Set to one
2	Not Used	Set to one
3	$\overline{\text{ALLOW}}$	Allows reserved mode commands to be declared legal.
4	$\overline{\text{SETINST}}$	Sets the Instrumentation bit of the 1553B Status Word
5	$\overline{\text{SETRES5}}$	Sets bit 5 ot the 1553B Status Word
6	$\overline{\text{SETRES6}}$	Sets bit 6 ot the 1553B Status Word
7	$\overline{\text{SETRES7}}$	Sets bit 7 ot the 1553B Status Word
8	$\overline{\text{SETDBCA}}$	Sets the Dynamic Bus Control Accept bit in the 1553B Status Word transmitted in response to Dynamic Bus Control mode command
9	$\overline{\text{INHTF}}$	Inhibits the Terminal Flag bit in the 1553B Status Word from being set.
10	$\overline{\text{INHSSF}}$	Inhibits the Subsystem Flag bit in the 1553B Status Word from being set.
11	$\overline{\text{SETTF}}$	Sets the Terminal Flag bit in the 1553B Status Word
12	$\overline{\text{SETSSF}}$	Sets the Subsystem Flag bit in the 1553B Staus Word
13	$\overline{\text{SETBUSY}}$	Sets the Busy bit in the 1553B Status Word
14	$\overline{\text{SETSERV}}$	Sets the Service Request bit in the 1553B Status Word
15	$\overline{\text{SETME}}$	Sets the Message Error bit in the 1553B Staus Word

Note: All of the SMWd bits are active low.

Table 11: Status Modifier Word

6.8.2 Hybrid Initialise Word

The Hybrid Initialise Word (HIWd) is located at address 401 (hex), it allows the host CPU to configure the device for a particular application. An option to make this word 'hard-wired' is selectable by leaving the H/$\overline{S}$ input open circuit. In order to alter the state of the device Initialise Word the following sequence must be performed: -

1. Set RTON bit in Hybrid Control Word to zero
2. Write 0403 into address 406/407
3. Set Hybrid Initialise Word to appropriate value
4. Write 0401 into address 406/407
5. Set RTON bit in Hybrid Control Word to one
6. Write 0403 into address 406/407

Notes:

1. All addresses and data in hex.
2. If H/$\overline{S}$ input is open circuit then 4. can be omitted.
3. It is recommended that H/$\overline{S}$ be left open circuit and only the 'hard-wired' HIWd be used.
4. The bit allocation of the Hybrid Initialise Word is listed in Table 12.

Bit	Name	Description
0	Logic One	Set to one
1	$\overline{ABR}$	When low selects contents of 7F3 (hex) as Data Word Associated with Transmit Bit Word mode commands
2	$\overline{TM0}$	Timeout multiplier bit 0 (see note 1)
3	$\overline{TM1}$	Timeout multiplier bit 1 (see note 1)
4	Logic One	Set to one
5	Logic One	Set to one
6	Logic One	Set to one
7	$\overline{FLAGOP}$	Subsystem and Terminal Flag setting option (see note 2)
8	BCSTEN0	When high enables the broadcast address on bus 0
9	BCSTEN1	When high enables the broadcast address on bus 1
10	RTADPAR	Remote Terminal address parity bit (see note 3)
11	RTAD0	Remote Terminal address bit 0
12	RTAD1	Remote Terminal address bit 1
13	RTAD2	Remote Terminal address bit 2
14	RTAD3	Remote Terminal address bit 3
15	RTAD4	Remote Terminal address bit 4

Notes:

1.

$\overline{TM1}$	$\overline{TM0}$	No Response Timeout (μs)
1	1	14
1	0	31
0	1	47
0	0	64

2. $\overline{FLAGOP}$ =1 if the TF or SSF bit is set, it will remain set until some positive action is taken to clear the setting condition, ie, mode command to reset or local resetting.

   $\overline{FLAGOP}$=0 if the TF or SSF bit is set, it will remain set until one status word has been transmitted with the bit set. The TF or SSF will then reset unless the fault condition is still present (ie, $\overline{SETTF}$ or $\overline{SETSSF}$ in the SMWd are still active or pins 79 or 81 still at logic 0).

3. RTADPAR. This pin must be set to a state such that bits 10-15 inclusive have an odd number of bits set to logic 1, ie, an odd parity.

Table 12: Hybrid Initialise Word

6.8.3 1553B Status Word

Location 402 (hex) contains a copy of the 1553B Status Word associated with the last Command Word received by the device.

Bit	Name		Description
0	TERMINALFLAG	Set by one of the following	Driving pin 81 to logic 0
			SMWd bit 9 high and SMWd bit 11 low
			1553 Protocol device(see note 1)
		Reset by one of the following	Status word transmission if HIWd bit 7 low and Driving pin 81 to logic 1
			Status word transmission if HIWd bit 7 low and SMWd bit 11 high
			Reset RT mode command and Driving pin 81 to logic 1
			Reset RT mode command and SMWd bit 11 high
			HCWd bit 0 low
1	Dynamic Bus Control Accept	Set by one of the following	Driving pin 80 to logic 0 and Reception of a valid DBCA mode command
			SMWd bit 8 low and Reception of a valid DBC A mode command
		Reset by one of the following	Driving pin 80 to logic 1 and Reception of any valid command except mode commands 02 or 12 (hex).
			SMWd bit 8 high and Reception of any valid command except mode commands 02 or 12 (hex).
			Reception of any valid command except mode commands 00 or 02 or 12 (hex)
			HCWd bit 0 low
2	Subsystem Flag	Set by one of the following	Driving pin 79 to logic 0
			SMWd bit 9 high and SMWd bit 11 low
		Reset by one of the following	Status word transmission if HIWd bit 7 low and Driving pin 79 to logic 1
			Status word transmission if HIWd bit 7 low and SMWd bit 12 high
			Reset RT mode command and Driving pin 79 to logic 1
			Reset RT mode command and SMWd bit 12 high
			HCWd bit 0 low
3	BUSY	Set by one of the following	Driving pin 78 to logic 0 SMWd bit 13 low
		Reset by of the following	Driving pin 78 to logic 1 SMWd bit 13 high HCWd bit 0 low
4	BROADCAST COMMAND REC'VD	Set by	1553 Protocol device (see note 2)
		Reset by	Reception of any valid command except mode commands 02 or 12 (hex)
5	RESERVED	Set by	SMWd bit 5 low
		Reset by	SMWd bit 5 high
		of the following	HCWd bit 0 low
6	RESERVED	Set by	SMWd bit 6 low
		Reset by	SMWd bit 6 high
		of the following	HCWd bit 0 low
7	RESERVED	Set by	SMWd bit 7 low
		Reset by one	SMWd bit 7 high
		of the following	HCWd bit 0 low

Table 13: 1553B Status Word

Bit	Name	Description	
8	SERVICE REQUEST	Set by one of the following	Driving pin 77 to logic 0
			SMWd bit 14 low
		Reset by one of the following	Driving pin 77 to logic 1
			SMWd bit 14 high
			HCWd bit 0 low
9	INSTRUMENTATION	Set by	SMWd bit 4 low
		Reset by one of the following	SMWd bit 4 high
			HCWd bit 0 low
10	MESSAGE ERROR	Set by one of the following	Driving pin 76 to logic 0
			SMWd bit 15 low
			1553 Protocol device (see note 3)
		Reset by one of the following	Driving pin 76 to logic 1 and Reception of any valid command except mode commands 02 or 12 (hex).
			SMWd bit 15 high and Reception of any valid command except mode commands 02 or 12 (hex).
			HCWd bit 0 low
11-15	REMOTE TERMINAL ADDRESS BITS 0 - 4	These bits will be set to the RT Address value after reception of the first valid command after a low to high transition on HCWd bit 0	

Notes:

1: The Terminal Flag bit in the 83100 1553B Status Word is set by the 1553 protocol device under the following conditions:-
- i. If the 83100 fails to receive and validate a 1553B word that has transmitted: BIT Word bit 2 will also be set.
- ii. If the 83100 detects a failure in either of its transmission timeout circuits as a result of performing an Initialise Self Test mode command.
- iii. If either of the 83100 transmission timeout circuits goes active as a result of the device attempting to transmit for more than 800 microseconds.

2: The Broadcast Command Received bit in the 83100 1553B Status Word is set by 1553 protocol device upon reception of a valid Command Word that contains a RT Address of 1F (hex) under the following conditions:-
- i. Pin 14 was logic 0 and pin 10 was open-circuit at the time of the last low to high transition on HCWd bit 0.
- ii. HIWd bits 8 and 9 were low and pin 10 was logic 0 at the time of the last low to high transition on HCW bit 0.

3: The message error bit in the 83100 1553B Status Word is set by the 1553 protocol device if any of the following conditions occur on reception of a valid command word.
- i. Too few valid Data Words received after reception of a receive command: Status Word not transmitted and BITWd bit 5 is set.
- ii. An invalid data sync received during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 set.
- iii. An incorrect parity bit detected during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 is set.
- iv. A contiguity error detected during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 set.
- v. Too many Data Words received after reception of a receive command: Status Word not transmitted and BITWd bit 6 set.
- vi. Any word received after reception of a transmit command: Status Word not transmitted and BITWd bit 6 set.
- vii. Detection of an invalid RT-RT message format: Status Word not transmitted and either BITWd bit 5 or 6 set
- viii. Command Word decoded as illegal: Status Word transmitted and BITWd bit 4 is set.
- ix. Command Word decoded as illogical - eg broadcast transmit data command: Status Word not transmitted and BITWd bit 3 set.

Table 13: 1553B Status Word (continued)

6.8.4 Hybrid Control Word

The Hybrid Control Word (HCWd) is located at address 403 (hex). This word allows the processor further control over the operation of the device in areas such as interrupt generation and self test. In order to alter the state of the Hybrid Control Word location 403 (hex) must be updated with the appropriate value then 403 (hex) written into either of the Transfer Control Word locations. This word powers up in the all zero state. The bit allocation of the Hybrid Control Word is listed in Table 14.

Bit	Name	Description
0	RTON	When reset to zero this bit inhibits operation of the 1553B RT Interface device. The hybrid will still be capable of performing subsystem initiated self test as well as updating 1553B Transmit data buffers. This bit must be set to one in order to allow the hybrid to decode and respond to 1553B commands
1	WRAPENTX	Enables the device's subsystem initiated 'wrap around' self test feature
2	WRAPENRX	Enables the device's 1553B initiated 'wrap around' self test feature
3	INTENBIT	Enables the device's interrupt output after completion of either 'wrap around' self test
4	INTENRX	Enables device's interrupt output after completion of receive commands
5	INTENTX	Enables device's interrupt output after completion of transmit commands
6	INTENDBCA	Enables device's interrupt output after reception of Dynamic Bus Control mode commands
7	INTENSWO	Enables device's interrupt output after reception of Synchronise without Data Word mode commands
8	INTENST	Enables device's interrupt output after reception of Initiate Self Test mode commands
9	INTENRST	Enables device's interrupt output after reception of Reset Remote Terminal mode commands
10	INTENVW	Enables device's interrupt output after reception of Transmit Vector Word mode commands
11	INTENSWI	Enables device's interrupt output after reception of Synchronise with Data Word mode commands
12	INTENTBW	Enables device's interrupt output after reception of Transmit BIT Word mode command if bit 1 of the HIWd is set
13	INTENRSV	Enables device's interrupt output after reception of reserved mode commands
14	SYNCWIEN	Enables the device's SYNC output to go active after reception of Synchronise with Data Word mode commands
15	ZERO	Logic Zero

Table 14: Hybrid Control Word

6.8.5 Hybrid Built in Test Word

Location 404 (hex) will contain a copy of the current 1553 Interface device Built in Test Word (BITWd) which will be transmitted in response to a Transmit BIT Word mode command. This word is updated after every valid Command Word is received by the device, If bit 1 of HIWd is set then the BIT word contents will be taken from RAM location 7F3 (hex), the bit allocation is then defined by the host CPU, otherwise the bit allocation is as listed in Table 15. In either case location 404 (hex) will contain the 1553 Interface device BITWd.

Bit	Name	Description
0*	TIMEOUT	Transmitter timeout
1*	HSF	SS Handshake Failure
2	LTF	Loop test fail ie device detects error in its own transmission
3	TRW	T/R Wrong in mode command
4	IM	Illegal mode command
5	WCL	Word count low
6	WCH	Word count high
7	BTD	Broadcast transmit data
8*	SHUT0	Bus 0 is shutdown
9*	SHUT1	Bus 1 is shutdown
10*	SSFINH	Subsystem flag inhibited by the subsystem
11*	TFINF	Terminal flag inhibited by the subsystem
12	TIME0	Transmitter timeout on bus 0
13	TIME1	Transmitter timeout on bus 1
14*	BCSTINH0	Broadcast recognition inhibited (bus 0)
15*	BCSTINH1	Broadcast recognition inhibited (bus 1)

* These bits will continue to be set until appropriate action is taken to clear them ie Reset RT mode command or clear RTON bit in HCWd.

Table 15: Hybrid Built in Test Word

6.8.6 Receive Access Control Word

The Receive Access Control Word (RACWd) is located at address 405 (hex), By setting the bits of this word to a subaddress value, the host CPU is able to prevent the device from updating the Receive Data Buffer associated with that subaddress value. This word will be set to zero on power up, The bit allocation of this word is listed in Table 16.

Bit	Name	Description
0	Zero	Logic Zero
1	Zero	Logic Zero
2	Zero	Logic Zero
3	Zero	Logic Zero
4	Zero	Logic Zero
5	SA0	Subaddress bit 0
6	SA1	Subaddress bit 1
7	SA2	Subaddress bit 2
8	SA3	Subaddress bit 3
9	SA4	Subaddress bit 4
10	Zero	Logic Zero
11	BCST	Broadcast Data Buffer bit (Logic1 indicates broadcast area)
12	Zero	Logic Zero
13	Zero	Logic Zero
14	Zero	Logic Zero
15	Zero	Logic Zero

Note: No Transfer Control Word is required for the RACWd

Table 16: Receive Access Control Word

6.8.7 Transfer Control Words

The Transfer Control Words (TCWd0 and TCWd1) are located at address 406 (hex) 407 (hex) respectively. These words are used by the host CPU to instruct the gate array to transfer words stored in the 'Processor RAM' to the '1553B RAM'. The bit allocation of these words is listed in Table 17. These words can be used to transfer the following:-

1. Transmit data words: by outputing a TCWd containing the base address of a Transmit Data Buffer and the number of words it wishes transferred ie, T/R, Subaddress and Word Count of expected transmit command, the host CPU can instruct the gate array to update a Transmit Data Buffer.

Note: A Word Count of 00 will ensure the entire contents of the buffer are transmitted.

2. Miscellaneous Words: by writing a TCWd containing a subaddress value of either 00 or 1F (hex) and a T/R bit of one, the host CPU can instruct the on-chip controller to update the single word whose address is contained in the TCWd, eg:

TCWd = 0400 SMWd transferred

TCWd = 0401 HlWd transferred

TCWd = 0403 HCWd transferred

TCWd = 07F0 1553B Vector Word transferred

The host CPU must ensure that a TCWd is clear before writing to it. The gate array will clear the TCWd upon completion of the transfer and upon power up.

Bit	Name	Description
0	WC0	Word Count bit 0
1	WC1	Word Count bit 1
2	WC2	Word Count bit 2
3	WC3	Word Count bit 3
4	WC4	Word Count bit 4
5	SA0	Subaddress bit 0
6	SA1	Subaddress bit 1
7	SA2	Subaddress bit 2
8	SA3	Subaddress bit 3
9	SA4	Subaddress bit 4
10	T/$\overline{R}$	Transmit/Receive bit
11*	Zero	Remote Terminal Address bit 0
12*	Zero	Remote Terminal Address bit 1
13*	Zero	Remote Terminal Address bit 2
14*	Zero	Remote Terminal Address bit 3
15*	Zero	Remote Terminal Address bit 4

*Note: TCWd bits 11-15 are only used during self test.

Table 17: Transfer Control Word

6.8.8 Last 1553B Command Word

Location 408 (hex) contains the latest valid 1553B Command Word (with the exception of Transmit Last Command Word mode command) received by the device.

6.8.9 Command Word Stack Pointer

Location 409 (hex) contains the Command Word Stack Pointer (CWSP). This word will be the stack address of the latest Command Word Stack location to be updated by the device. This word will be reset to zero on power up.

7. POWER UP

On power up the MCT83100 requires the $\overline{RSIP}$ input be held low for at least 1.0µs after VCC reaches 4.5V. Upon this input going to a logic 1 the device will perform a reset routine which will result in:-

1. Command Word Stack Locations 000-01F set to 0000
2. RACWd set to 0000
3. TCWd0 and TCWd1 set to 0000
4. CWSP set to 0000

The reset routine results in reseting all of the 'status' information and disabling the devices from decoding and responding to 1553B Command Words. It is the responsibility of the host CPU to set up the following before setting the RTON bit in the HCWd:-

1. SMWd - if applicable - powers up random in the memory but in the gate array powers up to FFFF (hex)
2. HIWd - if applicable
3. Hybrid BITWd - if applicable
4. Transmit Data Buffers
5. Transmit Mode Data Buffers
6. HCWd - ie at minimum set RTON bit

Note: All of the above need to be transferred out of the "Processor RAM" using the Transfer Control Words.

8. INTERRUPTS

There are four interrupt signals that can be used by the host CPU as prompts regarding messages that have been received. Use of these signals is optional.

1. $\overline{SYNC}$ - This output will pulse low upon reception of valid Synchronise without Data mode commands unconditionally and valid Synchronise with Data mode commands if bit 14 of the HCWd has been set previously.
2. $\overline{RSOP}$ - This output will pulse low upon reception of valid Reset RT mode commands.
3. $\overline{VECT}$ - This output will pulse low upon reception of valid Transmit Vector Word mode commands.
4. $\overline{INT}$ - After reception of a valid command - if the relevant HCWd bit has been set previously - this output will go low until the input $\overline{INTACK}$ is taken low in response. If $\overline{INTACK}$ is connected to $\overline{INT}$ then this input will pulse low for nominally 300ns.

9. BUILT IN TEST

The device has four Built in Test (BIT) features:-

1. Upon reception of a valid Initiate Self Test mode command the device will test the 1553B transmission timeout circuit associated with the data bus on which the command was received. This test will take nominally 27.5µs after the Status Word is transmitted.
2. The device will monitor and validate every word it transmits on each of the 1553B data buses. If the device detects an error it will set the Terminal Flag bit and bit 2 in the BITWd
3. Whenever bit 1 of HCWd is set, the device will, upon reception of a new TCWd0 value:-
   a. Transfer the number of Data Words from theTransmit Data Buffer indicated by the TCWd in the "Processor RAM" to the equivalent Receive Data Buffer i n the "1553B RAM".
   b. Transfer the Data Words from the Receive Data Buffer in the "1553B RAM" to the equivalent Receive Data Buffer in the "Processor RAM".
   c. Write the TCWd into the next Command Word Stack location and increment the CWSP.
   d. Take the $\overline{INT}$ line active low if bit 4 of the HCWd is set.

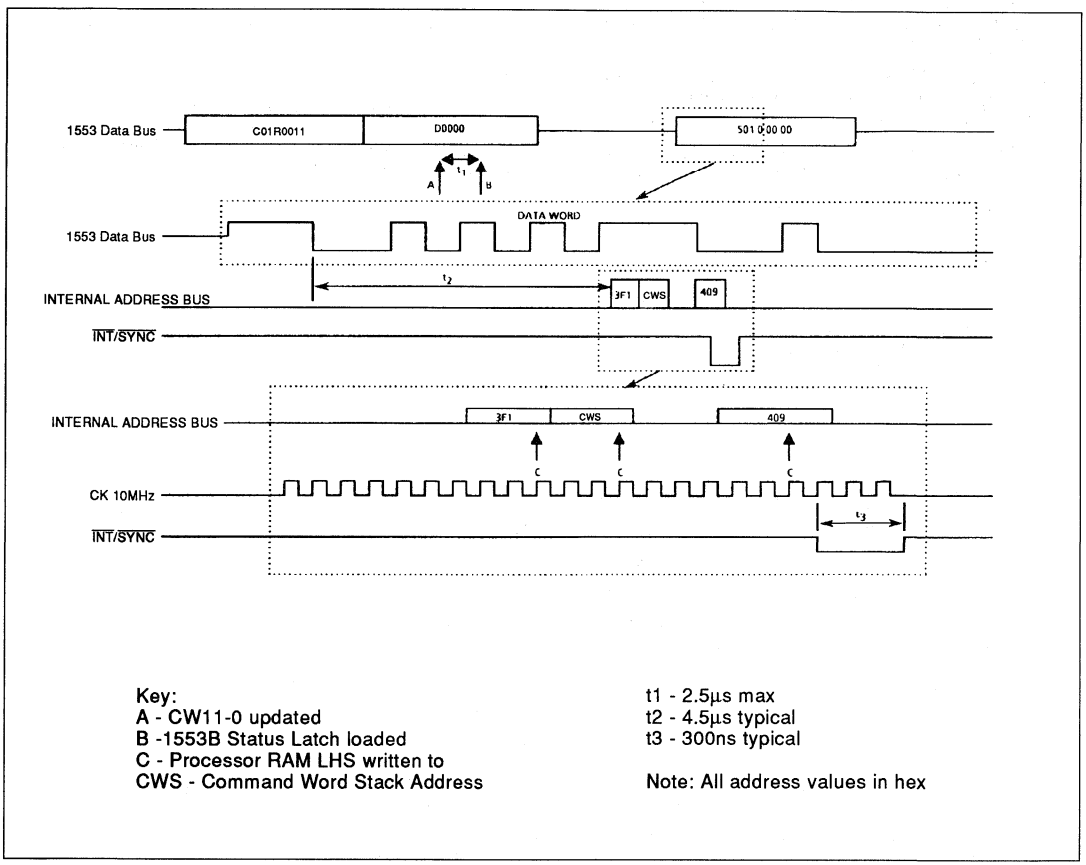
   It is the responsibility of the host CPU to check that the data contained in the Receive and Transmit Data Buffers is identical in order to ascertain the success or failure of the BIT. A 32 word self test sequence will take nominally 50µs. Note: The RTON bit in the Hybrid Control Word must be zero during this type of self test.
4. Whenever bit 2 of the HCWd is set the device will upon reception of a receive command containing a subaddress value of 1E (hex):-
   a. Transfer the associated Data Words to the "Processor RAM" Receive Data Buffer 1E (hex).
   b. Transfer the contents of "Processor RAM" Receive Data Buffer 1E (hex) to Transmit Data Buffer 1E (hex) in the "1553 RAM".
   c. Write the Command Word into the next Command Word Stack location and increment the CWSP.
   d. Take the $\overline{INT}$ line active low if bit 3 of the HCWd is set.
   e. Update the HIWd, 1553SWd, BITWd and 1553CWd locations in the "Processor RAM".

10. MODE COMMANDS (RX DATA)

Upon reception of a valid receive mode command with an associated Data Word, the device will :-

1. Load the Command Word Latches with the received Command Word.
2. Store the associated Data Word in the Receive Mode Data Buffer in the "1553B RAM" area indicated by the mode code field of the received Command Word.
3. Modify the 1553B Status Word using the SMWd and the 6 hard wired lines, then Transmit its 1553B Status Word .
4. Transfer the mode Data Word into the equivalent location in the "Processor RAM".
5. Write the Command Word into the next Command Word Stack location and increment the CWSP.
6. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
7. In the case of a Synchronise With Data Word mode command, also pulse the $\overline{SYNC}$ line active low if the bit 11 of the HCWd is set.
8. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

A typical Synchronise With Data mode command sequence is shown in Figure 6.



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 4.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 6: Synchronise with Data Word Mode Command

11. RECEIVE COMMANDS

Upon reception of a valid non-mode receive command, the device will:-

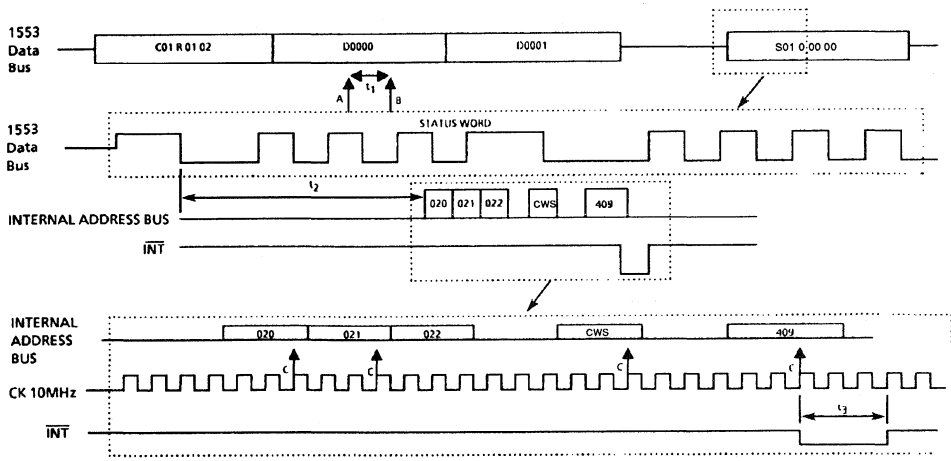
1. Load the Command Word Latches with the received Command Word.
2. Store the associated Data Words in the Receive Data Buffer in the "1553B RAM" area indicated by the subaddress value of the Command Word.
3. If the correct number of contiguous valid Data Words are received the device will modify the 1553B Status Word using SMWd and 6 hard wired status lines, transmit the 1553B Status Word, then inspect the RACWd .
4. If the subaddress value in the RACWd matches that of the Command Word the device will wait until the host CPU alters the contents of the RACWd before continuing, but will service any valid 1553B Command Words arriving in the meantime.
5. If the subaddress values do not match, the gate array will transfer the Data Words into the equivalent locations in the "Processor RAM".
6. Write the Command Word into the next Command Word Stack location and increment the CWSP.
7. Take the $\overline{INT}$ line active low if bit 4 of the HCWd is set.
8. Finally update the HIWd, 1553SWd, BITWd and 1553CWd locations in the "Processor RAM". Note: These locations may not always be updated if a further valid command is receivedwwith an inter-message gap less than 20µs after reception of a broadcast command.

Host CPU Actions:- Whenever the host CPU wants to read a Receive Data Buffer and wants to avoid reception of a 'part message' it must:-

1. Write the subaddress of the buffer into the RACWd. Note: No Transfer Control Word required for RACWd.
2. Wait for 600ns.
3. Read the Data Words out of the buffer in numerical order starting at the first location in the buffer.
4. Clear the RACWd on completion.

Error detection - if an error is detected in the incoming message the device will not transmit the 1553B Status Word, but the appropriate status word bits will be set and all further operations will be aborted, ie. the following RAM locations will not be updated, Command Word Stack and the CWSP. Also, the $\overline{INT}$ line will not go active and the invalid message will not be transferred into the "Processor RAM". However HIWd, 1553SWd, BITWd, 1553CWd will be updated as normal.

Figure 7 shows a 2 word receive command to subaddress 01. This figure identifies the gate array's accesses to the left hand side of the "Processor RAM". It can be seen that the first location in the Receive Data Buffer 020 (hex) is written, followed by location 021 (hex). Address 022 (hex) is then accessed without being written to. Finally one of the Command Word Stack locations is updated, the address of which is then written into location 409 (hex).



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 4.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 7: Receive Command - 2 Words to Subaddress 01

12. TRANSMIT COMMANDS

Upon reception of a valid non-mode transmit command the device will:-

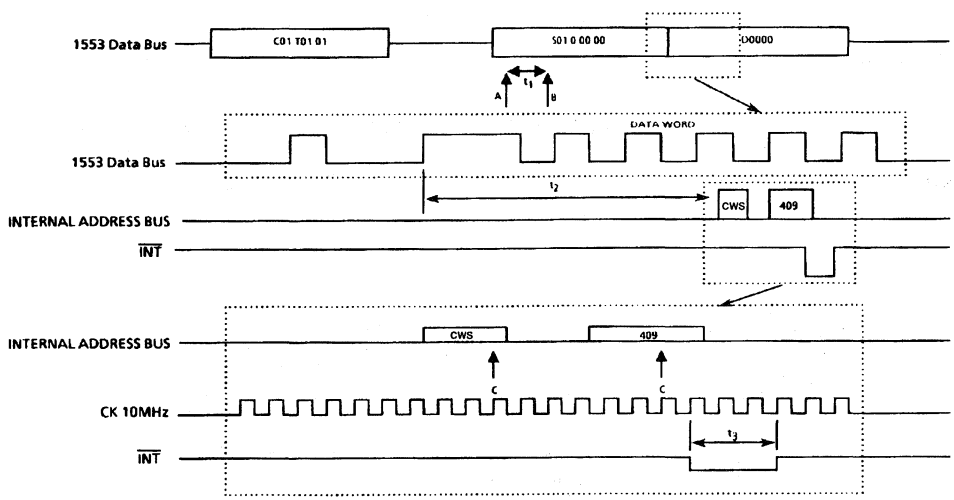
1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired status lines, then transmit the 1553B Status Word.
3. Transmit the appropriate number of Data Words contained in the Transmit Data Buffer indicated by the Command Word Subaddress bits.
4. Write the Command Word into the next Command Word Stack location and increment the CWSP.
5. Take the $\overline{INT}$ line active low if bit 5 of the HCWd is set.
6. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

Host CPU Actions - Whenever a host CPU wishes to update a Transmit Data Buffer, it must:-

1. If the appropriate Transmit Data Buffer has been updated within the last 800µs - check that neither TCWd contains the appropriate subaddress value.
2. Write the Data Words into the appropriate Transmit Data Buffer.
3. Interrogate the TCWd locations in order to ascertain which is zero.
4. Write the appropriate subaddress value and word count into the TCWd containing zero. A word count of 00 will ensure that all of the 32 words in the buffer are transferred.

When the gate array detects the TCWd being updated, it will transfer the indicated number of Data Words to the indicated buffer in the "1553B RAM". This transfer may be delayed if that buffer is being accessed in order to service a Transmit Command. Upon completion of the data transfer the device will clear the relevant TCWd.

Figure 8 shows a one word transmit command to a subaddress 01. This figure identifies the gate array's accesses to the LHS of the "Processor RAM". It can be seen that one of the Command Word Stack locations is written to the address, which is then written into address 409 (hex).



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

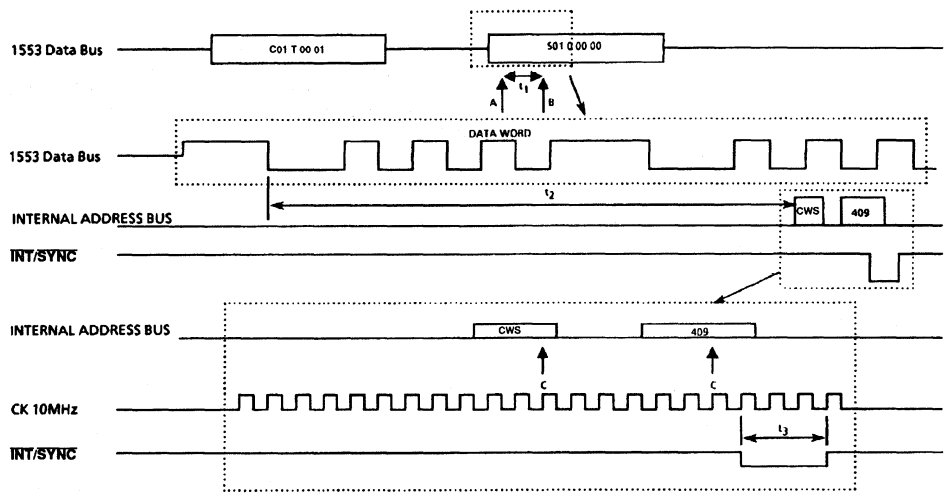
Figure 8: Transmit Command - 1 Word from Subaddress 01

13. MODE COMMANDS (NO DATA)

Upon reception of a valid mode command (no data) the device will:-

1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired status lines, then transmit the 1553B Status Word.
3. Write the Command Word into the next Command Word Stack location and increment the CWSP.
4. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
5. In the case of Reset RT mode command also pulse the $\overline{RSOP}$ line active low.
6. In the case of Synchronise Without Data mode command also pulse the $\overline{SYNC}$ line active low.
7. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

Typical Synchronise Without Data and Reset RT mode command sequences are shown in Figures 9 and 10 respectively.

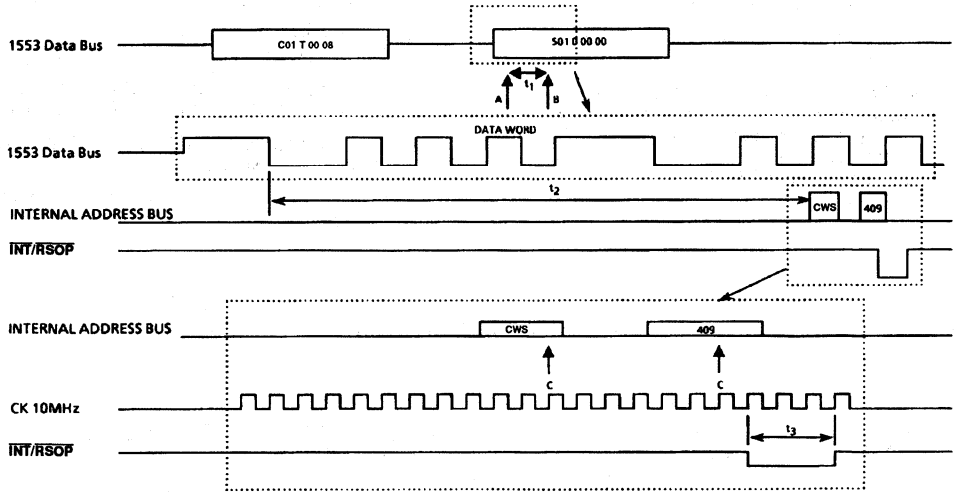


Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 9: Synchronise without Data Word Mode Command



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

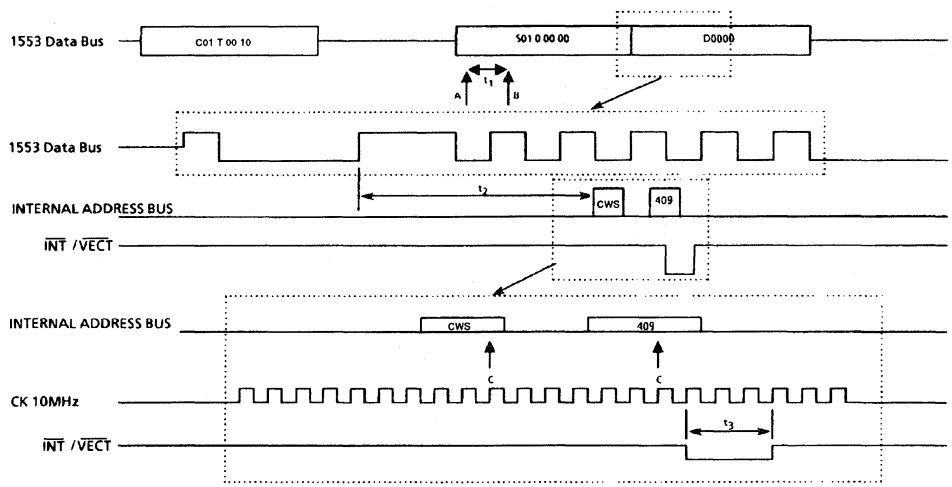
Figure 10: Reset Remote Terminal Mode Command

14. MODE COMMANDS (TX DATA)

Upon reception of a valid transmit mode command with an associated Data Word, the device will :-

1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired lines, then transmit its 1553B Status Word followed contiguously by the contents of the RAM location indicated by the mode code field of the Command Word.
3. Write the Command Word into the next Command Word Stack location and increment the CWSP.
4. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
5. In the case of a Transmit Vector Word mode command, also pulse the $\overline{VECT}$ line active low.
6. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

A typical Transmit Vector Word mode command sequence is shown in Figure 11.



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 11: Transmit Vector Word Mode Command

15. ILLEGAL COMMANDS

The MCT83100 implements the illegal command option of 1553B and sets the message error bit in the Status Word as appropriate in response to illegal mode commands. The mode commands that the MCT83100 deems legal are listed in Table 19. The host CPU is given the option of illegalising any broadcast-T/R-subaddress-word count combination by driving $\overline{ME}$ input low within 2.5µs of the CW11-0 output pins being updated. It is also possible to make all of the reserved mode commands legal by setting bit 3 of the SMWd low, and any of these may then be illegalised using the $\overline{ME}$ input.

Note: The $\overline{ME}$ input is strobed 2.5µs after the Command Word outputs change.

Label	Parameter	min	max	unit
t	CW11-0 Valid to $\overline{ME}$	-	2.5	µs

Table 18: Message Error Timing

16. BROADCAST COMMANDS

Upon reception of a valid Broadcast Command the device will load any associated Data Words into the Broadcast Receive Data Buffer indicated by the subaddress value. By setting bits 8 & 9 of the HIWd to zero the device can be prevented from acting upon broadcast commands - should a broadcast command be received it will be completely ignored.

Transmit/ Receive Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	no	no
1	00001	Synchronise	no	yes
1	00010	Transmit Status Word	no	no
1	00011	Initiate Self Test	no	yes
1	00100	Transmitter Shutdown	no	yes
1	00101	Override Transmitter Shutdown	no	yes
1	00110	Inhibit Terminal Flag Bit	no	yes
1	00111	Override Inhibit Terminal Flag Bit	no	yes
1	01000	Reset Remote Terminal	no	yes
1	10000	Transmit Vector Word	yes	no
0	10001	Synchronise	yes	yes
1	10010	Transmit Last Command	yes	no
1	10011	Transmit BIT Word	yes	no
0	10100	Selected Transmitter Shutdown	yes	yes
0	10101	Override Selected Transmitter Shutdown	yes	yes

Table 19: Legal Mode Commands

17. RESPONSE TIME

The response time of the MCT83100 when measured from the mid-point of the parity bit to the mid-point of the sync bit is 10.5 ±0.5µs.

Label	Parameter	Typ	Max	Unit
t_{INT}	$\overline{INT}$ Pulse Width with $\overline{INTACK}$ Low	300	385	ns
t_{SYNC}	$\overline{SYNC}$ Pulse Width	300	360	ns
t_{VECT}	$\overline{VECT}$ Pulse Width	300	360	ns
t_{RSOP}	$\overline{RSOP}$ Pulse Width	300	360	ns
t_{ILH}	$\overline{INTACK}$ falling edge to $\overline{INT}$ rising edge	-	30	ns

Table 20: Interrupt Timing

18. COMMAND WORD BITS 11-0

The twelve hard wired Command Word lines are updated by the device 60ns (max) after the rising edge of the 10MHz clock signal. The least significant eleven bits (CW10-0) follow the Command Word bits exactly. Bit 11 will be high for broadcast commands and low for non-broadcast commands.

19. RAM ACCESS

Whenever a host CPU attempts to access the same location as the on-board gate array the $\overline{RAMBUSY}$ signal will go active. The host CPU must not access the on-board RAM whilst $\overline{RAMBUSY}$ signal is active. The gate array accesses to the LHS of the "Processor RAM" are nominally 300ns for all 'receive' locations ie 000-3FF and 800-BFF (hex) and 400ns for all 'transmit' locations ie 400-7FF (hex). Hence the absolute maximum time that $\overline{RAMBUSY}$ will be active is 475 ns - ie gate array access (400ns) plus $\overline{RAMBUSY}$ delay (70ns) + 5ns to allow for clock skew.

Note: In the majority of system designs it is unlikely that both the gate array and the host CPU will attempt to access the same location at exactly the same time.

20. RECEIVE DATA BUFFER

In order to prevent reception of incomplete 1553 messages, a host CPU must write a RACWd containing the relevant subaddress value into location 405 (hex) before reading the Receive Data Buffer contents. The Data Buffer must be read in ascending numerical order starting at the first location of the Receive Data Buffer.

The on-board gate array inspects its internal copy of the RACWd contents immediately prior to initiating the transfer of a received message between the "1553 RAM" and the "Processor RAM". This transfer is carried out in ascending numerical order starting at the first location in the Receive Data Buffer. If the internal RACWd contains the same subaddress value as that contained in the received Command Word, then the transfer will be delayed until the RACWd contents are changed. If the subaddress values do not match, the transfer will go ahead.

Figures 13 shows when the data transfers occur after reception of a seven word receive command. Three situations are highlighted:-

a) During a 'normal' sequence when the host CPU accesses the Receive Data Buffer after the gate array has completed loading it.

b) If the RACWd is written to by the host CPU immediately after the internal RACWd has been interrogated by the gate array then the host CPU is held off from reading the former contents of the "Processor RAM" by the $\overline{RAMBUSY}$ signal.

c) When the RACWd is written to by the host CPU immediately before the gate array has interrogated it. In this situation the gate array 'C' transfer, (see Figure 12), is held up until the host CPU alters the contents of the RACWd .

The gate array accesses will take 300ns each therefore the maximum delay incurred on the host CPU attempting to read a Receive Data Buffer will be 475ns minus the time difference between it writing the RACWd and then attempting to read the data location.

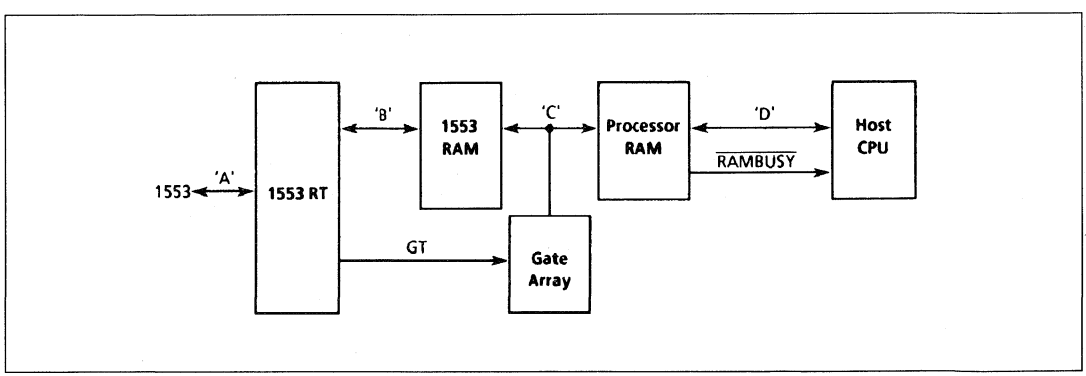


Figure 12: MCT83100 Data Flow Diagram (read in conjunction with Figures 13 and 14)

21. RECEIVE DATA TRANSFERS

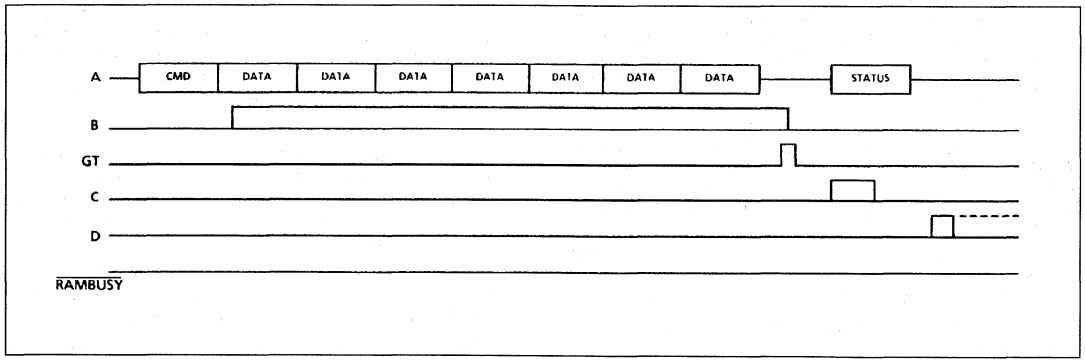


Figure 13a: Normal Sequence

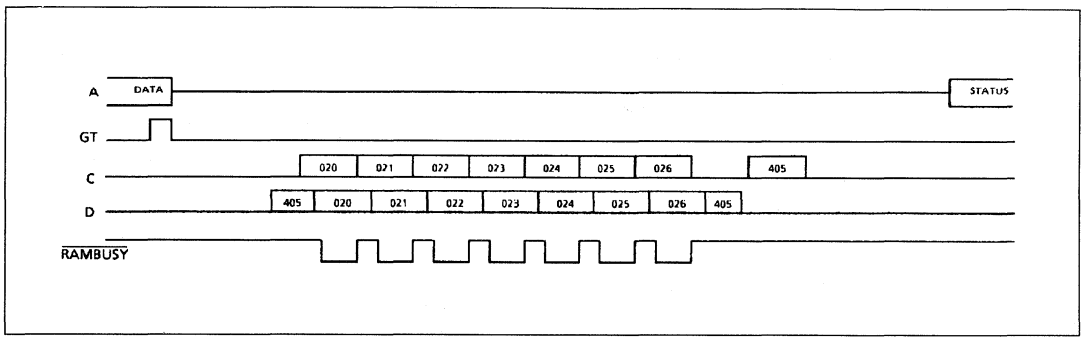


Figure 13b: RACWd Updated After Being Interrogated by The Gate Array

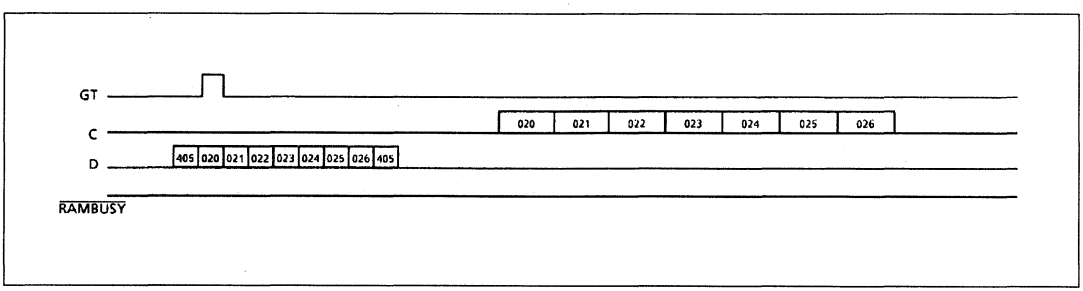


Figure 13c: RACWd Updated Before Being Interrogated By The Gate Array

Note: A,B,C and D refer to the data transfers indicated in Figure 12. Host CPU memory access time is shown considerably less than 300ns for diagramatic purposes. Normally processor access would be slower and less $\overline{\text{RAMBUSY}}$ pulses would be generated.

22. TRANSMIT DATA BUFFER

In order to prevent transmission of incomplete 1553 messages, the host CPU must ensure that neither TCWd contains the appropriate subaddress value, before updating a Transmit Data Buffer. Once the Data Buffer has been updated, the host CPU must then interrogate the TCWd locations in order to ascertain which is zero, then write the appropriate subaddress value and word count into the TCWd containing zero. When the gate array detects the TCWd being updated, it will transfer the indicated number of Data Words to the indicated buffer in the "1553 RAM". This transfer may be delayed if that buffer is being accessed in order to service a Transmit Command. Upon completion of the data transfer the device will clear the relevant TCWd. Figure 8 details the transmit data transfers.

The host CPU may encounter two delays in updating a Transmit Data Buffer.

(i) If the host CPU instructs the gate array to transfer a 32 word message immediately after reception of a transmit command containing the relevant subaddress value, then the gate array will not clear the TCWd for 736µs assuming a second 32 word transfer is requested using the other TCWd.

(ii) If the gate array is instructed to transfer two 32 word messages simultaneously then both TCWds will be non zero for a maximum of 82µs, assuming simultaneous reception of a 32 word receive command. (The internal transfers interleave.)

Figure 14b shows how an internal transmit data transfer is delayed by the transfer being initiated just after reception of a transmit command to that subaddress.

Figure 14c shows that an internal transmit data transfer, once started, will procede in parallel with the much slower 1553 data transfer.

Note: A 32 word Transmit Data Buffer update will take typically 40µs.

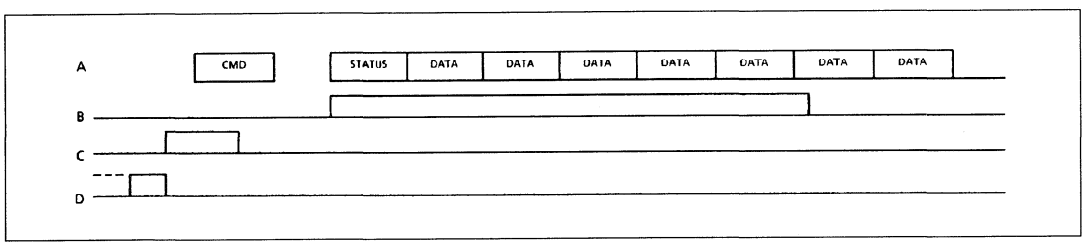


Figure 14a: Normal Sequence

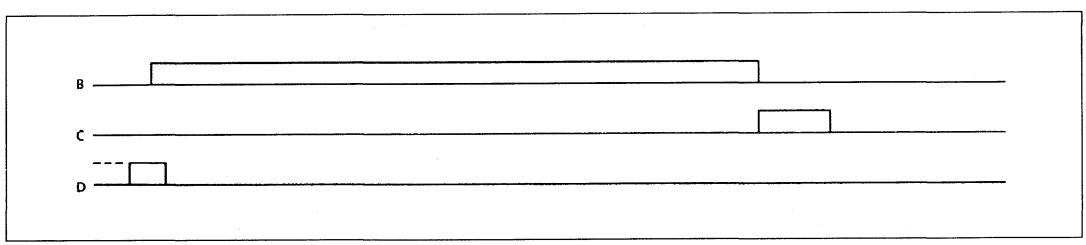


Figure 14b: Transmit Command Received Before TCWd is Updated

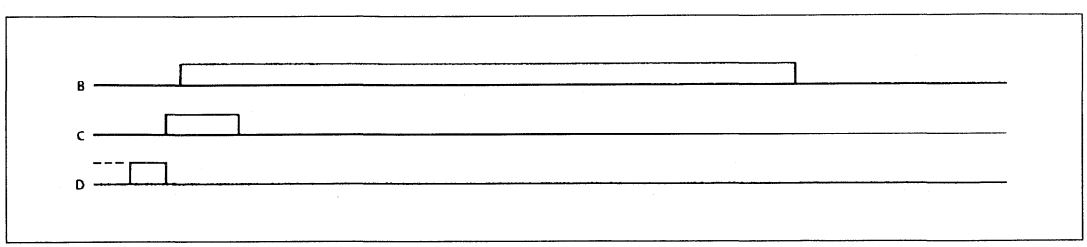


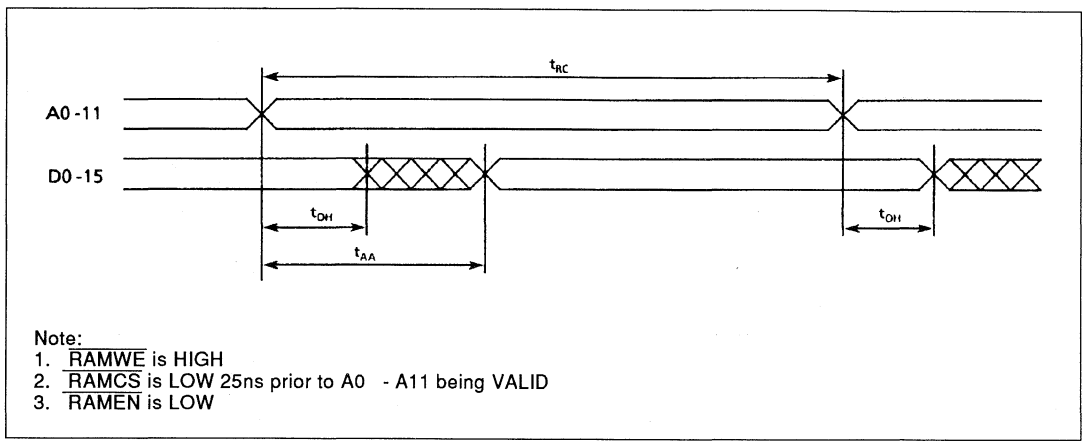
Figure 14c: Transmit Command Received After TCWd is Updated

Note: A,B,C and D refer to the data transfers indicated in Figure 12.

23. MEMORY ACCESS SIGNAL TIMINGS

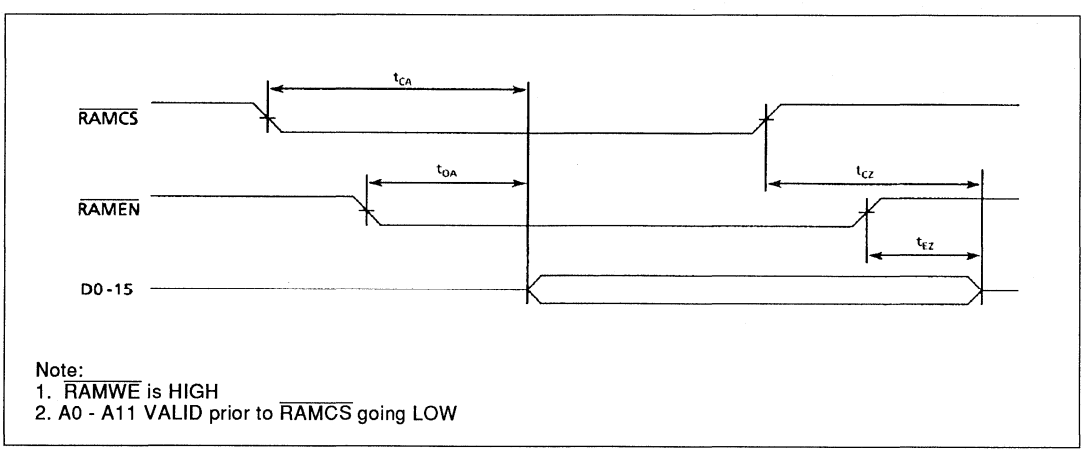
Label	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	90	2400	ns
t_{AA}	Address Access Time	-	90	ns
t_{CA}	$\overline{RAMCS}$ Access Time	-	115	ns
t_{OA}	$\overline{RAMEN}$ Access Time	-	40	ns
t_{OH}	Output hold from address change	10	-	ns
t_{EZ}	$\overline{RAMEN}$ rising edge to Data in High Z	-	40	ns
t_{CZ}	$\overline{RAMCS}$ rising edge to Data in High Z	-	65	ns

Table 21: Read Cycle - Figures 15 and 16 apply



Note:
1. $\overline{RAMWE}$ is HIGH
2. $\overline{RAMCS}$ is LOW 25ns prior to A0 - A11 being VALID
3. $\overline{RAMEN}$ is LOW

Figure 15: Timing Waveform of Read Cycle 1

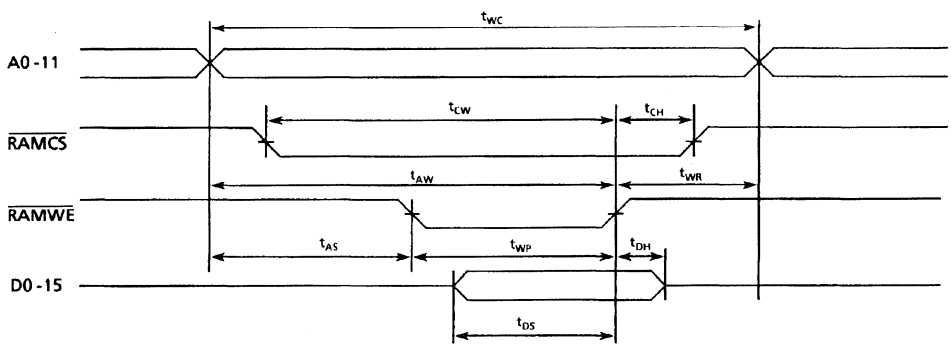


Note:
1. $\overline{RAMWE}$ is HIGH
2. A0 - A11 VALID prior to $\overline{RAMCS}$ going LOW

Figure 16: Timing Waveform of Read Cycle 2

Label	Parameter	Min	Max	Unit
t_{WC}	Write Cycle Time	115	2400	ns
t_{CW}	$\overline{RAMCS}$ Active to $\overline{RAMWE}$ rising time	110	-	ns
t_{AW}	Address Valid to $\overline{RAMWE}$ rising edge	85	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	$\overline{RAMWE}$ pulse Width	55	-	ns
t_{WR}	Address Hold Time after $\overline{RAMWE}$ rising edge	0	-	ns
t_{CH}	$\overline{RAMCS}$ hold time after $\overline{RAMWE}$ rising edge	0	-	ns
t_{DS}	Data Set Up time	30	-	ns
t_{DH}	Data Hold Time	0	-	ns

Table 22: Write Cycle - Figure 17 Applies



Note:
1. $\overline{RAMWE}$ is HIGH during address transition
2. $\overline{RAMOE}$ is HIGH

Figure 17: Timing Waveform of Write Cycle

Label	Parameter	Min	Max	Unit
t_{CBL}	$\overline{RAMCS}$ to $\overline{RAMBUSY}$ active	-	70	ns
t_{CBH}	$\overline{RAMCS}$ to $\overline{RAMBUSY}$ inactive	-	70	ns
t_{ABL}	Address Valid to $\overline{RAMBUSY}$ active	-	55	ns
t_{ABH}	Address Valid to $\overline{RAMBUSY}$ inactive	-	45	ns
t_{ICS}	Internal $\overline{RAMCS}$ Pulse	-	400	ns

Table 23: $\overline{RAMBUSY}$ Timing - Figures 18 and 19 Apply

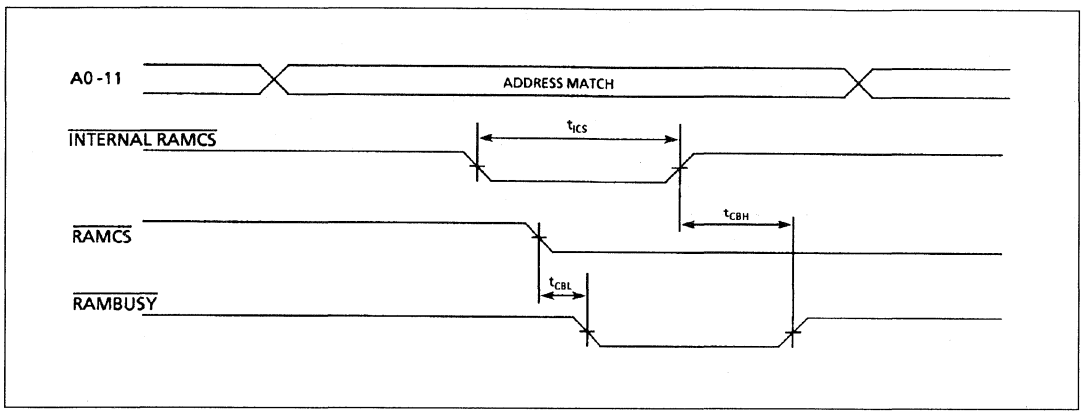


Figure 18: Timing Waveform of Contention Cycle - CS Arbitration

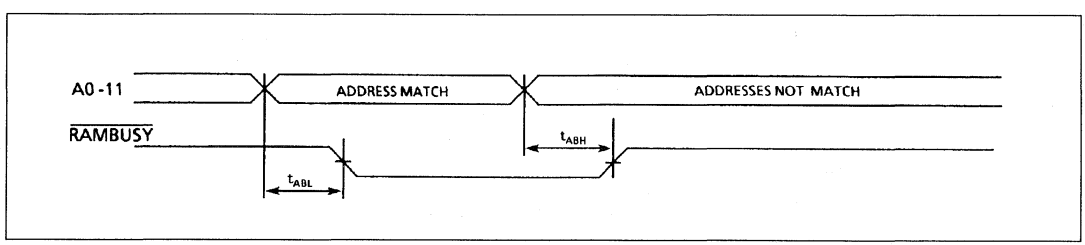


Figure 19: Timing Waveform of Contention Cycle - Address Arbitration

24. TYPICAL INTERFACE CONNECTIONS

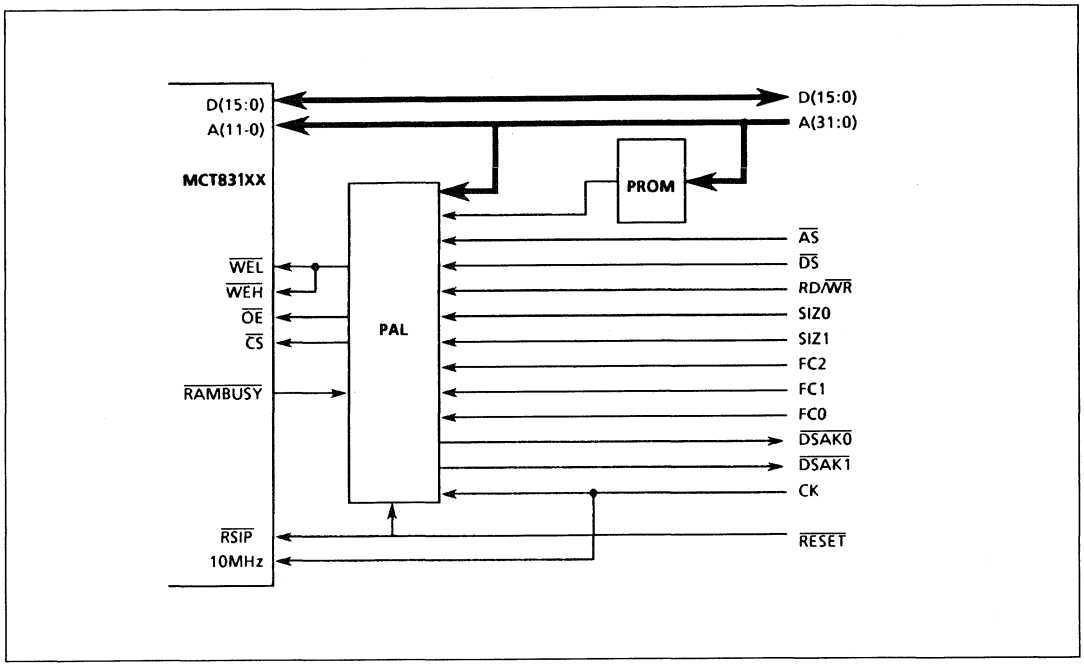


Figure 20: Typical 16-Bit Interface

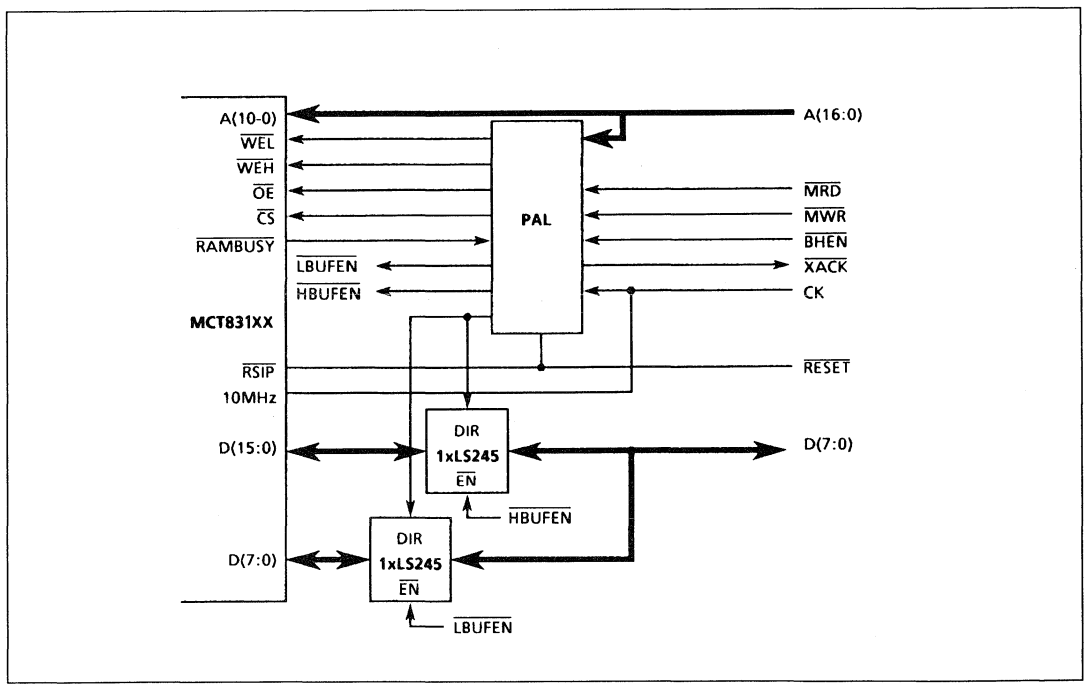


Figure 21: Typical 8-Bit Interface

25. PACKAGE OUTLINES

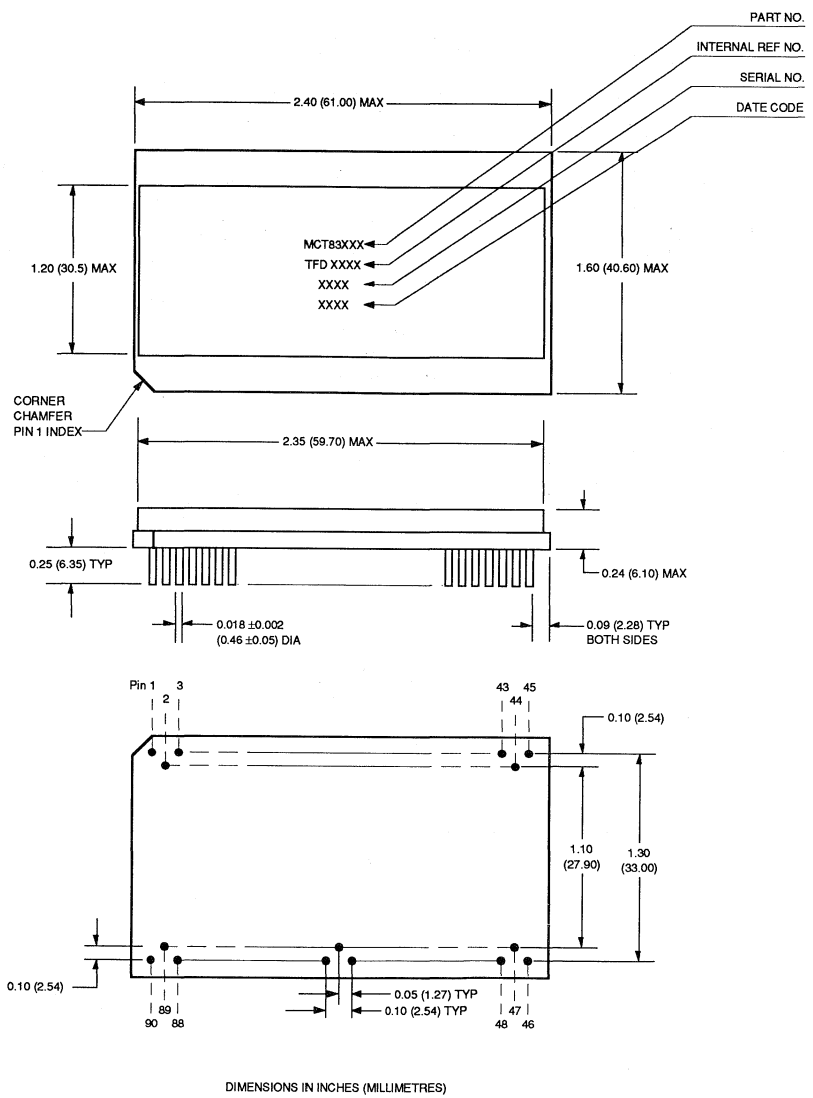


Figure 22: Package Outline - Plug-In

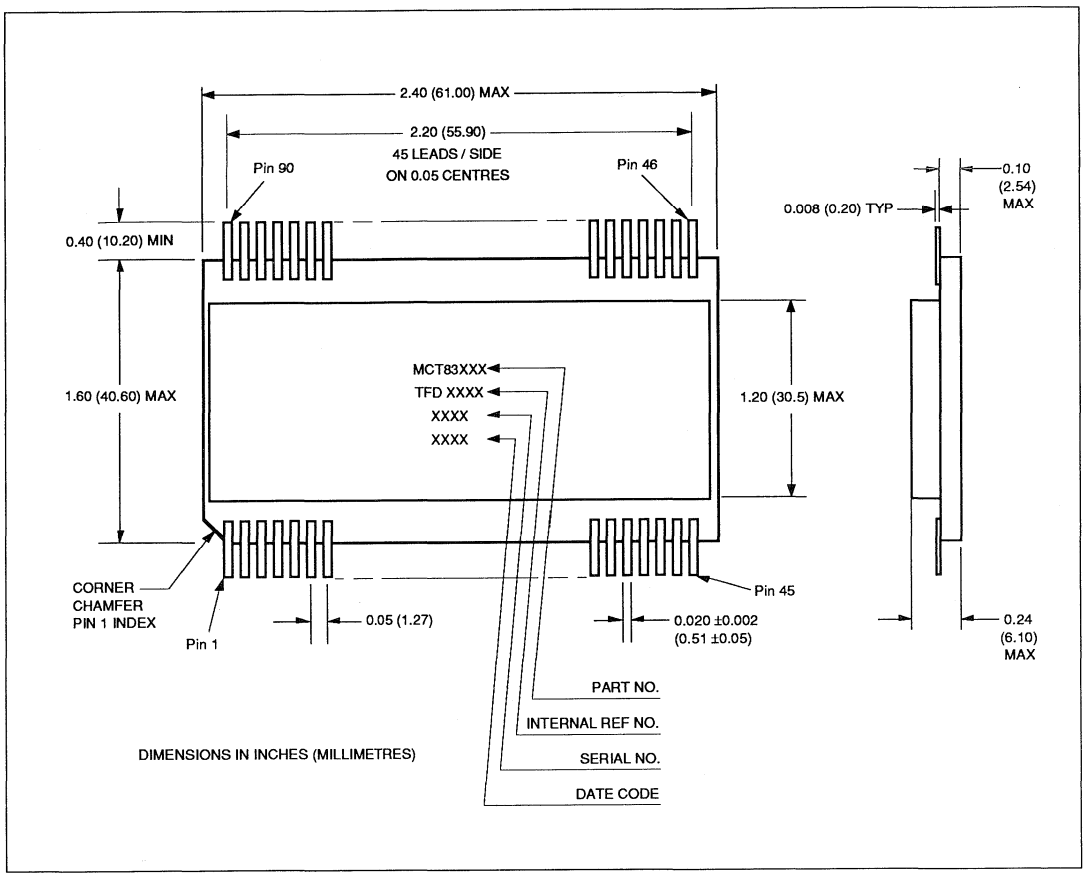


Figure 23: Package Outline - Flat-Pack

APPENDIX A - MCT83910/1/2 OPERATION

The MCT83910 version of the MCT83100 series of hybrids has been designed to provide the STANAG 3838 Remote Terminal port of a STANAG 3910/STANAG 3838 interface.

A typical interface is shown in Figure 24.

The MCT83910 is similar to the MCT83102 but differs in the following areas:

1. The 'hard' Hybrid Initialise Word is no longer buffered within the device and if required must be buffered externally. A $\overline{\text{HIWDEN}}$ output is provided to enable the contents of such a buffer onto the 'HD' bus (see below).

2. The 12 bit latched Command Word is no longer available on dedicated pins but can be latched off the 'HD' bus (see below). A CWLD output is provided to latch the Command Word.

3. The 16 bit data bus between the MIL-STD-1553B interface device and the left hand side of the "1553 RAM" is made available to the STANAG 3910 interface along with 6 control lines. This 16 bit 'HD' bus and its associated control lines (see Tables 26) are provided for the transfer of high speed action and status words.

All commands/status/data transfers over the 'HD' bus are preceded by the transfer of a control word. This control word is available on both edges of the $\overline{\text{CLE}}$ output and provides a description of the following word. Details of the bit allocation of the control word are given in Table 25. The control words for both receive and transmit commands along with an indication of the timing relationships between the STANAG 3910 interface control signals is given in Figures 25 and 26.

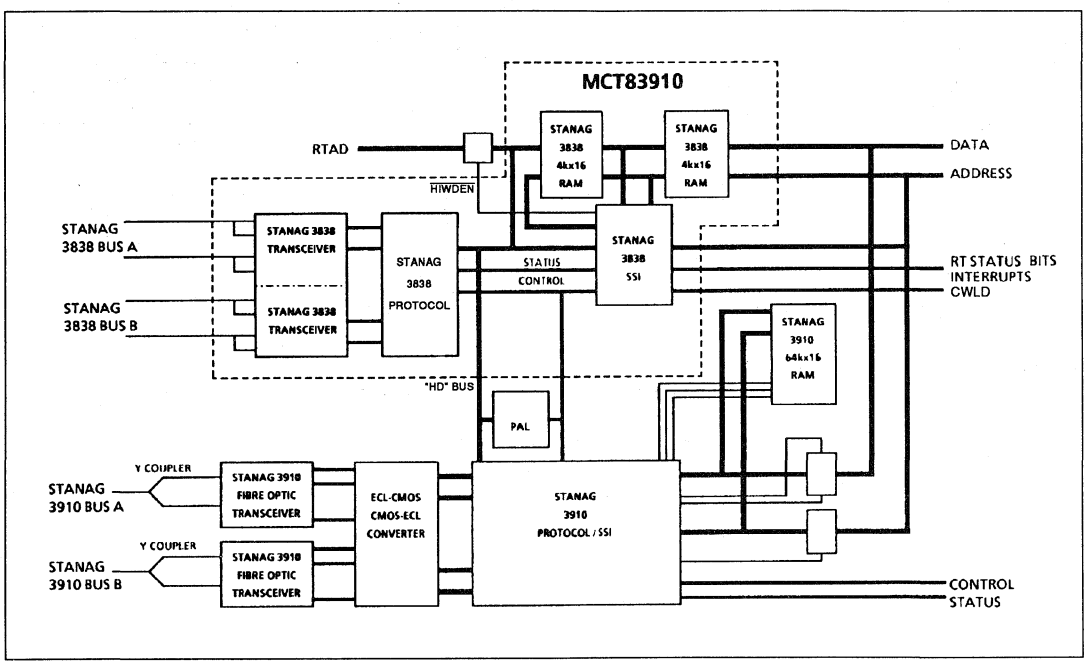


Figure 24: STANAG 3910 / STANAG 3838 Interface Example

MCT83910/1/2 PIN-OUT

1	BUS1(+)	24	*HD14*	47	RAMBUSY	70	*GT*
2	BUS1(-)	25	*HIWDEN*	48	D15	71	*WE*
3	VEE(1)	26	*HD6*	49	D14	72	*HD3*
4	VDD(1)	27	*HD5*	50	D13	73	*HD2*
5	0V	28	*HD4*	51	D 12	74	*HD1*
6	VCC	29	RAMWEH	52	D11	75	*HD0*
7	TP1	30	RAMWEL	53	D10	76	ME
8	TP2	31	RAMOE	54	D9	77	SR
9	TXINH1	32	RAMCS	55	D8	78	BUSY
10	H/S	33	A11	56	D7	79	SSF
11	10MHZ	34	A10	57	D6	80	*CSIN*
12	RSIP	35	A9	58	D5	81	TF
13	RSOP	36	A8	59	D4	82	TXINH0
14	VECT	37	A7	60	D3	83	TP4
15	SYNC	38	A6	61	D2	84	TP3
16	INT	39	A5	62	D1	85	VCC
17	INTACK	40	A4	63	D0	86	0V
18	*HD12*	41	A3	64	*RD*	87	VDD(0)
19	*HD8*	42	A2	65	*CLE*	88	VEE(0)
20	*HD10*	43	A1	66	*HD9*	89	BUS0(-)
21	*HD15*	44	A0	67	*CSOUT*	90	BUS0(+)
22	*HD11*	45	0V	68	*HD7*		
23	*HD13*	46	CASE	69	*CWLD*		

Notes:
1. Refer to Table 2 for description of power supply options.
2. For the 24 signals in italics refer to Tables 26 for description. Remainder of pins are described in Table 2.

Table 24: MCT83910 Series Pin Out

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>BCST</td><td>Command word had the broadcast address when high</td></tr>
<tr><td>14</td><td>RESMODE</td><td>Reserved mode code detected when high</td></tr>
<tr><td>13</td><td>SYNCVEC</td><td>Synchronise/Transmit Vector Word being transferred when high</td></tr>
<tr><td>12</td><td>CMDSTAT</td><td>Command/Status Word being transferred when high</td></tr>
<tr><td>11</td><td>NMD</td><td>Non Mode Data: 1=normal data transfers. 0=mode data transfers</td></tr>
<tr><td>10</td><td>TR</td><td rowspan="11">During data transfers the SA field contains the subaddress of the command word and the CWC field contains the Current word count. During command word, status modifier word and mode data transfers, the SA and CWC field are as described below:

<table>
<tr><th>WE</th><th>RD</th><th>TR</th><th>SA</th><th>CWC</th><th></th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>00</td><td>00</td><td>Command word (Receive)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>00</td><td>00</td><td>Command word (Transmit)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>00</td><td>00</td><td>Status modifier word read (Receive)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>01-1E</td><td>0-1F</td><td>Received data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>01-1E</td><td>0-1F</td><td>Data to be transmitted</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1F</td><td>0-1F</td><td>Mode data (to S/System)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1F</td><td>0-1F</td><td>Mode data (from S/System)</td></tr>
</table>
Thus, command words, data words and data words associated with mode commands can be directly located in subsystem memory.</td></tr>
<tr><td>9</td><td>SA4</td></tr>
<tr><td>8</td><td>SA3</td></tr>
<tr><td>7</td><td>SA2</td></tr>
<tr><td>6</td><td>SA1</td></tr>
<tr><td>5</td><td>SA0</td></tr>
<tr><td>4</td><td>CWC4</td></tr>
<tr><td>3</td><td>CWC3</td></tr>
<tr><td>2</td><td>CWC2</td></tr>
<tr><td>1</td><td>CWC1</td></tr>
<tr><td>0</td><td>CWC0</td></tr>
</table>

Table 25: MIL-STD-1553B Interface Control Word

Pin	Name	Dir	Logic	Description
21	HD15	I/O	C4	16 bit internal tri-state data bus ('HD' BUS) which allows subsystem to detect STANAG 3910 action words. The Hybrid Initialise Word is loaded by the device on power up via this data bus. The 1553B Command Word is available on this bus on both edges of CWLD.
24	HD14			
23	HD13			
18	HD12			
22	HD11			
20	HD10			
66	HD9			
19	HD8			
68	HD7			
26	HD6			
27	HD5			
28	HD4			
72	HD3			
73	HD2			
74	HD1			
75	HD0			

Table 26a: MCT83910 Pin Descriptions Internal Data Bus

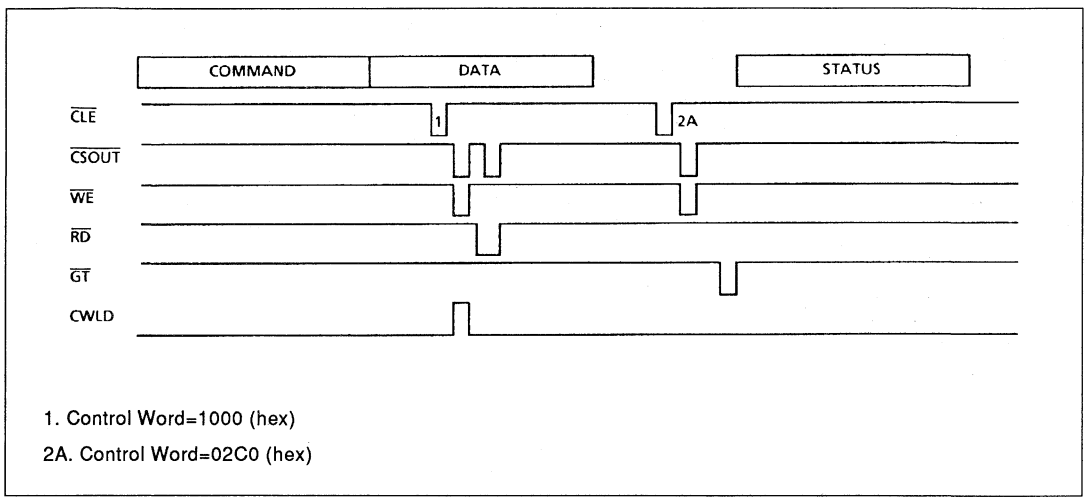
Pin	Name	Dir	Logic	Description
80	$\overline{CSIN}$	I/P	C4	Active low chip select input to the LHS of the 1553B dual port RAM.
67	$\overline{CSOUT}$	O/P		Active low internal chip select output which under normal operation should be connected to pin 80. Failure to make this connection allows the subsystem to connect external devices to the internal data bus.
25	$\overline{HIWDEN}$	O/P		Active low pulse which can be used to enable Hybrid Initialise Word onto the internal data bus.
69	CWLD	O/P		Active high pulse which can be used to load the 1553B Command Word off the internal data bus.
70	$\overline{GT}$	O/P		Active low pulse which indicates a valid 1553B transaction.
71	$\overline{WE}$	O/P		Active low write pulse to LHS of the 1553B dual port RAM
64	$\overline{RD}$	O/P		Active low read pulse to LHS of the 1553B dual port RAM
65	$\overline{CLE}$	O/P		Active low pulse which can be used to load internal control words off the internal data bus.

Table 26b: MCT83910 Pin Descriptions Internal Data Bus Control

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage	2.5	-	-	V
VOL	Output Low Level Voltage	-	-	0.4	V
IOH	Output High Level Current	-	-	-0.8	mA
IOL	Output Low Level Current	-	-	2.0	mA
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	0	-	0.7	V
IIH	Input High Level Current	-	-	10	µA
IIL	Input Low Level Current	-	-	-0.4	mA

Table 27: MCT83910 Electrical Characteristics - CMOS Input/Output - Type C4

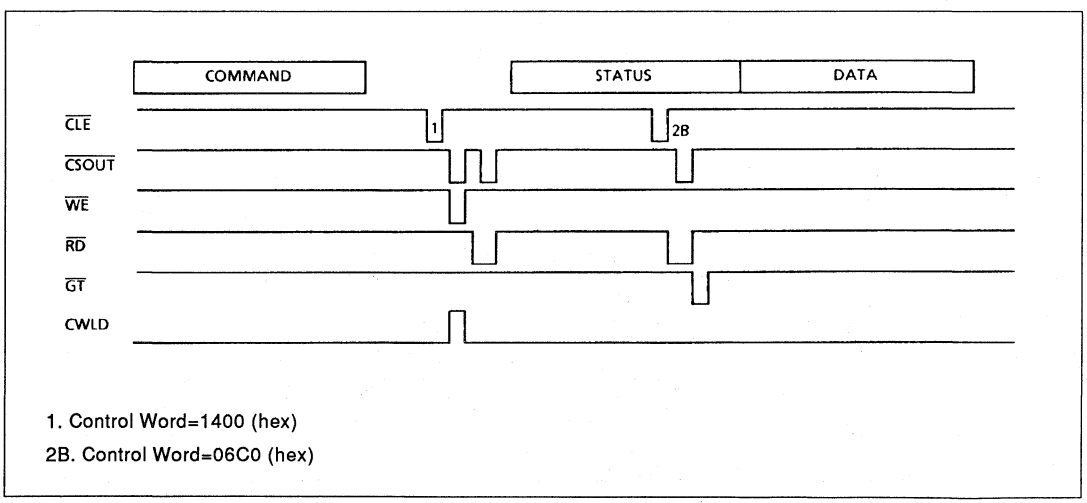
STANAG 3910 Interface Timing Diagrams



1. Control Word=1000 (hex)

2A. Control Word=02C0 (hex)

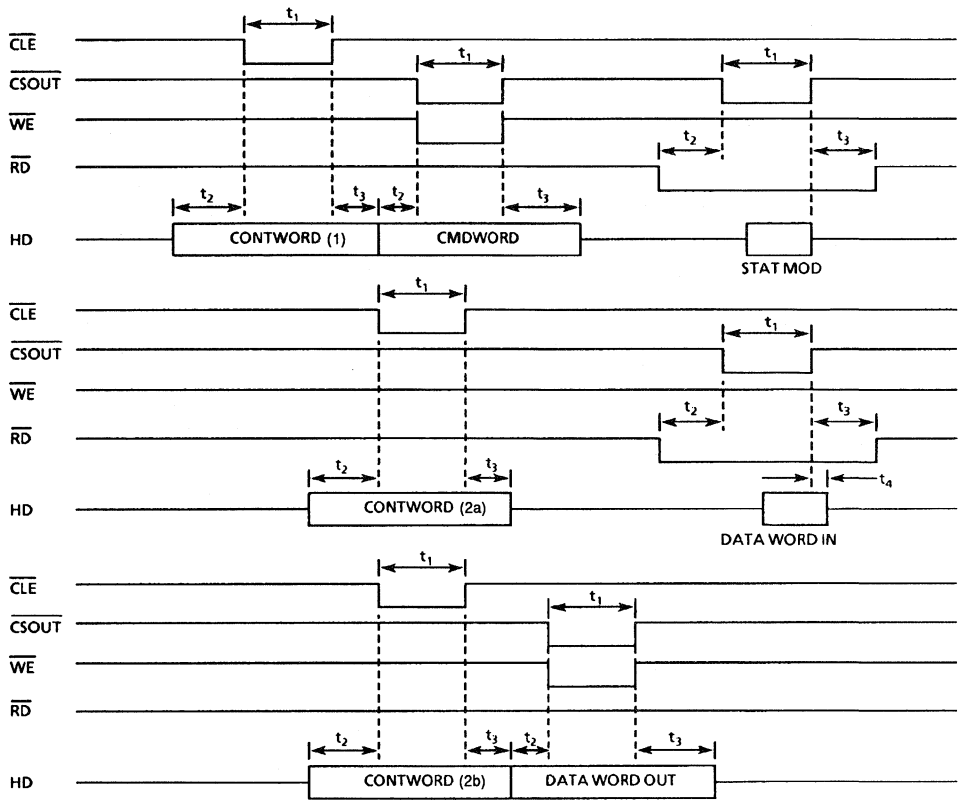
Figure 25a: Receive Command - 1 Word Subaddress 22



1. Control Word=1400 (hex)

2B. Control Word=06C0 (hex)

Figure 25b: Transmit Command - 1 Word Subaddress 22



Label	Timed from	Timed to	Min	Typ	Max	Unit
t1	Strobe↓	Strobe↑	-	1.0	-	µs
t2	Data Valid	Strobe↓	-	0.5	-	µs
t3	Strobe↑	Data Valid	-	0.5	-	µs
t4	Strobe↑	Data Valid	0	-	-	µs

Notes:
1. 'strobe' may be any of $\overline{CLE}$, $\overline{CSOUT}$ or $\overline{WE}$, whichever is relevent for the transfer.
2. '↑' represents a low to high transition.
3. '↓' represents a high to low transition.

Figure 26: STANAG 3910 Interface Timing Details (refer to Figures 25a and 25b for basic transfers)

Section 2

Driver/Receivers (Transceivers)

3122-1.2 October 1991

CT1487M/CT1589M

MIL-STD-1553 LOW POWER SINGLE AND DUAL TRANSCEIVERS

FEATURES

- Available in ±15V (CT1487M) and ±12 V (CT1589M) versions
- AC interstage coupling prevents static burnout
- Receiver filtered to improve S/N ratio of system
- Dissipates only 1.3 watt total at 25% transmitting duty cycle (dual unit - 1.8 watts total). 100% duty cycle permissible at 125°C case temperature
- 20 mV typical output offset
- Meets MIL-STL-1553A/B
- Available to Standard Military Drawings (see Ordering Information)
- 24 pin double dip package or flat pack for single unit
- 36 pin double dip package or flat pack for dual unit
- TTL compatible

Note: All data shown is for a single transceiver unless otherwise noted. Dual transceivers are two completely independent units in a common package.

GENERAL DESCRIPTION

The CT1487M/CT1589M family of single and dual transceivers is a second generation series incorporating monolithic bipolar devices for improved reliability and producibility. For thermal considerations, the drive stage transistors are "off" the bipolar array. Input/output signals are compatible with both MIL-STD-1553A and B systems.

DETAILED DESCRIPTION

RECEIVER DESCRIPTION

The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are RX DATA OUT and RX $\overline{\text{DATA}}$ OUT and represent positive and negative excursions, respectively, of the input beyond a predetermined threshold. See Figure 2 for receiver logic waveforms.

The positive and negative thresholds are designed for optimum word error rate. The receiver begins to detect Data Bus signals (1 MHz, sinusoidal) that exceed 0.9 volt nominal peak-to-peak when used with the specified transformer. See Figure 4 for typical input/output connections.

If the RECEIVER STROBE input is LOW, the RX DATA OUT and RX $\overline{\text{DATA}}$ OUT are inhibited. If unused, a 2K-ohm pullup to +5V is recommended.

Note: See ORDERING INFORMATION for units with inverted outputs. (Pg 7)

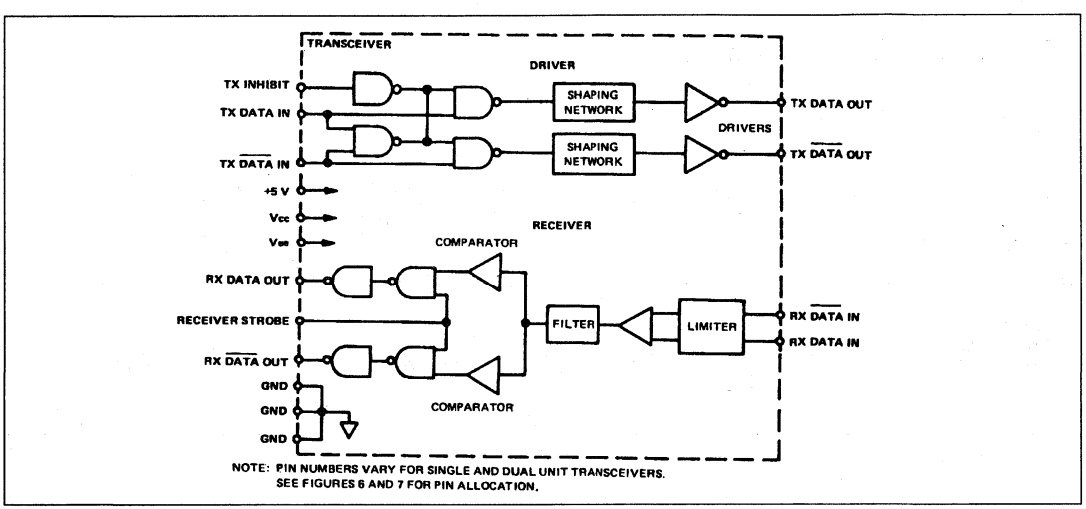


Figure 1: Functional Diagram, CT1487M

DRIVER DESCRIPTION

The Driver section accepts complementary TTL data at the input. When coupled to the Data Bus with the specified transformer (isolated on the Data Bus side with 55-ohm fault isolation resistors and loaded by two 70-ohm terminations plus additional receivers), the Data Bus signal produced is 6.8 volts nominal peak-to-peak (at point A, Figure 4).

When both TX DATA IN and TX $\overline{\text{DATA}}$ IN inputs are both held LOW or held HIGH, the driver output becomes a high impedance and is removed from the line. In addition, an overriding TX INHIBIT input takes priority over the condition of the data inputs and disables the driver. See Figure 3 for the driver logic waveforms.

TX DATA IN and TX $\overline{\text{DATA}}$ IN inputs must be complementary waveforms of 50% average duty cycle and with less than 15 ns skew between them.

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS	CT1487	CT1589
Power supply voltage (V_{cc})	−0.3 to +18.0V	−0.3 to + 18.0V
Power supply voltage (V_{ee})	+0.3 to −18.0V	+0.3 to −18.0V
Power supply voltage (V_{ccl})	−0.3 to +7.0V	−0.3 to +7.0V
Logic input voltage (RECEIVER STROBE, INHIBIT, TX $\overline{\text{DATA}}$ IN, TX DATA IN)	−0.3 to +5.5V	−0.3 to +5.5V
Receiver differential input (RX DATA IN, RX $\overline{\text{DATA}}$ IN)	± 20 V (40 V p-p)	± 20 V (40 V p-p)
Receiver input voltage (RX DATA IN or RX $\overline{\text{DATA}}$ IN)	± 15 V	± 15 V
Driver output current (TX DATA OUT or TD $\overline{\text{DATA}}$ OUT)	+200 mA	+300 mA
Transmission duty cycle at T_c = 125°C Operating case temperature range (T_c)	100% −55 to +125°C	100% −55 to +125°C

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION	SYMBOL	CT1487M MIN	CT1487M TYP	CT1487M MAX	CT1589M MIN	CT1589M TYP	CT1589M MAX	UNIT
Power supply voltages	V_{cc} V_{ee} V_{ccl}	14.25 -14.25 4.5	15 -15 5	15.75 -15.75 5.5	11.4 -11.4 4.5	12 -12 5	12.6 -12.6 5.5	V V V
Power dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	P_c	Note 1	350	500	Note1	350	500	mW
Thermal resistance, most critical device	$\varnothing_{jc}$			50			50	°C/W
Junction to case temperature rise of most critical device at 100% duty cycle transmission	T_{jc}			25			25	°C
Total supply current "standby" mode, or transmitting at less than 1% duty cycle (e.g. 20 µs of transmission every 2ms or longer interval)			S* D*	S* D*		S* D*	S* D*	
	I_{cc}		15 30	22 44		15 30	22 44	mA
	I_{ee}	Note 2	25 50	35 70	Note 2	25 50	35 70	mA
	I_{ccl}	Note 2	32 64	45 90	Note 2	32 64	45 90	mA
Total supply current transmitting at 1MHz into a 35-ohm load at point A in Figure 4 — DUTY CYCLE								
25%	$I_{cc}25$	Note 3	55 70	75 100	Note 3	70 85	95 120	mA
100%	$I_{cc}100$	Note 3	185 200	235 260	Note 3	224 240	290 315	mA

* S = single unit, D = dual unit (one unit transmitting)

Notes: 1. Decreases linearly to zero at zero duty cycle.
2. I_{ee} and I_{ccl} limits do not change with mode of operation or duty cycle.
3. Decreases linearly to applicable "standby" value at zero duty cycle.

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION (See Figure 2)

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Differential input impedance DC to 1MHz		Z_{in}	9 K			ohms
Differential voltage range		V_{idr}	± 20V			V_{peak}
Input common mode voltage range		V_{icr}	± 10V			V_{peak}
Common mode rejection ratio (from point A, Figure 4)		CMRR	40			dB
STROBE characteristics (Logic "0" inhibits output)						
"0" input current (vs = 0.4 V)		I_{il}			-1	mA
"1" input current (Vs = 2.7 V)		I_{il}			40	µA
"0" input voltage		V_{il}			0.7	V
"1" input voltage		V_{ih}	2			V
Threshold characteristics (sine wave at 1MHz) NOTE: Threshold voltages refer to point A, Figure 4.		V_{th1}	0.8		1.1	V_{p-p}
Filter characteristics	2 MHz	V_{th2}	1.5		8	V_{p-p}
(sine wave input)	3 MHz	V_{th3}	5			V_{p-p}
OUTPUT CHARACTERISTICS						
"1" state (I_{source} = 400 µA)		V_{oh}	2.5	3.4		
"0" state (I_{sink} = 4 mA) NOTE: With receiver input below threshold both RX DATA OUT and RX $\overline{\text{DATA}}$ OUT remain in "0" state.		V_{oh}			0.5	
Delay (average) from differential input zero crossings to RX DATA OUT and RX $\overline{\text{DATA}}$ OUT output 50% points		t_{DRX}		340	450	ns

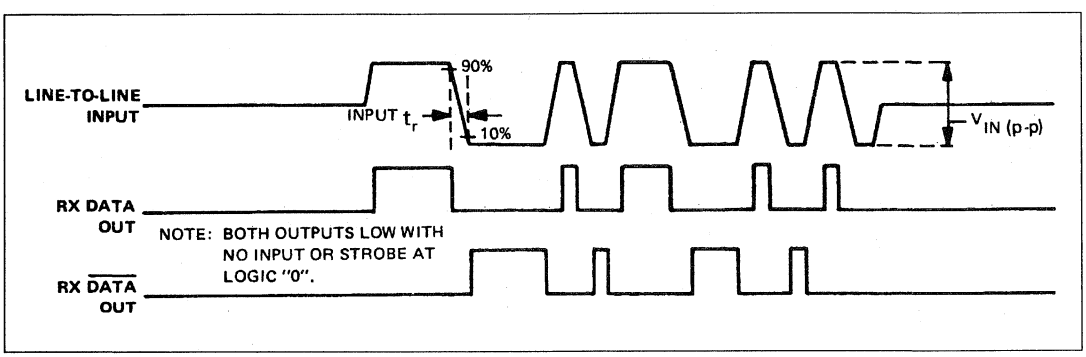


Figure 2: Receiver Logic Waveforms (for Inverted Data Output, see Ordering Information)

ELECTRICAL CHARACTERISTICS, DRIVER SECTION (See Figure 3)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
"0" input current (V_{in} = 0.4 V)	I_{il}			–1	mA
"1" input current (V_{in} = 2.7 V)	I_{ih}			80	µA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Delay from TX INHIBIT (0 → 1) to inhibited output impedance	t_{DXOFF}		150	225	ns
Delay from TX INHIBIT (1 → 0) to active output impedance	t_{DXON}		100	150	ns
Differential output noise	V_{noi}			10	mV_{p-p}
Differential output impedance (inhibited) at 1 MHz	Z_{oi}	8K			ohms
OUTPUT CHARACTERISTICS					
Differential output level at point B, Figure 4 (145-ohm load)	V_o	26	28	35	V_{p-p}
Rise and fall times (10%–90% of p-p output)	t_r	100	160	300	ns
Output offset at point A in Figure 4 (35-ohm load) 2.5 µs after mid-bit crossing of parity bit of last word of a 660 µs message	V_{os}		±20	±75	mV peak
Delay from 50% point of TX DATA IN or TX $\overline{\text{DATA}}$ IN to zero crossing of differential output	t_{DTX}		100	200	ns

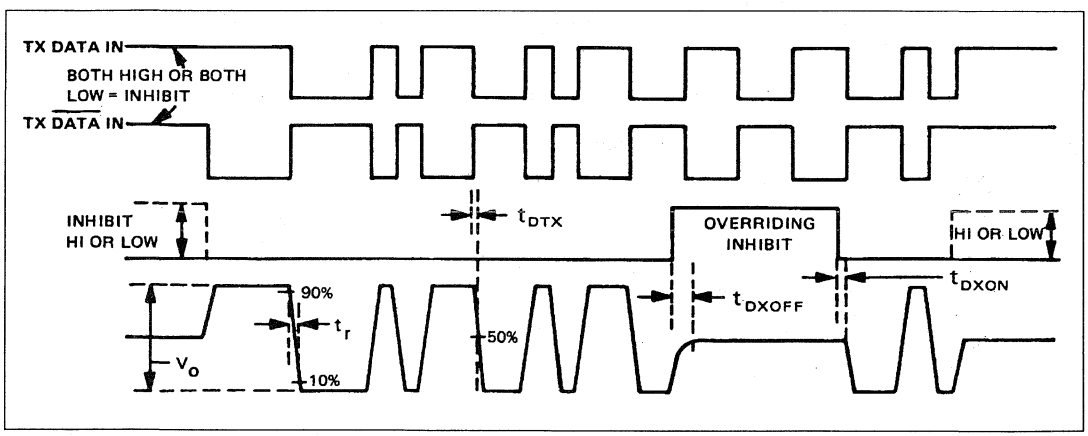
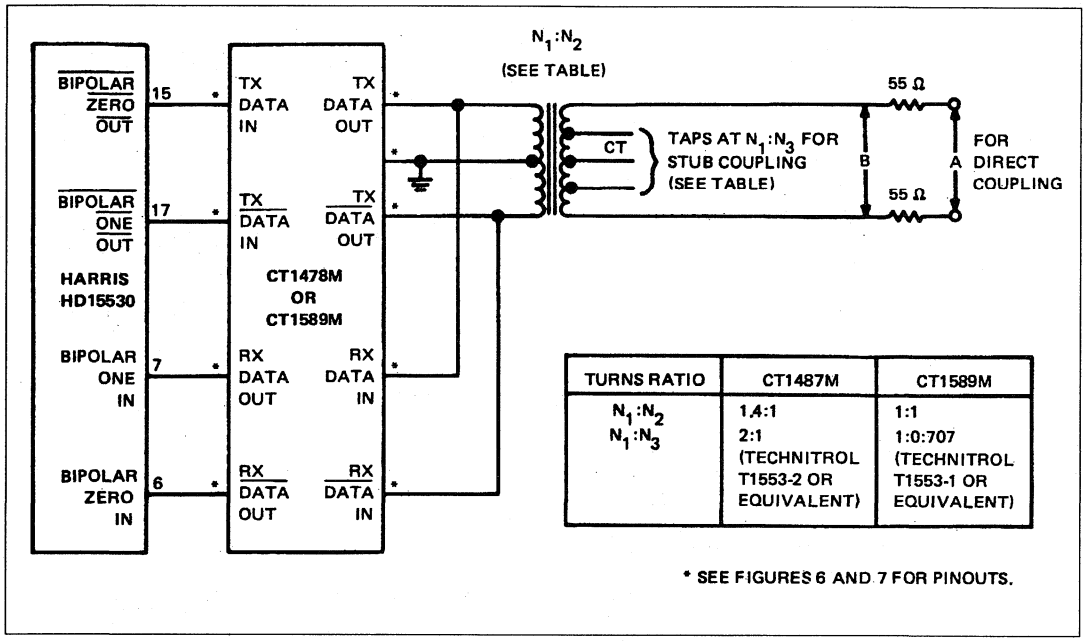


Figure 3: Driver Logic Waveforms



TURNS RATIO	CT1487M	CT1589M
$N_1:N_2$ $N_1:N_3$	1.4:1 2:1 (TECHNITROL T1553-2 OR EQUIVALENT)	1:1 1:0:707 (TECHNITROL T1553-1 OR EQUIVALENT)

Figure 4: Typical Input/Output Connections

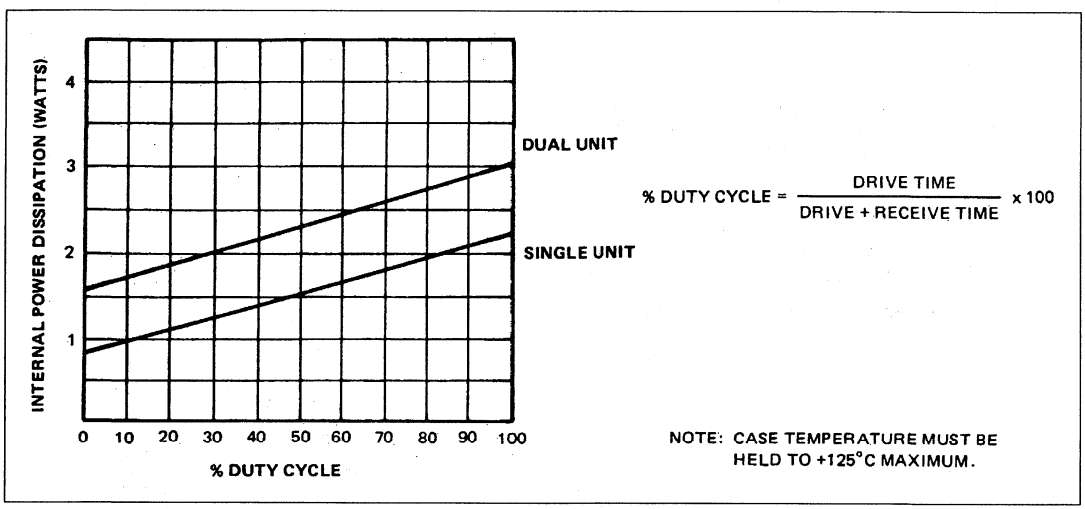


Figure 5: Typical Internal Power Dissipation (Total Hybrid)

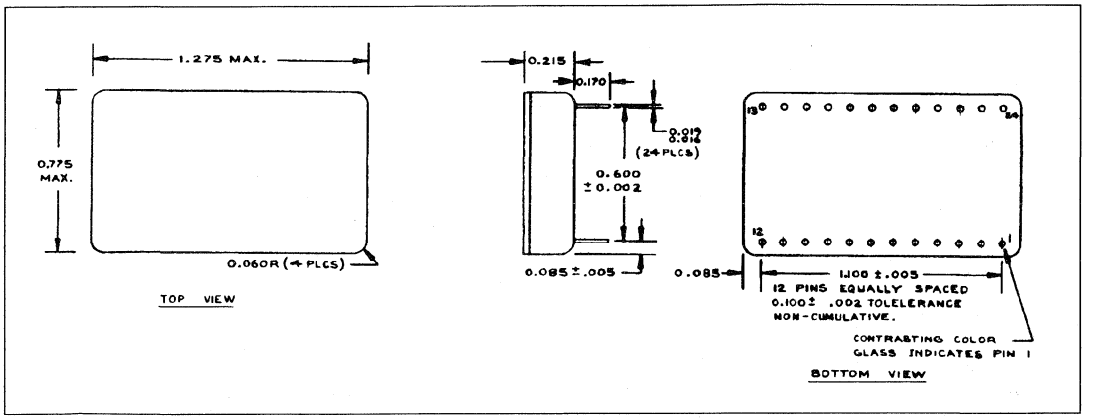
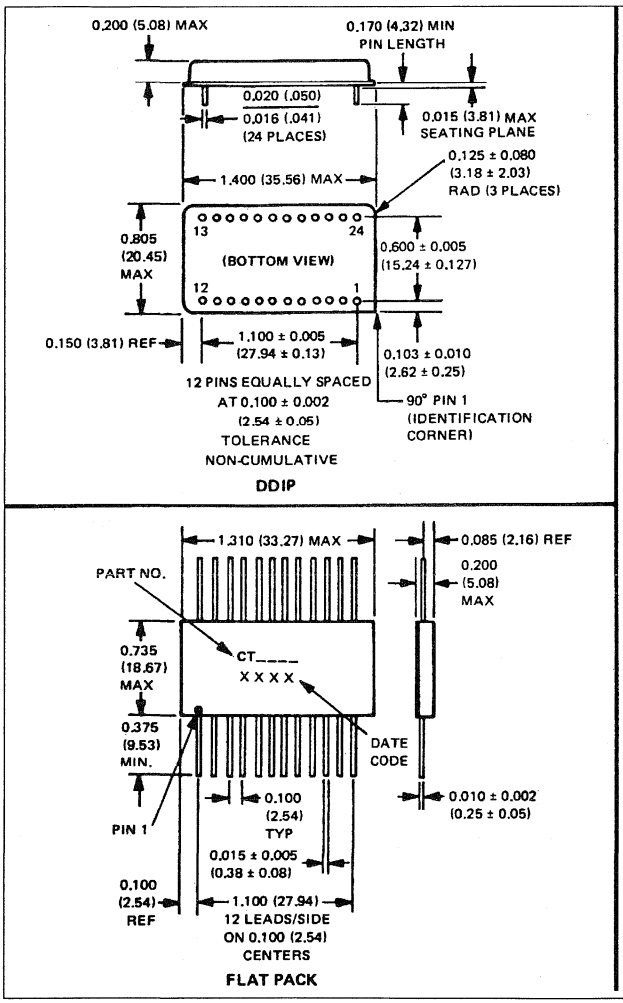


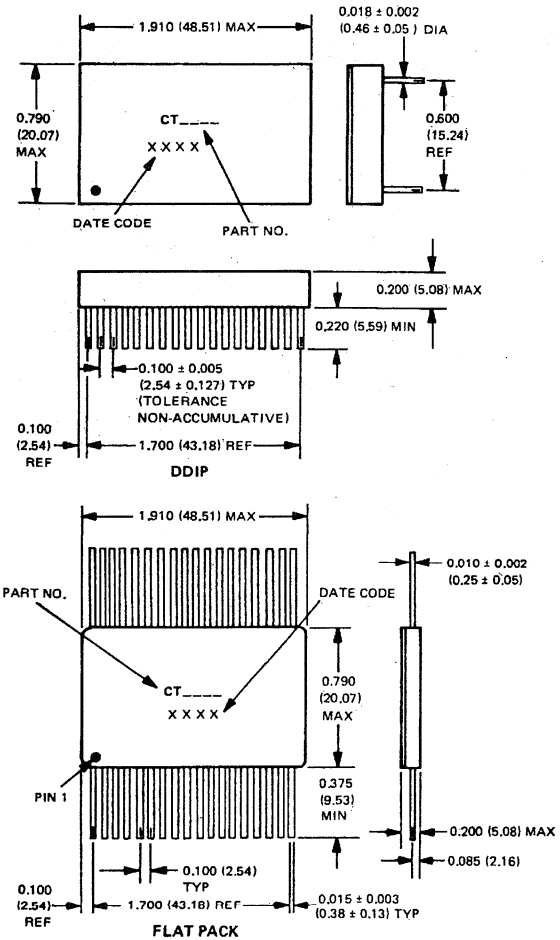
Figure 6: Mechanical Outline for the "MP" Package



SINGLE UNIT (DDIP AND FLAT PACK)			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA OUT	13	Vcc
2	TX DATA OUT	14	N.C.
3	GND	15	RX DATA IN
4	N.C.	16	RX DATA IN
5	N.C.	17	N.C.
6	N.C.	18	GND
7	RX DATA OUT	19	Vee
8	STROBE	20	+5 V
9	GND	21	TX INHIBIT
10	RX DATA OUT	22	TX DATA IN
11	N.C.	23	TX DATA IN
12	N.C.	24	N.C.

NOTES:
1. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
3. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
4. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E, METHOD 208C.

Figure 7: Mechanical Outline and Pinouts (Single Unit)



DUAL UNIT (DDIP AND FLAT PACK)		
PIN	FUNCTION	CHANNEL
1	TX DATA OUT	1
2	TX DATA OUT	1
3	GND	
4	N.C.	
5	RX DATA OUT	1
6	STROBE	1
7	GND	
8	RX DATA OUT	1
9	N.C.	
10	TX DATA OUT	2
11	TX DATA OUT	2
12	GND	2
13	N.C.	2
14	RX DATA OUT	2
15	STROBE	2
16	GND	2
17	RX DATA OUT	2
18	N.C.	
19	Vcc	2
20	RX DATA IN	2
21	RX DATA IN	2
22	GND	
23	Vee	2
24	+5 V	2
25	TX INHIBIT	2
26	TX DATA IN	2
27	TX DATA IN	2
28	Vcc	1
29	RX DATA IN	1
30	RX DATA IN	1
31	GND	
32	Vee	1
33	+5 V	1
34	TX INHIBIT	1
35	TX DATA IN	1
36	TX DATA IN	1

NOTES:
1. GND PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
4. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
5. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E, METHOD 208C.

Figure 8: Mechanical Outline and Pinouts (Dual Unit)

ORDERING INFORMATION

Some of these devices are available to Standard Military Drawings. Contact Customer Services at one of the addresses below for more information.

"Inverted Receiver Data Output" refers to the logic state of RX DATA OUT and RX $\overline{\text{DATA}}$ OUT when the bus is quiet. All part numbers with the "I" suffix produce logic "1" at the receiver outputs for quiet bus.

CT1487M	–	±15 V Single Unit Plug-in Package
CT1487MP	–	±15 V Single Unit Plug-in Package
CT1487MFP	–	±15 V Single Unit Flat Pack
CT1487MI	–	±15 V Single Unit Plug-in Package, Inverted Receiver Data Outputs
CT1487MIFP	–	±15 V Single Unit Flat Pack, Inverted Receiver Data Outputs
CT1487D	–	±15 V Dual Unit Plug-in Package
CT1487DI	–	±15 V Dual Unit Plug-in Package, Inverted Receiver Data Outputs
CT1487DFP	–	±15 V Dual Unit Flat Pack
CT1487DIFP	–	±15 V Dual Unit Flat Pack, Inverted Receiver Data Outputs
CT1589M	–	±12 V Single Unit Plug-in Package
CT1589MP	–	±12 V Single Unit Plug-in Package
CT1589MFP	–	±12 V Single Unit Flat Pack
CT1589MI	–	±12 V Single Unit Plug-in Package, Inverted Receiver Data Outputs
CT1589MIFP	–	±12 V Single Unit Flat Pack, Inverted Receiver Data Outputs
CT1589D	–	±12 V Dual Unit Plug-in Package
CT1589DI	–	±12 V Dual Unit Plug-in Package, Inverted Receiver Data Outputs
CT1589DFP	–	±12 V Dual Unit Flat Pack
CT1589DIFP	–	±12 V Dual Unit Flat Pack, Inverted Receiver Data Outputs

DS3180-1.2 November 1991

CT2520-23 Series

LOW POWER +5 VOLTS ONLY TRANSCEIVER FOR MIL-STD-1553B

GENERAL DESCRIPTION

The CT2520 + 5V only transceiver is a third generation hybrid device utilizing custom monolithic drivers and receivers. This allows the device to be operated from a single + 5V supply. This design results in lower power and 100% duty cycle is permissible at 125°C case temperature. Each driver dissipates less than 1.0 watt at 25% duty cycle.

FEATURES

- Monolithic +5V only drivers
- AC interstage coupling prevents static burnout
- Receiver filtered to improve S/N ratio of system
- 20mV typical output offset
- TTL compatible
- Available to Standard Military Drawings, please consult your nearest Customer Service Centre

TRANSCEIVER	TYPE	PACKAGE	NOTES
CT2520	DUAL	36PIN DIL OR FP	
CT2521	DUAL	36PIN DIL OR FP	1
CT2522	SINGLE	24PIN DIL OR FP	1
CT2523	SINGLE	44PIN LCC	

Note 1: PLUG IN PIN FOR PIN COMPATIBLE with Industry Standard Transceivers

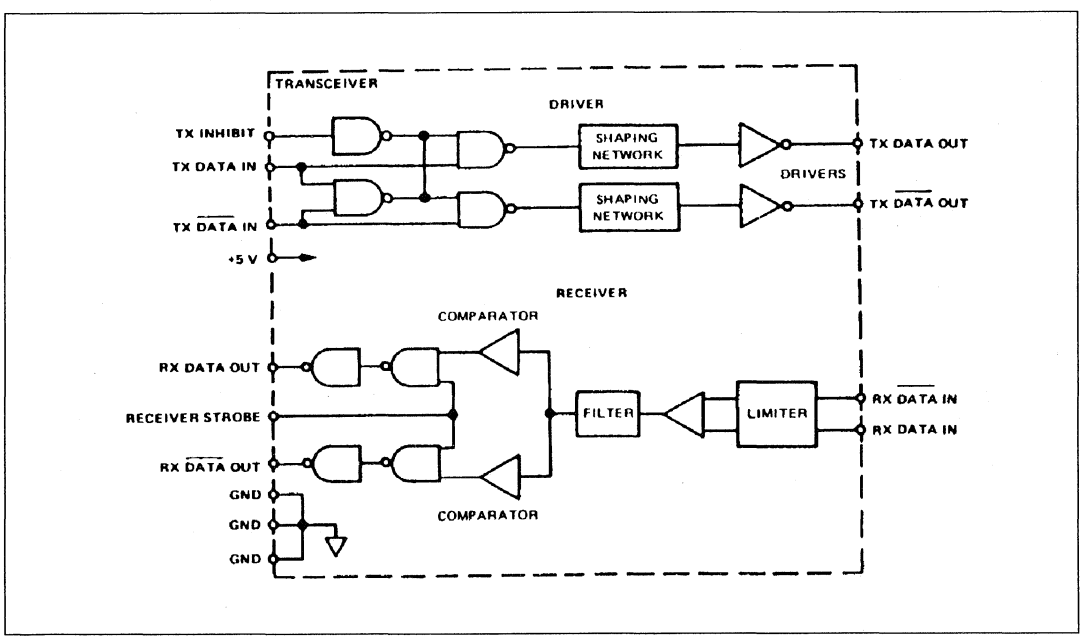


Figure 1: Functional Diagram

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION

PARAMETER / CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Differential Input/Output (Inhirited) Impedance DC to 1MHz, Total Hybrid	Z_{in}	3.5K			ohms
Differential voltage range	V_{idr}	±20V			V_{peak}
Input common mode voltage range	V_{icr}	±10V			V_{peak}
Common mode rejection ratio (from point A)	CMRR	40			dB
STROBE characteristics					
(Logic "0" inhibits output)					
"0" input current (V_S = 0.4V)	I_{il}			-1	mA
"1" input current (V_S = 2.7V)	I_{ih}			40	µA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Threshold characteristics (sine wave at 1 MHz)	V_{th1}	0.6		1.2	Vp-p
NOTE: Threshold voltages refer to point A.					
Filter characteristics 2MHz	V_{th2}	1.5		8	Vp-p
(sine wave input) 3MHz	V_{th3}	5			Vp-p
OUTPUT CHARACTERISTICS					
"1" state (I_{source} = 400µA)	V_{oh}	2.4	3.4		
"0" state (I_{sink} = 4mA)	V_{oh}			0.5	
NOTE: With receiver input below threshold both RX DATA OUT and RX $\overline{\text{DATA}}$ OUT remain in "0" state.					
Delay (average) from differential input zero crossings to RX DATA OUT and RX $\overline{\text{DATA}}$ OUT output 50% points	t_{DRX}		300	450	ns

ELECTRICAL CHARACTERISTICS, DRIVER SECTION

PARAMETER / CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
"0" input current (V_{in} = 0.4V)	I_{il}			-1	mA
"1" input current (V_{in} = 2.7V)	I_{ih}			40	µA
"0" input voltage	V_{il}			0.7	V
"1" input voltage	V_{ih}	2			V
Delay from TX INHIBIT (0 → 1) to inhibited output impedance	t_{DXOFF}		150	225	ns
Delay from TX INHIBIT (1 → 0) to active output impedance	t_{DXON}		100	150	ns
Differential output noise	V_{noi}			10	mVp-p
OUTPUT CHARACTERISTICS					
Differential output level at point 8, (145-ohm load)	V_O	25	27	35	Vp-p
Rise and fall times (10% - 90% of p-p output)	t_r	100	160	300	ns
Output offset at point A (35-ohm load) 2.5µs after mid-bit crossing of parity bit of last word of a 660µS message	V_{OS}		±20	±75	mV peak
Delay from 50% point of TX DATA IN or TX $\overline{\text{DATA}}$ IN to zero crossing of differential output	t_{DTX}		100	200	ns

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER / CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power supply voltages		V_{cc}	4.5	5.0	5.5	V
Power dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	CT2520 CT2521/2/3	P_c	Note 1		1500 250	mW mW
Thermal resistance, most critical device	CT2520 CT2521/2/3	θ_{jc}			10 60	°C/W °C/W
Junction to case temperature rise of most critical device at 100% duty cycle transmission	CT2520/1/2/3	T_{jc}			15	°C
Total supply current "standby" mode, or transmitting at less than 1% duty cycle (e.g. 20µs of transmission every 2ms or longer interval)		I_{cc}		55	70	mA
Total supply current transmitting at 1MHz into a 35-ohm load at point A	*DUTY CYCLE					
	25% 100%	$I_{cc}25$ $I_{cc}100$	Note 2 Note 2	150 430	180 550	mA mA
*One Channel Only						

Note 1: Decreases linearly to zero at zero duty cycle.
Note 2: Decreases linearly to applicable "stand by" value at zero duty cycle.

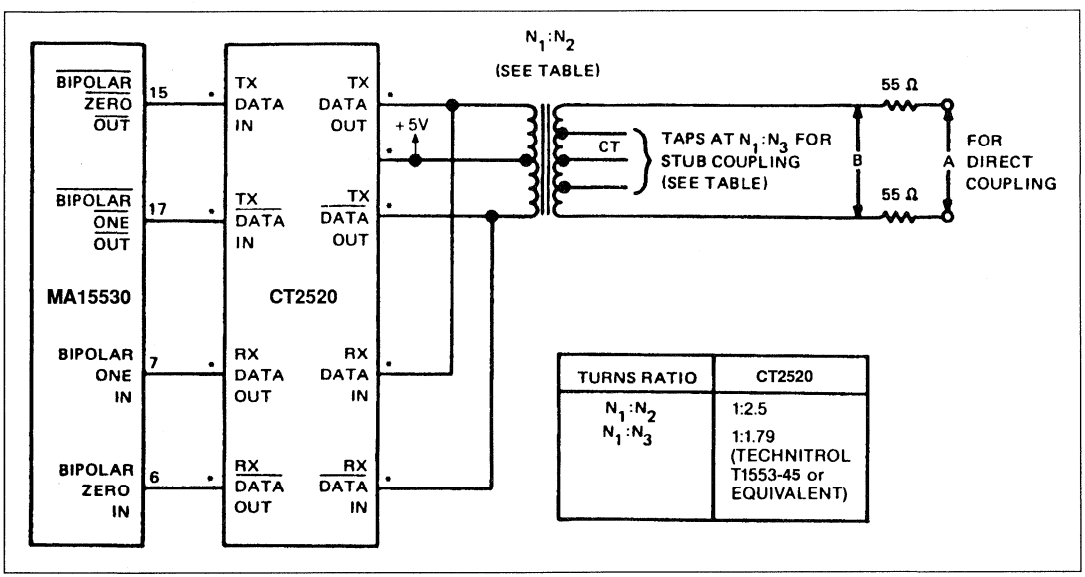


Figure 2: Typical Input/Output Connections - CT2520

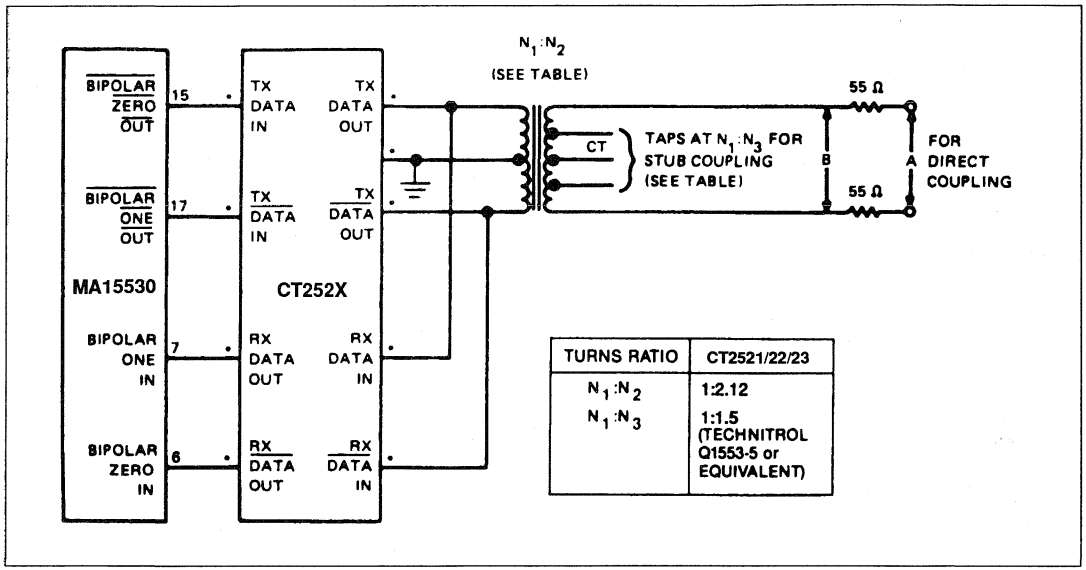
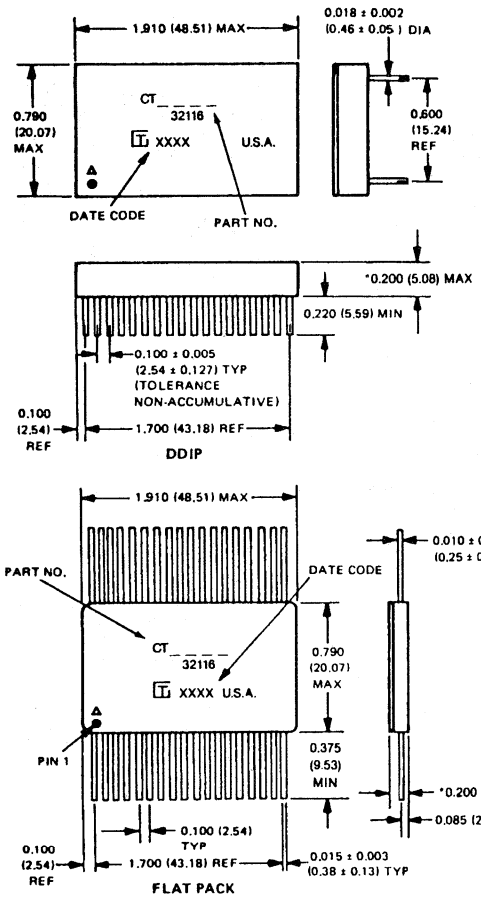


Figure 3: Typical Input/Output Connections - CT2521/22/23

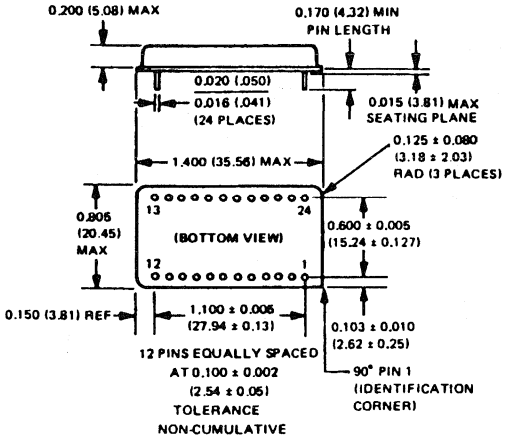


DUAL UNIT (DDIP AND FLAT PACK)		
PIN	FUNCTION	CHANNEL
1	TX DATA OUT	1
2	TX DATA OUT	1
3	GND	
4	N.C.	
5	RX DATA OUT	1
6	STROBE	1
7	GND	
8	RX DATA OUT	1
9	CASE GND	
10	TX DATA OUT	2
11	TX DATA OUT	2
12	GND	2
13	N.C.	2
14	RX DATA OUT	2
15	STROBE	2
16	GND	2
17	RX DATA OUT	2
18	N.C.	
19	N.C.	2
20	RX DATA IN	2
21	RX DATA IN	2
22	GND	
23	N.C.	2
24	+5 V	2
25	TX INHIBIT	2
26	TX DATA IN	2
27	TX DATA IN	2
28	N.C.	1
29	RX DATA IN	1
30	RX DATA IN	1
31	GND	
32	N.C.	1
33	+5 V	1
34	TX INHIBIT	1
35	TX DATA IN	1
36	TX DATA IN	1

NOTES:
1. GDN PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
4. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
5. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS MIL-STD-883, METHOD 2003.

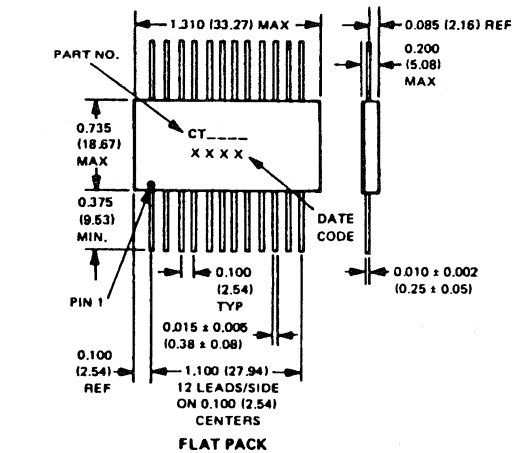
LOWER PACKAGES AVAILABLE, PLEASE CONTACT FACTORY.

Figure 4: Mechanical Outline and Pinouts (Dual Unit) CT2520/21



DDIP

SINGLE UNIT (DDIP AND FLAT PACK)			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA OUT	13	N.C.
2	TX DATA OUT	14	N.C.
3	GND	15	RX DATA IN
4	N.C.	16	RX DATA IN
5	N.C.	17	N.C.
6	N.C.	18	GND
7	RX DATA OUT	19	N.C.
8	STROBE	20	+5 V
9	GND	21	TX INHIBIT
10	RX DATA OUT	22	TX DATA IN
11	N.C.	23	TX DATA IN
12	N.C.	24	N.C.



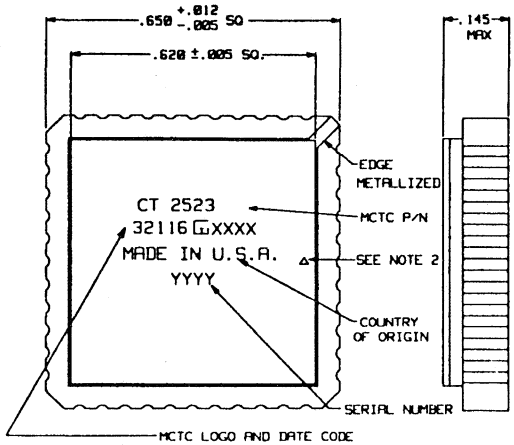
FLAT PACK

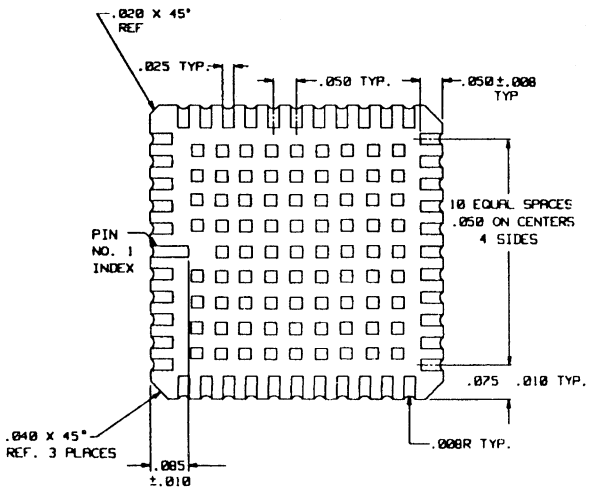
NOTES:
1. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
3. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
4. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS OF MIL-STD-202E. METHOD 208C.

NOTES:
1. GDN PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD INDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.
4. LEAD CLUSTER SHALL BE CENTERED WITHIN ±0.10 (2.54) OF OUTLINE DIMENSIONS. LEAD SPACING DIMENSIONS APPLY ONLY AT SEATING PLANE.
5. PIN MATERIAL MEETS SOLDERABILITY REQUIREMENTS MIL-STD-883, METHOD 2003.

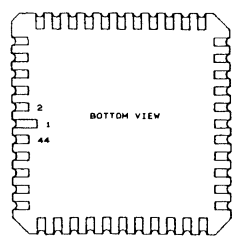
**LOWER PROFILE PACKAGES AVAILABLE, PLEASE CONTACT FACTORY.*

Figure 5: Mechanical Outline and Pinouts - CT2522





PIN	FUNCTION
1,2,3	VCC (+5V)
4,5,6	NC
7,8	TX DATA OUT
9,10	NC
11,12	TX $\overline{\text{DATA}}$ OUT
13	NC
14	ANALOG GND
15,16	DIGITAL GND
17	RX STROBE
18	RX DATA OUT
19,20	NC
21	RX $\overline{\text{DATA}}$ OUT
22,23,24	NC
25,26,27	NC
28	RX $\overline{\text{DATA}}$ IN
29	RX DATA IN
30,31,32	NC
33,34,35	NC
36	TX INHIBIT
37	TX DATA IN
38	TX $\overline{\text{DATA}}$ IN
39,40,41	ANALOG GND
42,43,44	VCC (+5V)



NOTES:
1. GDN PINS OF EACH SECTION SHOULD ALL BE CONNECTED EXTERNALLY.
2. DIMENSIONS SHOWN ARE IN INCHES (MILLIMETERS IN PARENTHESES).
3. LEAD INDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.

Figure 6: Mechanical Outline and Pinouts - CT2523

RECOMMENDED DESIGN PRACTICES

(a) DECOUPLING

Decouple V_{cc} to ground, close to the hybrid with a >10µF tantalum capacitor in parallel with a 100nF ceramic bypass capacitor.

Note: Peak transmission current drawn from Vcc is 650mA.

(b) PCB LAYOUT

- Full PCB ground - planning is recommended.
- It is good practice to ensure connections from encorder/decoder to 'TXLOGICIN', '$\overline{\text{TXLOGICIN}}$' and 'TXINHIBIT' are as short as possible and of balanced length, shape and area. Optimum results are obtained when these signals have minimum rise/fall times and minimum differential delays.
- Connections between '$\overline{\text{TXDATAOUT}}$' and the center tapped transformer should be designed to:
  (i) Withstand peak transmission currents at rquired operating duty cycles
  (ii) Minimise added series inductance
  (iii) Ensure system capacitance in conjunction with transceiver and transformer impedances does not reduce overall input impedance below the value stated in MIL-STD-1553B.

These connections should also be balanced in terms of length, shape and area.

3111-1.2 October 1991

CT3231M/MFP

LOW POWER DRIVER/RECEIVER FOR MIL-STD-1553

(Note: "M" designates monolithic devices used internally. Specifications also apply to the CT3231 and CT3231FP except as noted.)

FEATURES

- 1.5 Watt Total Hybrid Dissipation at 25% Transmitting Duty Cycle
- Meets MIL-STD-1553B
- TTL Compatible
- Meets MIL-STD-883 & MIL-M-38510
- Thick Film Hybrid Technology
- Driver/Receiver in a single Package for Space & Weight Savings
- Plug-In or Flat Pack Configuration
- Filtering on Receiver to Improve S/N Ratio of System

DRIVER DESCRIPTION

The CT3231M Driver section accepts complementary TTL Data at the input, and produces a 30 volt nominal peak-to-peak differential signal across a 140Ω load at the output. When coupled to the Data Bus with a 1:1 transformer, isolated on the Data Bus side with two 55.0 ohm fault isolation resistors, and loaded by two 70 ohm terminations plus additional receivers, the Data Bus signal produced is 7.2 volts nominal peak-to-peak.

When both "DATA" and "$\overline{\text{DATA}}$" inputs are held low or both are held high, the driver output becomes a high impedance and is "removed" from the line. In addition, an overriding "INHIBIT" input provides for removal of the Driver output from the line. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the Driver. See Driver Logic Waveforms, Figure 3.

DATA and $\overline{\text{DATA}}$ inputs must be complementary waveforms, of 50% duty cycle average, with no gate delays between them. It is recommended that those inputs be driven from a "D" type flip-flop.

RECEIVER DESCRIPTION

The CT3231M Receiver section accepts Bi-Phase Differential data at the input and produces two TTL signals at the output. The outputs are "DATA" and "$\overline{\text{DATA}}$", and represent positive and negative excursions (respectively) of the input beyond a predetermined threshold. See Receiver Logic Waveforms, Figure 2.

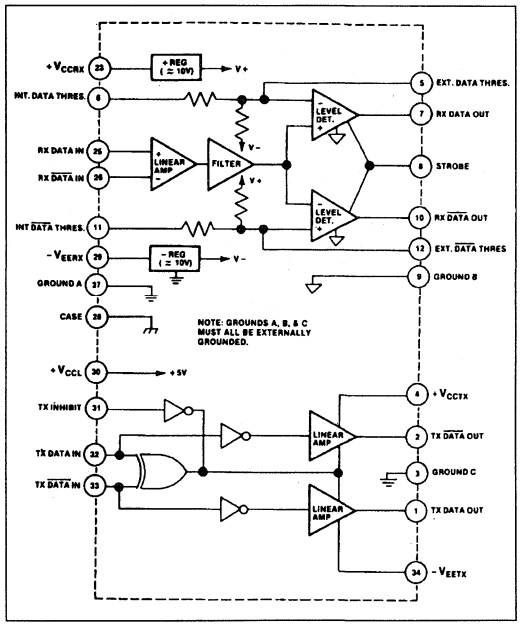


Figure 1: Functional Diagram and Pinouts

The positive and negative thresholds may be internally set by grounding the appropriate pins, or externally set with resistors. The pre-set internal thresholds will detect Data Bus signals exceeding 1 volt p-p and ignore signals less than 0.5 volt p-p when used with 1:1 transformer. (See Figure 4 for a suitable transformer and typical connection.)

A low level at the STROBE input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K ohm pull-up to +5V is recommended.

CT3231M SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Pin 4 or 23 ..... – 0.3 to + 18.0V
Supply Voltage, Pin 29 or 34 ..... + 0.3 to – 18.0V
Supply Voltage, Pin 30 ..... – 0.3 to + 7.0V
Logic Input Voltage, Pin 8, 31, 32, or 33 ..... – 0.3 to + 5.5V
Receiver Differential Input, Pin 25 to Pin 26 ..... ± 20 V (40 V p-p)
Receiver Input Voltage, Pin 25 or Pin 26 ..... ± 15 V
Driver Peak Output Current, Pin 1 or Pin 2 ..... ± 300 mA
Total Package Power Dissipation at (Ambient)T_A = + 25°C ..... 4.0 watts (Note 1)
(Derate above T_A = + 25°C at 40 mW/°C)
Power Dissipation at Specified Case Temperatures ..... See Figure 5
Operating Case Temperature Range (T_C) ..... – 55 to + 125°C
(See Figure 5 for limitations)

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges (V_{CCL} is common to both Driver and Receiver)		V_{CCRX} V_{EERX} V_{CCL}	+ 11.75 – 11.75 + 4.75		+ 15.75 – 15.75 + 5.25	V V V
Supply Current (I_{CCL} includes Driver and Receiver Together)		I_{CCRX} I_{EERX} I_{CCL}		25 30 35		mA mA mA
Differential Input Impedance	D.C. f = 1MHz	R_{IN} Z_{IN}	6K 4K			ohms ohms
Differential Voltage Range		V_{IDR}	± 20			V peak
Input Common Mode Voltage Range		V_{ICR}	± 10			V peak
Common Mode Rejection Ratio (From Point A, Fig. 4)		CMRR	40			dB
Strobe Characteristics (Logic "0" inhibits Output) "0" Input Current (V strobe = 0.5 V) "1" Input Current (V strobe = 2.7 V) "0" Input Voltage "1" Input Voltage Strobe Delay (turn-on or turn-off)		 I_{IL} I_{IH} V_{IL} V_{IH} t_{SD}	 2.0 	 6	 – 4 400 0.7 	 mA µA V V nS
Threshold Characteristics (Sinewave input, 100KHz to 1MHz) *Note: Threshold voltages are referred to the Input* Internal (Pin 6 & 11 grounded) External (Pin 6 & 11 open; threshold setting resistors from Pin 5 to ground & from Pin 12 to ground; R_{TH} Max = 10K ohms)		 V_{TH_1} R_{TH}/V_{TH_1}	 0.6 	 4000	 0.9 	 V p-p ohms/V p-p
Filter Characteristics (Pin 6 & 11 Grounded) (Sinewave input)	f = 2MHz f = 4MHz	V_{TH_2} V_{TH_3}	0.8 4.2		1.5 8.5	V p-p V p-p
Output Characteristics, RX Data & $\overline{\text{Data}}$ "1" State (I_{SOURCE} = – 0.4 ma) Note 2 "0" State (I_{SINK} = 4 ma) Note 2 *Note: With Receiver input below threshold, both RX Data & RX $\overline{\text{Data}}$ outputs remain in "1" state.* Delay (average) from differential input zero crossings to RX Data & RX $\overline{\text{Data}}$ output 50% points.		 V_{OH} V_{OL} t_{DRX}	 2.5 	 3.3 190	 0.5 450	 V V nS

Note 1: *Assumes unit in free air (natural convection cooling).*

Note 2: *For CT3231/CT3231FP ONLY, "1" state (I_{SOURCE} = –1 ma), "0" state (I_{SINK} = 10 ma).*

ELECTRICAL CHARACTERISTICS, DRIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges (See Receiver Section for V_{CCL})		V_{CCTX} V_{EETX}	+ 11.75 − 11.75		+ 15.75 − 15.75	V V
Supply Current, "Standby" mode (see Receiver Section for I_{CCL}) (TX Inhibit high; or TX Data & TX $\overline{\text{Data}}$ both high or both low)		I_{CCTXS} I_{EETXS}		12 0	Note 2 1	mA mA
Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4	DUTY CYCLE 25%	I_{CCX25} I_{EEX25}	Note 4 Note 3	45 35	Note 2 Note 2	mA mA
(I_{CCL} limits do not change with mode of operation or duty cycle	100%	I_{CCTX} I_{EETX}	Note 4 Note 3	150 135	Note 2 Note 2	mA mA
Input Characteristics, TX Data in or TX $\overline{\text{Data}}$ in "0" Input Current (V_{IN} = 0.4 V) "1" Input Current (V_{IN} = 2.7 V) "0" Input Voltage "1" Input Voltage		 I_{ILD} I_{IHD} V_{ILD} V_{IHD}	 2.0	 	 − 1.2 100 0.7 	 mA µA V V
Inhibit Characteristic "0" Input Current (V_{IN} = 0.4 V) "1" Input Current (V_{IN} = 2.7 V) "0" Input Voltage "1" Input Voltage Delay from TX $\overline{\text{Inhibit}}$ (0→1) to inhibited output impedance Delay from TX $\overline{\text{Inhibit}}$ (1→0) to active output impedance Differential output noise, inhibit mode Differential output impedance (inhibited) at 1MHz		 I_{ILI} I_{IHI} V_{ILI} V_{IHI} t_{DXOFF} t_{DXON} V_{NOI} Z_{OI}	 2.0 10K	 300 100 	 − 0.8 50 0.7 400 250 10 	 mA µA V V nS nS mVp-p ohms
Output Characteristics (Figure 3) Differential output level (140 ohm load) Differential Active output impedance at 1MHz Rise and Fall times (10% to 90% of p-p output) Output offset at point A in Fig. 4 (35 ohm load) 2.5 µS after mid-bit crossing of the parity bit of the last word of a 660 µS message Delay from 50% point of TX Data or TX $\overline{\text{Data}}$ input to zero crossing of differential output		 V_O Z_{OA} t_r V_{OS} t_{DTX}	 26 100 	 30 4 150 ± 20 100	 35 300 ± 75 250	 V p-p ohms nS mV peak nS

Note 2: *Maximum supply currents for driver and receiver combined are included in power and thermal data table.*

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Total Supply Current, "Standby" mode or transmitting at less than 1% duty cycle (e.g. 20 µS of transmission every 2mS or longer interval)		I_{CCS} I_{EES} I_{CCL}		40 30 35	50 40 45	mA mA mA
Total Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4	DUTY CYCLE 25%	I_{CC25} I_{EE25}	Note 4 Note 4	70 65	80 75	mA mA
(I_{CCL} limits do not change with mode of operation or duty cycle)	100%	I_{CC100} I_{EE100}	Note 4 Note 4	175 165	190 180	mA mA
Power Dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	SUPPLY VOLTAGE ± 12 V ± 15 V	P_{C12} P_{C15}	Note 3 Note 3	300 450	400 600	mW mW
Thermal Resistance, junction-to-case, of most critical device		$Ø_{JC}$		80	100	°C/W
Allowable transmitting duty cycle when case is held to + 100°C maximum		Note 5			100	%
Allowable transmitting duty cycle when case is held to + 125°C maximum	± 12 V supplies ± 15 V supplies	Note 5 Note 5			80 55	% %

Note 3: *Decreases linearly to zero at zero duty cycle.*

Note 4: *Decreases linearly to applicable "Standby" value at zero duty cycle.*

Note 5: *Based upon operating junction temperature of 160°C for hottest device. For lower operating junction temperatures, reduce maximum duty cycle accordingly.*

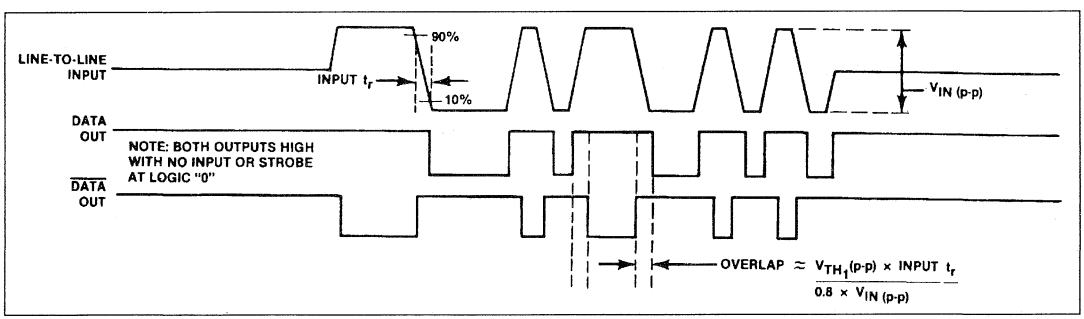


Figure 2: Receiver Logic Waveforms

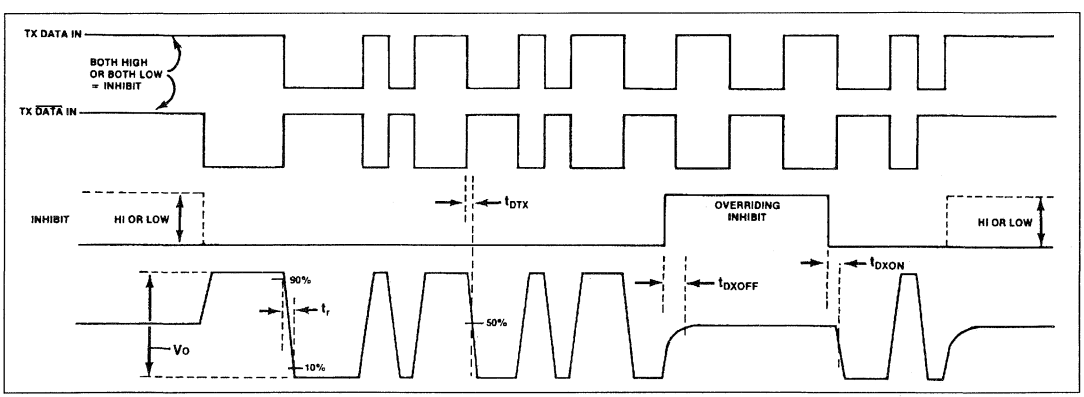


Figure 3: Driver Logic Waveforms

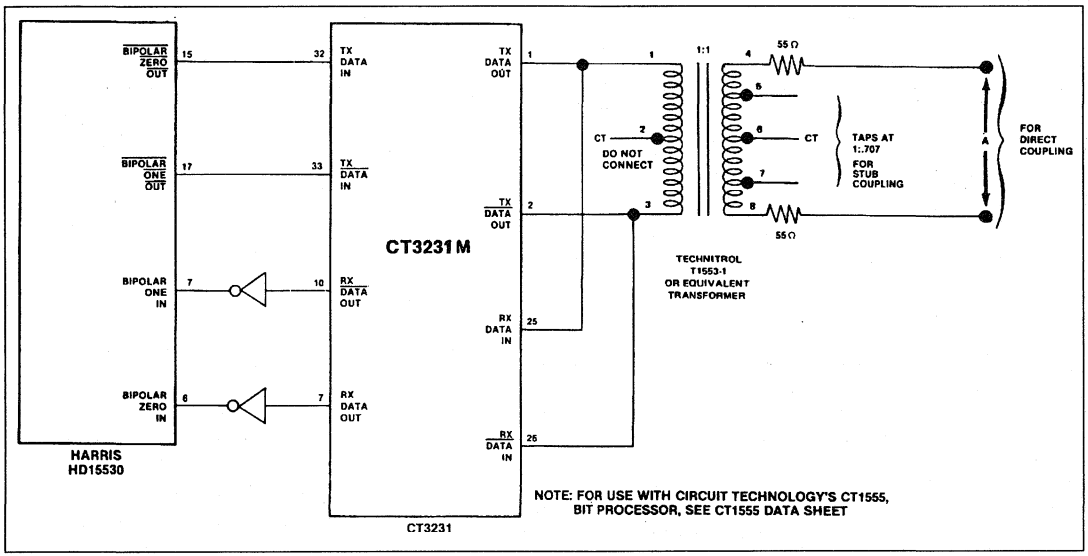
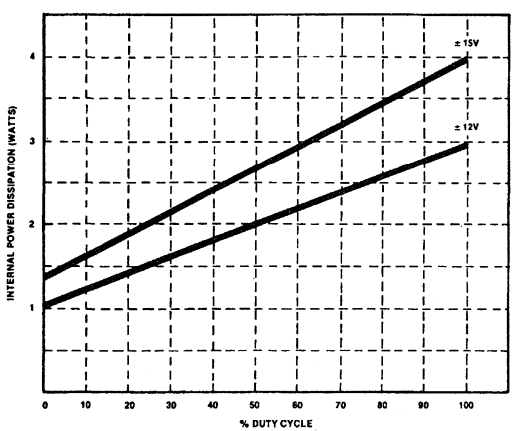


Figure 4: Typical Input/Output Connections



$$\% \text{ DUTY CYCLE} = \frac{\text{TRANSMIT TIME}}{\text{TRANSMIT \& RECEIVE TIME}} \times 100$$

NOTE: CASE TEMPERATURE MUST BE HELD TO + 100°C MAXIMUM FOR 100% DUTY CYCLE. FOR OPERATION AT CASE TEMPERATURE OF + 125°C, SEE "POWER AND THERMAL DATA"

Figure 5: Typical Power Dissipation (Total Hybrid)

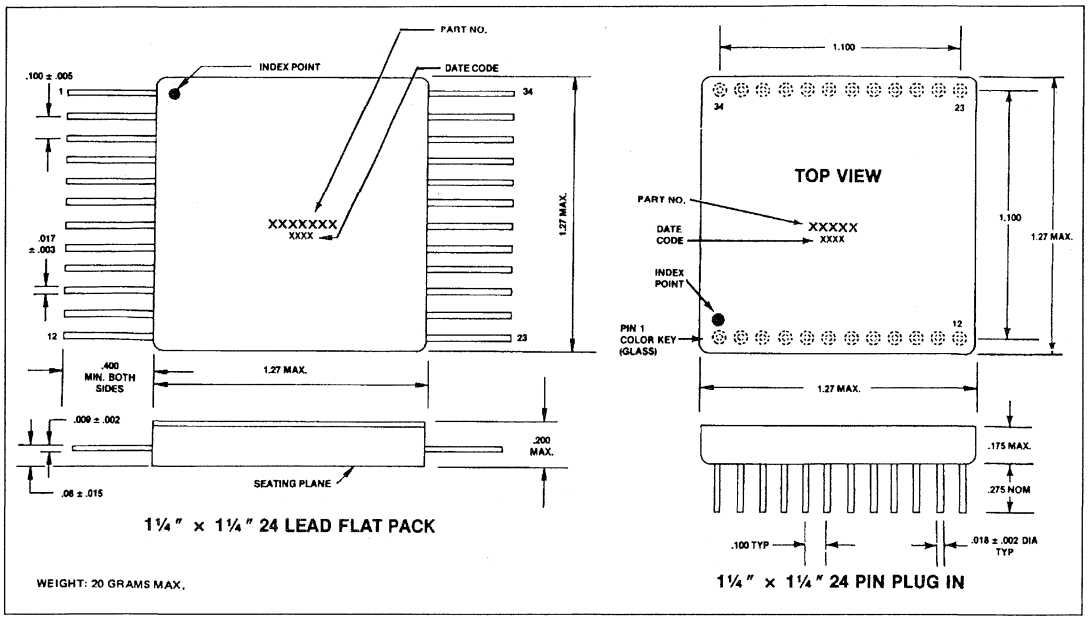


Figure 6. Package outline drawings

DS3110-1.3 October 1991

CT3232M/MFP

LOW POWER DRIVER/RECEIVER FOR MIL-STD-1553 & MACAIR

(Note: "M" designates monolithic devices used internally. Specifications also apply to the CT3232 and CT3232FP except as noted.)

FEATURES

- 1.5 Watt Total Hybrid Dissipation at 25% Transmitting Duty Cycle
- Compatible with MIL-STD-1553A/B & MACAIR A3818, A5232, A5690 & A4905
- Thick Film Hybrid Technology
- Driver/Receiver in a single Package for Space & Weight Savings
- Plug-In or Flat Pack Configuration
- Filtering on Receiver to Improve S/N Ratio of System
- Pin for pin interchangeable with CT3231 Series

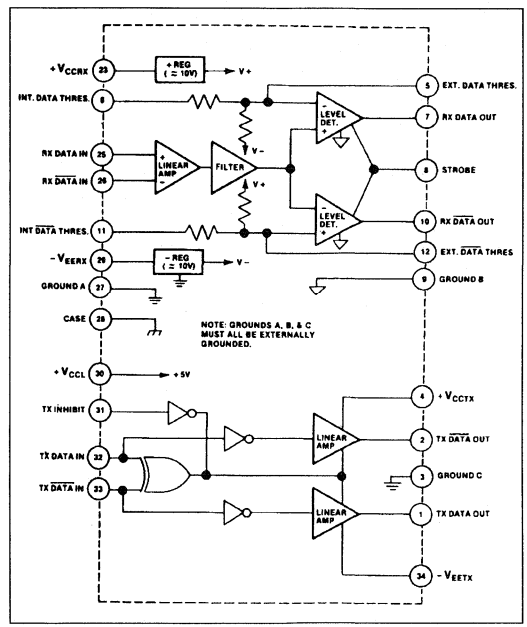


Figure 1: Functional Diagram and Pinouts

DRIVER DESCRIPTION

The CT3232M Driver section accepts complementary TTL Data at the input, and produces a 30 volt nominal peak-to-peak differential signal across a 140Ω load at the output. When coupled to the Data Bus with a 1:1 transformer, isolated on the Data Bus side with two 55.0 ohm fault isolation resistors, and loaded by two 70 ohm terminations plus additional receivers, the Data Bus signal produced is 7.2 volts nominal peak-to-peak.

When both "DATA" and "$\overline{\text{DATA}}$" inputs are held low or both are held high, the driver output becomes a high impedance and is "removed" from the line. In addition, an overriding "INHIBIT" input provides for removal of the Driver output from the line. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the Driver. See Driver Logic Waveforms, Figure 3.

DATA and $\overline{\text{DATA}}$ inputs must be complementary waveforms, of 50% duty cycle average, with no gate delays between them.

RECEIVER DESCRIPTION

The CT3232M Receiver section accepts Bi-Phase Differential data at the input and produces two TTL signals at the output. The outputs are "DATA" and "$\overline{\text{DATA}}$", and represent positive and negative excursions (respectively) of the input beyond a predetermined threshold. See Receiver Logic Waveforms, Figure 2.

The positive and negative thresholds may be internally set by grounding the appropriate pins, or externally set with resistors. The pre-set internal thresholds will detect Data Bus signals exceeding 1 volt p-p and ignore signals less than 0.5 volt p-p when used with 1:1 transformer. (See Figure 4 for a suitable transformer and typical connection.)

A low level at the STROBE input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K ohm pull-up to +5V is recommended.

CT3232M SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Pin 4 or 23 ..... – 0.3 to + 18.0V
Supply Voltage, Pin 29 or 34 ..... + 0.3 to – 18.0V
Supply Voltage, Pin 30 ..... – 0.3 to + 7.0V
Logic Input Voltage, Pin 8, 31, 32, or 33 ..... – 0.3 to + 5.50V
Receiver Differential Input, Pin 25 to Pin 26 ..... ± 20 V (40 V p-p)
Receiver Input Voltage, Pin 25 or Pin 26 ..... ± 15 V
Driver Peak Output Current, Pin 1 or Pin 2 ..... ± 300 mA
Total Package Power Dissipation at (Ambient) T_A = + 25°C ..... 4.0 watts (Note 1)
(Derate above T_A = + 25°C at 40 mW/°C)
Power Dissipation at Specified Case Temperatures ..... See Figure 5
Operating Case Temperature Range (T_C) ..... – 55 to + 125°C
(See Figure 5 for limitations)

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges (V_{CCL} is common to both Driver and Receiver)		V_{CCRX} V_{EERX} V_{CCL}	+ 11.75 – 11.75 + 4.75		+ 15.75 – 15.75 + 5.25	V V V
Supply Current (I_{CCL} includes Driver and Receiver Together)		I_{CCRX} I_{EERX} I_{CCL}		25 30 35		mA mA mA
Differential Input Impedance	f = 1MHz	Z_{IN}	9K			ohms
Differential Voltage Range		V_{IDR}	± 20			V peak
Input Common Mode Voltage Range		V_{ICR}	± 10			V peak
Common Mode Rejection Ratio (From Point A, Fig. 4)		CMRR	40			dB
Strobe Characteristics (Logic "0" inhibits Output) "0" Input Current (V strobe = 0.5 V) "1" Input Current (V strobe = 2.7 V) "0" Input Voltage "1" Input Voltage Strobe Delay (turn-on or turn-off)		 I_{IL} I_{IH} V_{IL} V_{IH} t_{SD}	 2.0 	 20	 – 4 400 0.7 	 mA µA V V nS
Threshold Characteristics (Sinewave input, 100KHz to 1MHz) *Note: Threshold voltages are referred to the Input* Internal (Pin 6 & 11 grounded) External (Pin 6 & 11 open; threshold setting resistors from Pin 5 to ground & from Pin 12 to ground; R_{TH} Max = 10K ohms)		 V_{TH_1} R_{TH}/V_{TH_1}	 0.6 	 4000	 1.0 	 V p-p ohms/V p-p
Filter Characteristics (Pin 6 & 11 Grounded) (Sinewave input)	f = 2MHz f = 3MHz	V_{TH_2} V_{TH_3}	1.0 3.0		3.0	V p-p V p-p
Output Characteristics, RX Data & $\overline{\text{Data}}$ "1" State (I_{SOURCE} = – 0.4 ma) Note 2 "0" State (I_{SINK} = 4 ma) Note 2 *Note: With Receiver input below threshold, both RX Data & RX $\overline{\text{Data}}$ outputs remain in "1" state.* Delay (average) from differential input zero crossings to RX Data & RX $\overline{\text{Data}}$ output 50% points.		 V_{OH} V_{OL} t_{DRX}	 2.5 	 3.3 290	 0.5 450	 V V nS

Note 1: *Assumes unit in free air (natural convection cooling).*

Note 2: *For CT3232/CT3232FP ONLY, "1" state (I_{SOURCE} = 1 ma), "0" state (I_{SINK} = 10 ma).*

ELECTRICAL CHARACTERISTICS, DRIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges (See Receiver Section for V_{CCL})		V_{CCTX} V_{EETX}	+ 11.75 − 11.75		+ 15.75 − 15.75	V V
Supply Current, "Standby" mode (see Receiver Section for I_{CCL}) (TX Inhibit high; or TX Data & TX $\overline{\text{Data}}$ both high or both low)		I_{CCTXS} I_{EETXS}		12 0	Note 2 1	mA mA
Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4	DUTY CYCLE					
	25%	I_{CCX25} I_{EEX25}	Note 4 Note 3	45 35	Note 2 Note 2	mA mA
(I_{CCL} limits do not change with mode of operation or duty cycle	100%	I_{CCTX} I_{EETX}	Note 4 Note 3	150 135	Note 2 Note 2	mA mA
Input Characteristics, TX Data in or TX $\overline{\text{Data}}$ in						
"0" Input Current (V_{IN} = 0.4 V)		I_{ILD}			− 1.2	mA
"1" Input Current (V_{IN} = 2.7 V)		I_{IHD}			100	µA
"0" Input Voltage		V_{ILD}			0.7	V
"1" Input Voltage		V_{IHD}	2.0			V
Inhibit Characteristic						
"0" Input Current (V_{IN} = 0.4 V)		I_{ILI}			− 0.8	mA
"1" Input Current (V_{IN} = 2.7 V)		I_{IHI}			50	µA
"0" Input Voltage		V_{ILI}			0.7	V
"1" Input Voltage		V_{IHI}	2.0			V
Delay from TX $\overline{\text{Inhibit}}$ (0→1) to inhibited output impedance		t_{DXOFF}		300	450	nS
Delay from TX $\overline{\text{Inhibit}}$ (0→1) to inhibited output impedance		t_{DXON}		100	350	nS
Differential output noise, inhibit mode		V_{NOI}			10	mVp-p
Differential output impedance (inhibited) at 1MHz		Z_{OI}	10K			ohms
Output Characteristics (Figure 3)						
Differential output level (open circuit)		V_O	28	32	35	V p-p
Differential Active output impedance at 1MHz		Z_{OA}			10	ohms
Rise and Fall times (10% to 90% of p-p output)		t_r	200		300	nS
Output offset at point A in Fig. 4 (35 ohm load) 2.5 µS after mid-bit crossing of the parity bit of the last word of a 660 µS message		V_{OS}		± 20	± 75	mV peak
Delay from 50% point of TX Data or TX $\overline{\text{Data}}$ input to zero crossing of differential output		t_{DTX}		220	350	nS

Note 2: *Maximum supply currents for driver and receiver combined are included in power and thermal data table.*

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Total Supply Current, "Standby" mode or transmitting at less than 1% duty cycle (e.g. 20 µS of transmission every 2mS or longer interval)		I_{CCS} I_{EES} I_{CCL}		40 30 35	50 40 45	mA mA mA
Total Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4	DUTY CYCLE 25%	I_{CC25} I_{EE25}	Note 4 Note 4	70 65	80 75	mA mA
(I_{CCL} limits do not change with mode of operation or duty cycle)	100%	I_{CC100} I_{EE100}	Note 4 Note 4	175 165	190 180	mA mA
Power Dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	SUPPLY VOLTAGE ± 12 V ± 15 V	P_{C12} P_{C15}	Note 3 Note 3	300 450	400 600	mW mW
Thermal Resistance, junction-to-case, of most critical device		$Ø_{JC}$		80	100	°C/W
Allowable transmitting duty cycle when case is held to + 100°C maximum		Note 5			100	%
Allowable transmitting duty cycle when case is held to + 125°C maximum	± 12 V supplies ± 15 V supplies	Note 5 Note 5			80 55	% %

Note 3: *Decreases linearly to zero at zero duty cycle.*

Note 4: *Decreases linearly to applicable "Standby" value at zero duty cycle.*

Note 5: *Based upon operating junction temperature of 160°C for hottest device. For lower operating junction temperatures, reduce maximum duty cycle accordingly.*

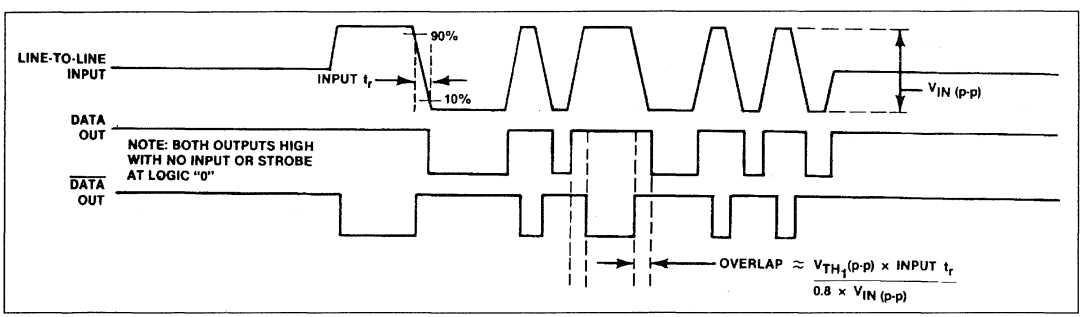


Figure 2: Receiver Logic Waveforms

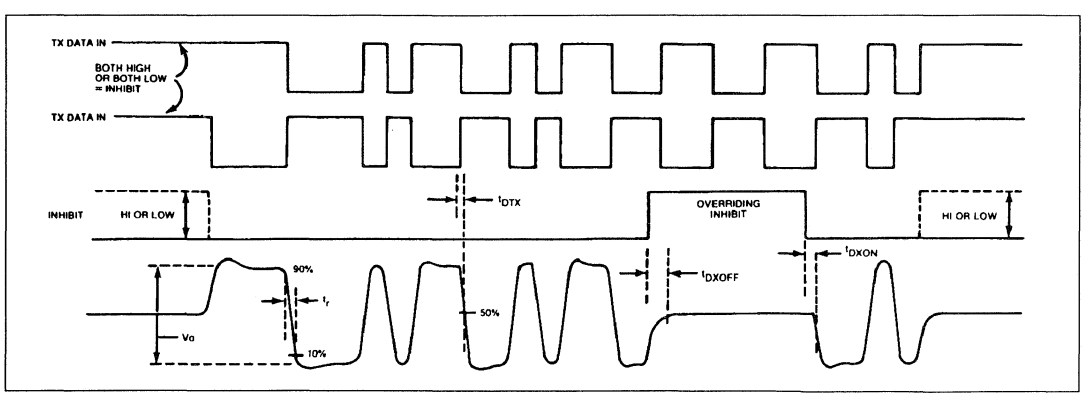


Figure 3: Driver Logic Waveforms

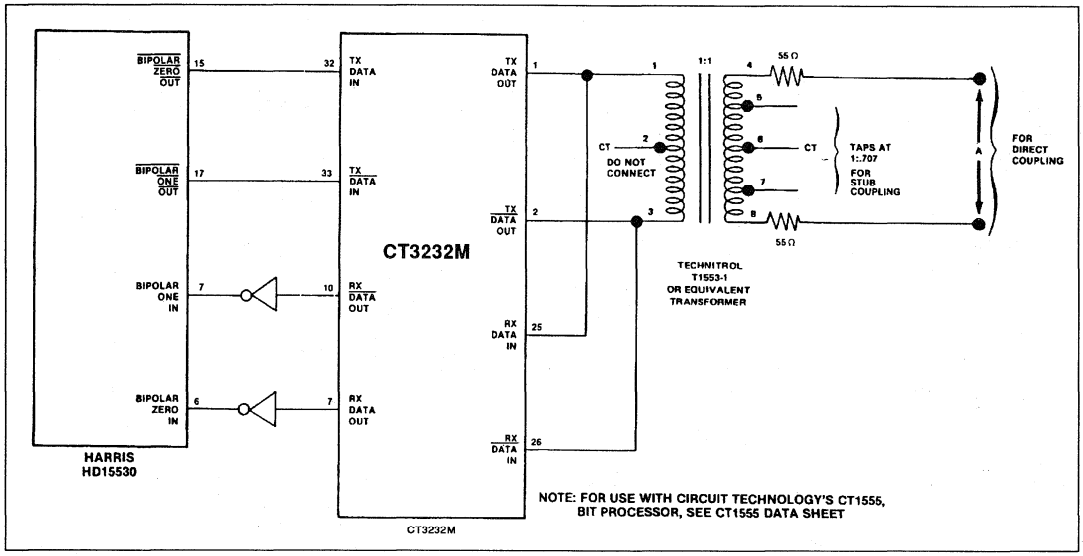
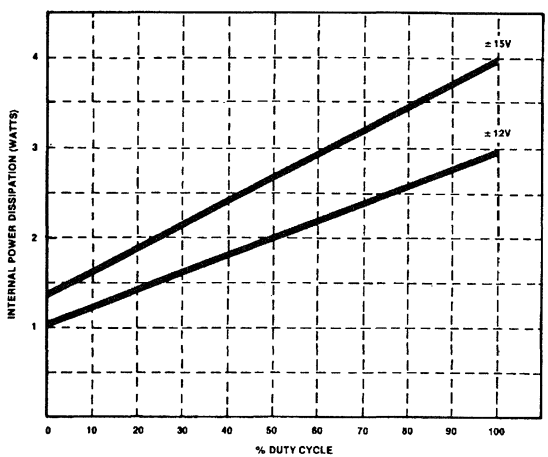


Figure 4: Typical Input/Output Connections



$$\% \text{ DUTY CYCLE} = \frac{\text{TRANSMIT TIME}}{\text{TRANSMIT \& RECEIVE TIME}} \times 100$$

NOTE: CASE TEMPERATURE MUST BE HELD TO + 100°C MAXIMUM FOR 100% DUTY CYCLE. FOR OPERATION AT CASE TEMPERATURE OF + 125°C, SEE "POWER AND THERMAL DATA"

Figure 5: Typical Power Dissipation (Total Hybrid)

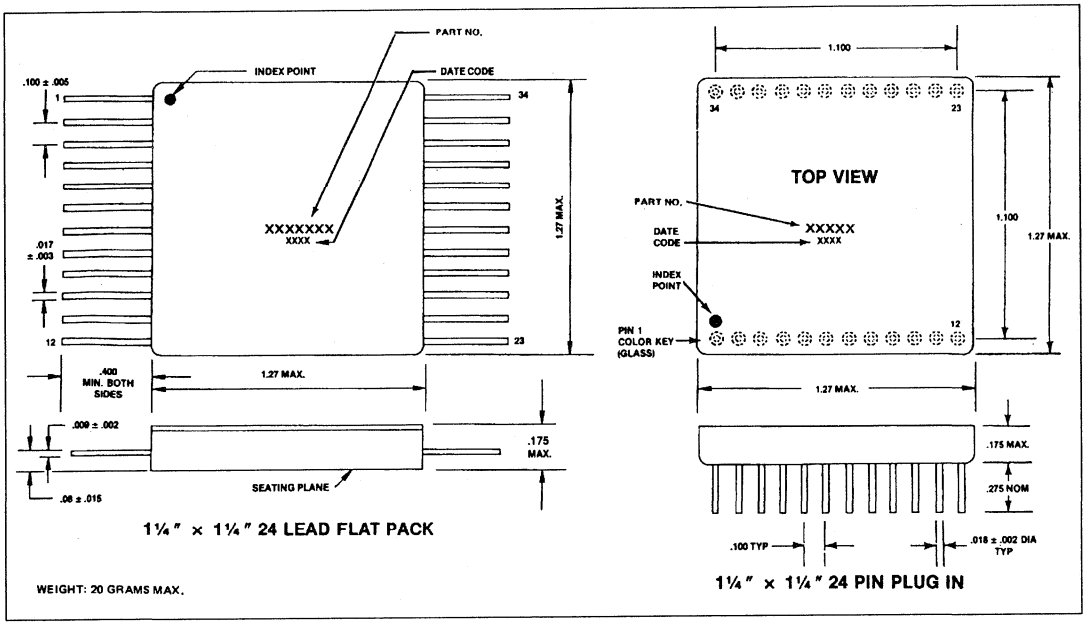


Figure 6: Package Outline Drawings

Section 3
Transceiver/Protocol

3074-1.2 December 1991

CT2512

MIL-STD-1553B DUAL REDUNDANT REMOTE TERMINAL HYBRID UNIT

The CT2512 contains 2 transceivers, 2 encoder/decoders, bit processors and complete Remote Terminal (RT) logic. The device is constructed using Marconi's advanced VLSI custom chip and hybrid technology. It functions as a complete dual redundant MIL-STD1553B RT Unit supporting all 13 mode codes for dual redundant operation.

The CT2512 is a pin-for-pin functional equivalent of the DDC BUS-65112 and performs parallel data transfers with a DMA type handshake. Multiple error flag outputs and host access to many of the RT Status Word bits are just some of the features that make this part ideal for many RT applications. The unit has an operating range of -55°C to + 125°C.

GPS (Farmingdale) is a MIL-STD-1772 Certified Manufacturer.

FEATURES

- Replaces DDC BUS-65112 / BUS-65117 (Flatpack Version)
- Functions as a Complete Remote Terminal Unit
- Supports 13 Mode Codes, Illegalization of Codes Allowed
- Transfers Data with DMA Type Handshaking
- Latched Outputs for Command Word and Word Count
- 14 Bit Built-In-Test Word Register
- 4 Error Flag Outputs
- Advanced Low Power VLSI Technology

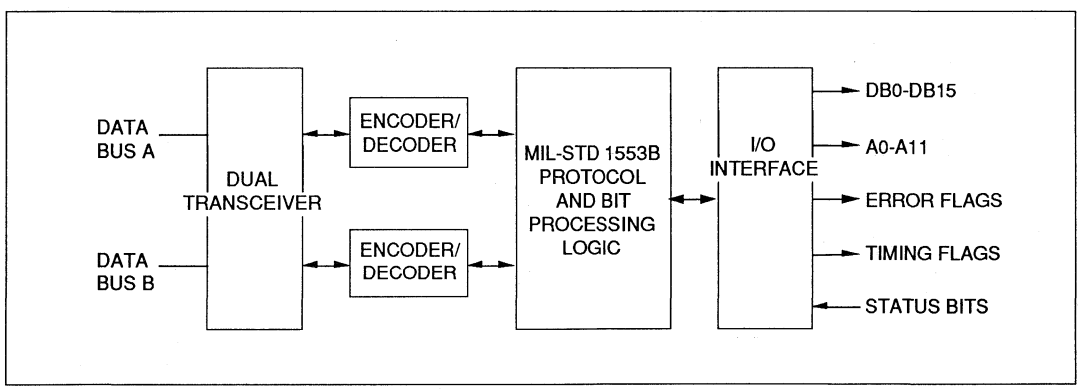


Figure 1: Functional Diagram - CT2512

ABSOLUTE MAXIMUM RATINGS	LIMITS
Power Supply Voltage (V_{CC}) (Pins 18, 76)	-0.3V to +18.0V
Power Supply Voltage (V_{EE}) (Pins 38, 57)	+0.3V to -18.0V
Power Supply Voltage (V_{CCL}) (Pins 37, 58 / 51)	-0.3V to +7.0V
Receiver Differential Input (Pins 20, 59 / 74, 36)	+/-20V (40v p-p)
Receiver Input Voltage (Pins 20, 59 /74, 36)	+/-15V
Driver Output Current (Pins 56, 17 / 39, 77)	+200ma
Transmission Duty Cycle at T_c = 125°C	100%
Operating Case Temperature Range (T_c)	-55° to +125°C

Figure 2: CT2512 Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltages	V_{CC} V_{EE} V_{CCL}	14.25 -14.25 45	15 -15 5	15.75 -15.75 5.5	V V V
Power Dissipation of most critical (hottest) device in hybrid during continuous transmission (100% Duty Cycle)	P_c	Note 1	350	500	mW
Thermal Resistance, most critical device	$ø_{jc}$		60		deg C/W
Junction to case temperature rise of most critical device at 100% duty cycle	T_{jc}		30		deg C
Total supply current 'standby' mode, or transmitting at less than 1% duty cycle (e.g. 20us of transmission every 2ms or longer interval)	I_{CC} I_{EE} I_{CCl}	 Note 2 Note 2	30 50 90	44 70 130	mA mA mA
Total supply current transmitting at 1 Mhz into a 35-ohm load at point A in Figure 2	I_{CC} @ 25% I_{CC} @ 100%	Note 3 Note 3	70 200	100 260	mA mA

Note 1: Decreases linearly to zero at zero duty cycle.
Note 2: I_{EE} limit does not change with mode of operation or duty cycle.
Note 3: Decreases linearly to applicable "standby" values at zero duty cycle.

Figure 3: Power and Thermal Data (Transceiver and Logic Sections)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Differential input impedance DC to 1MHz	Z_{in}	9K			ohms
Differential voltage range	V_{dir}	+/-20V			Vpeak
Input common mode voltage range	V_{icr}	+/-10V			Vpeak
Common mode rejection ratio (from point A, Figure 1)	CMMR	40			dB
Threshold characteristics (sine wave at 1MHz)	V_{th}	0.8		1.1	V p-p

Note: Threshold voltages refer to point A, Figure 2.

Figure 4: Electrical Characteristics (Receiver Section)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Differential output level at point B, Figure 1 (145 ohm load)	V_o	26	28	35	V p-p
Rise and Fall times (10% to 90% of p-p output)	T_r	100	160	300	ns
Output offset at point A in Figure 2 (35-ohm load) 2.5us after mid-bit crossing of parity bit of last word of a 660us message	V_{os}		+/-20	+/-75	mV peak
Differential output noise	V_{noi}			10	mV p-p

Figure 5: Electrical Characteristics (Transmitter Section)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VIH	INPUT "1"	2.4			VDC	
VIL	INPUT "0"			0.7	VDC	
IIL	INPUT I	-100		-650	uA	Note 1A
IIH	INPUT I			-650	uA	Note 1B
IIL	INPUT I	-20		+20	uA	Note 2A
IIH	INPUT I	-20		+20	uA	Note 2B
VOH	OUTPUT "1"	2.7			VDC	Note 3A/4A
VOL	OUTPUT "0"			0.4	VDC	Note 3B/4B

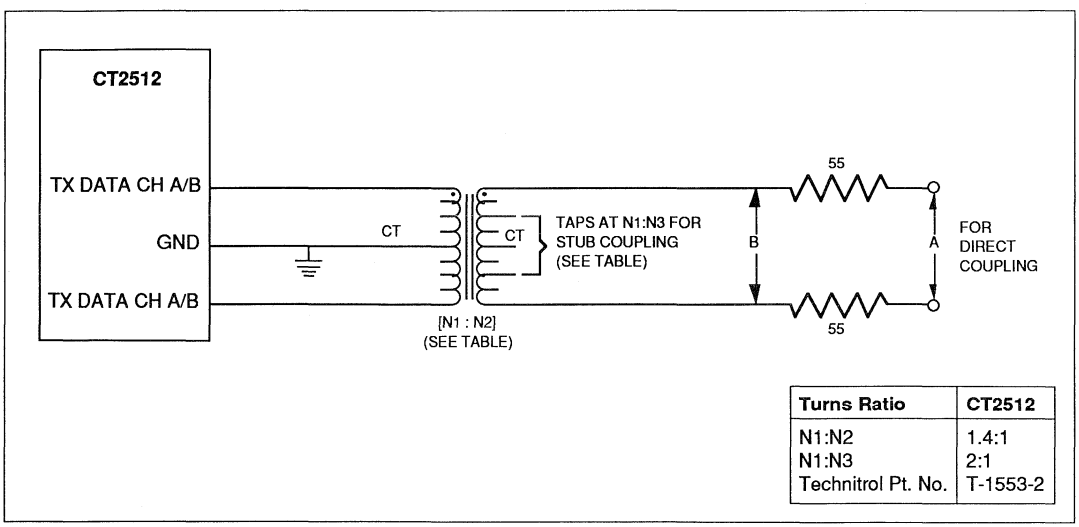
Note 1: For INPUT pins 12,13,14,15, 53, 54, 55.
V_{CC}= 5.5V
A. @ V_{IL} = 0.4V
B. @ V_{IH} = 2.4V

Note 2: All remaining INPUTS other than in Note 1.
V_{CC}= 5.5V
A. @ V_{IL} = 0.4V
B. @ V_{IH} = 2.4V

Note 3: For OUTPUT pins 4 through 11 and 43 through 50.
A. @ V_{CC} = 4.5V and I_{OH} = 3mA
B. @ V_{CC} = 2.4V and I_{OL} = 6mA

Note 4: All remaining OUTPUTS other than in Note 3.
A. @ V_{CC} = 4.5V and I_{OH} = 2mA
B. @ V_{CC} = 5.5V and I_{OL} = 4mA

Figure 6: CT2512 Logic Characteristics



Turns Ratio	CT2512
N1:N2	1.4:1
N1:N3	2:1
Technitrol Pt. No.	T-1553-2

Figure 7: Typical Direct Coupled Configuration

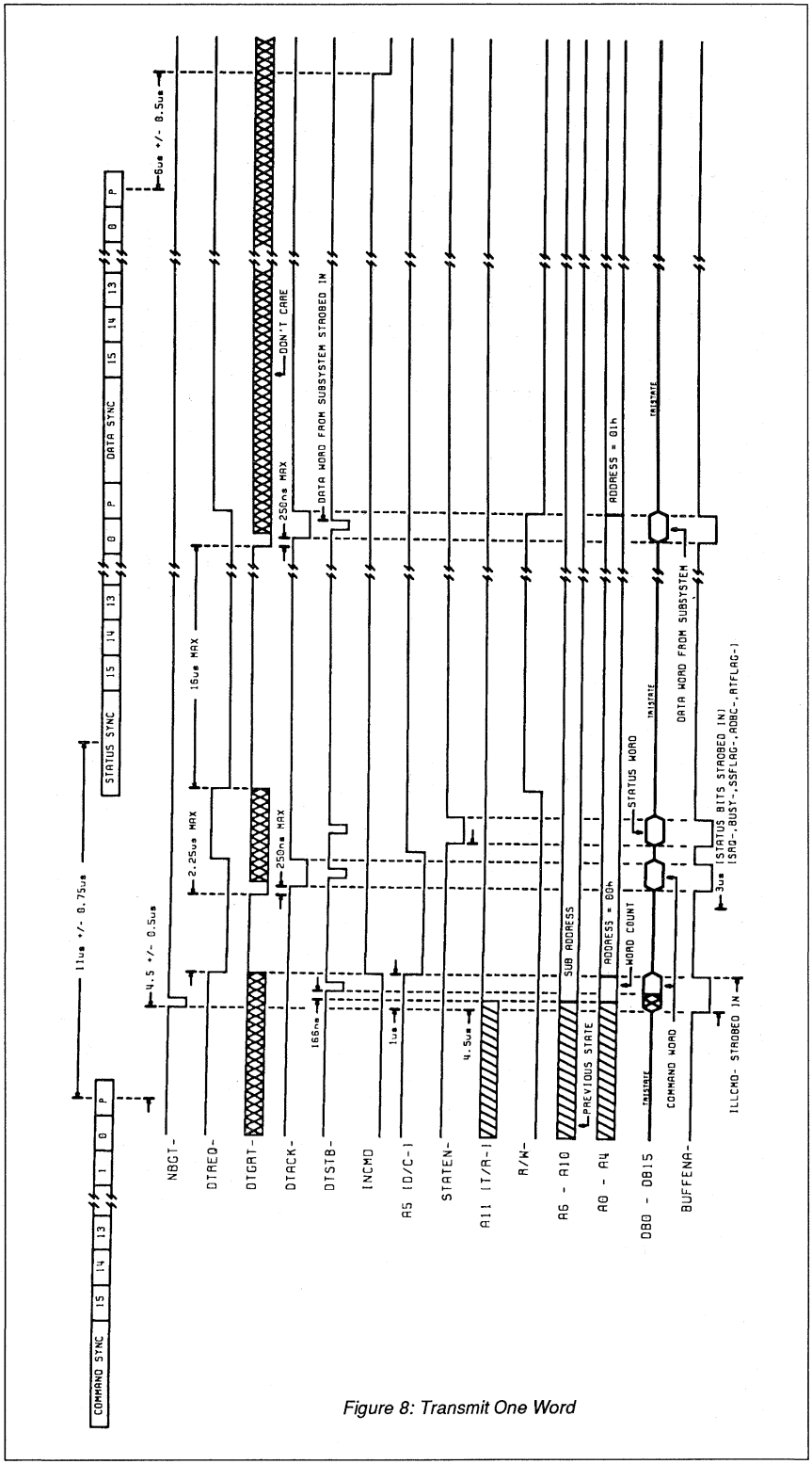


Figure 8: Transmit One Word

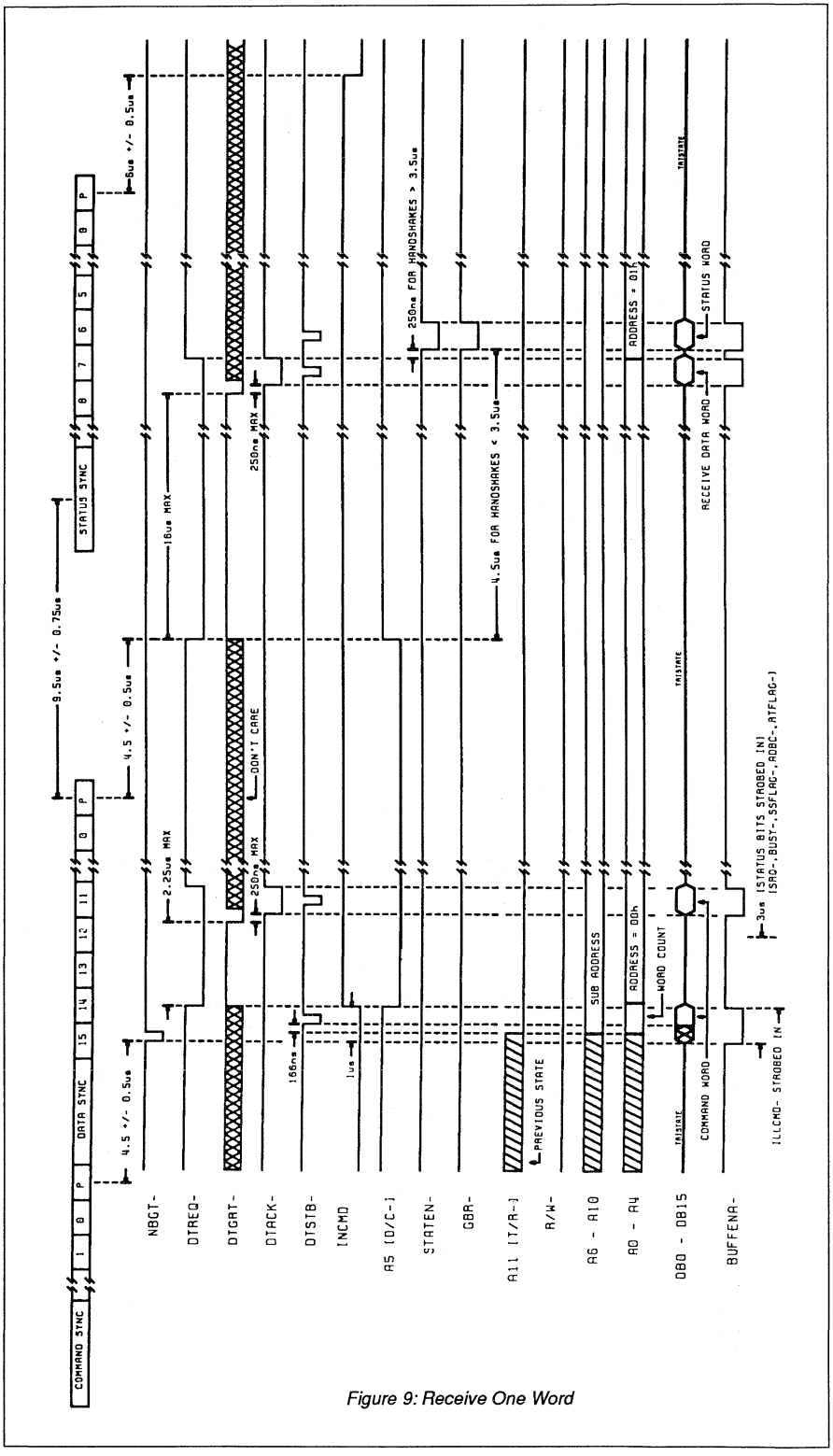


Figure 9: Receive One Word

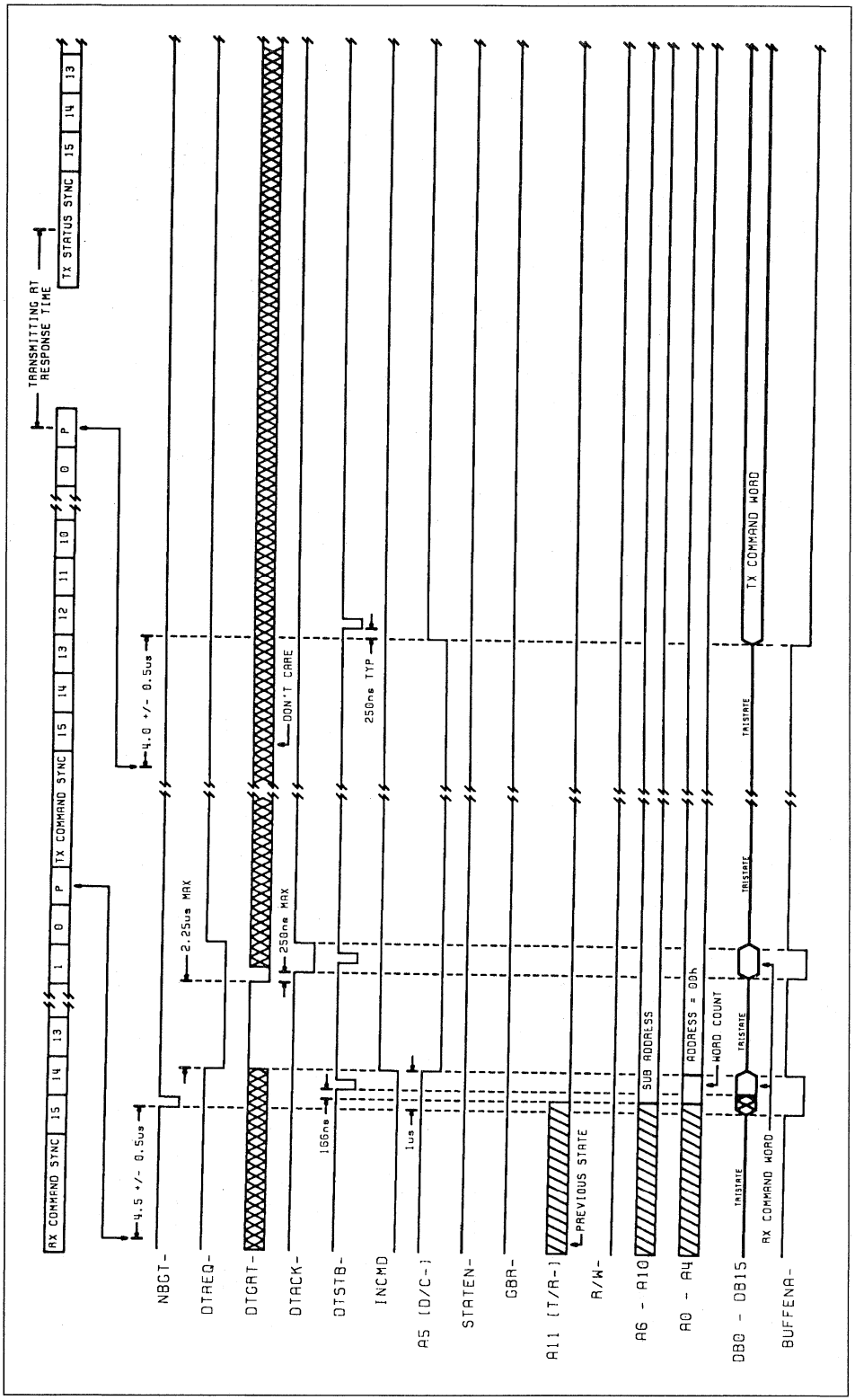


Figure 10: RT to RT Receive One Word (Part A)

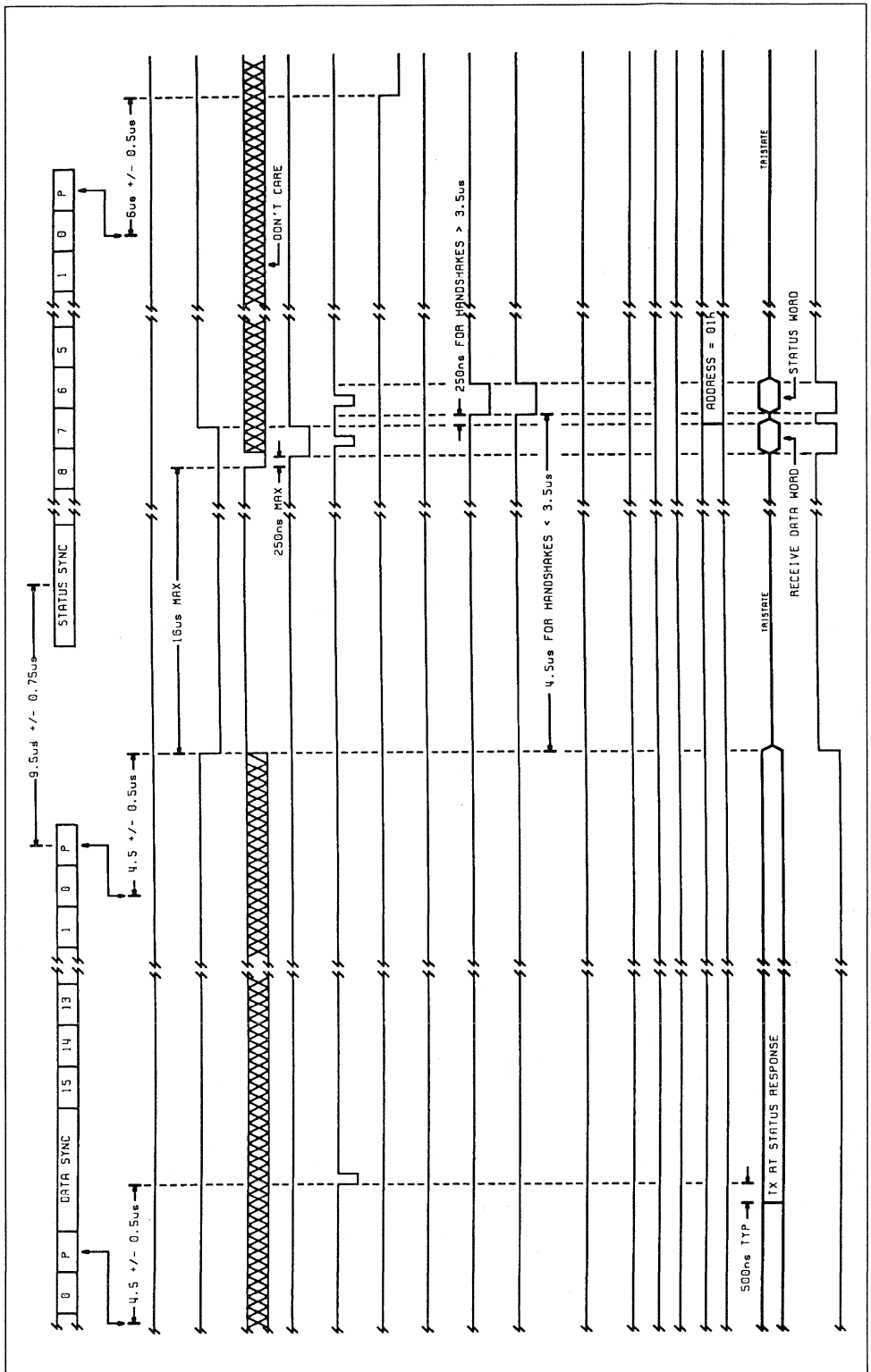


Figure 11: RT to RT Receive One Word (Part B)

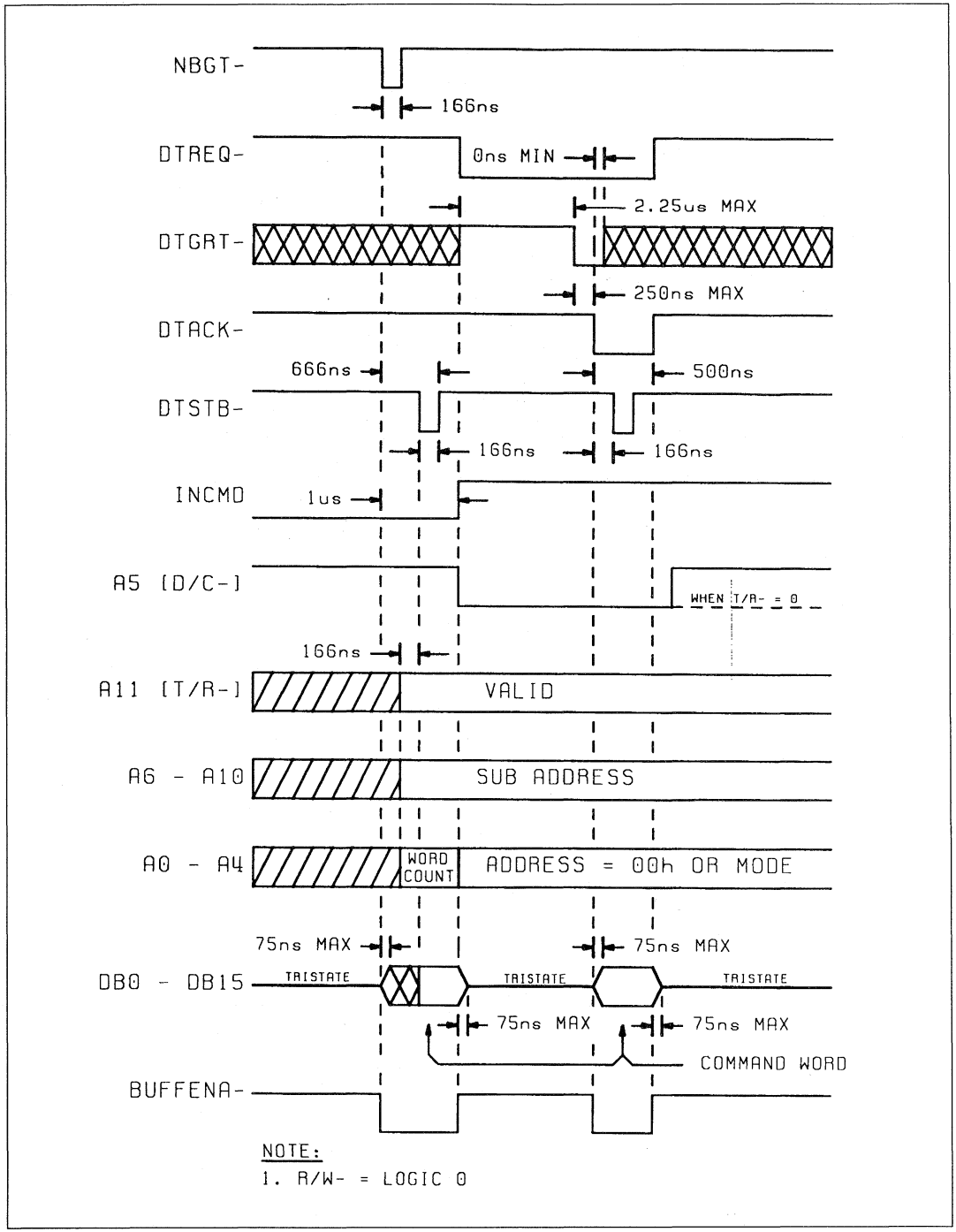


Figure 12: Command Word Transfer

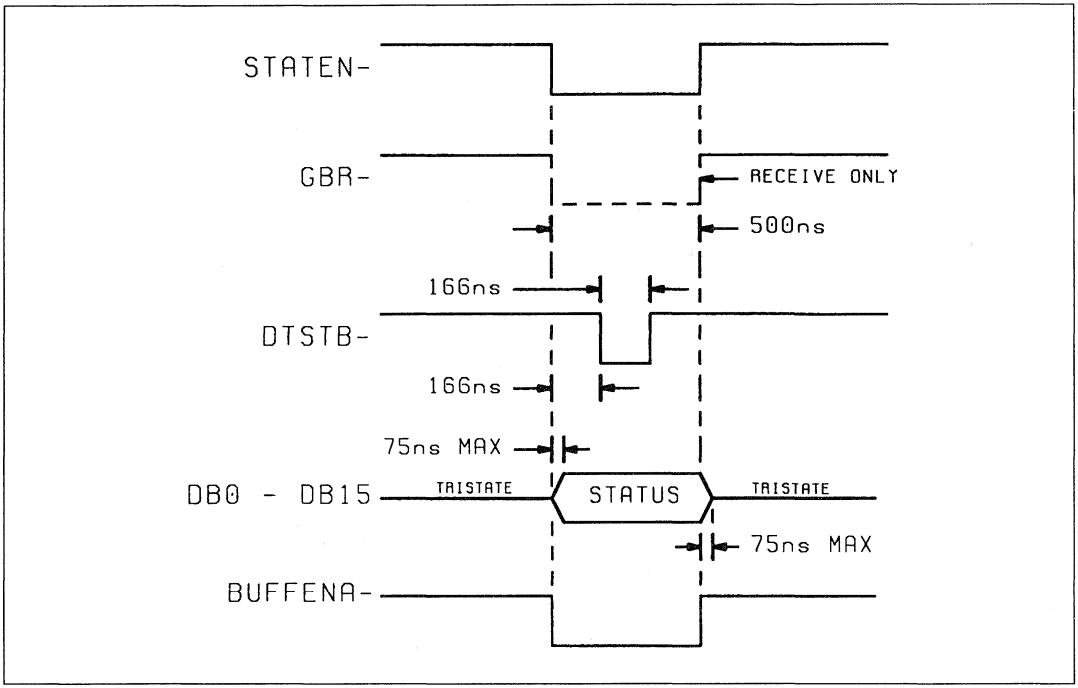


Figure 13: Status Word Transfer

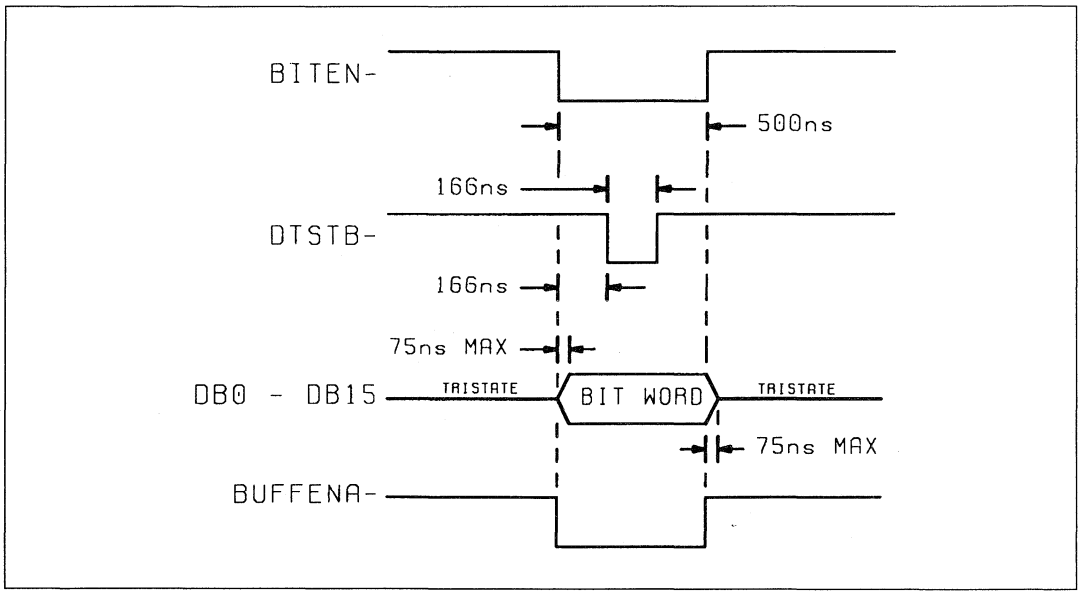


Figure 14: Bit Word Transfer

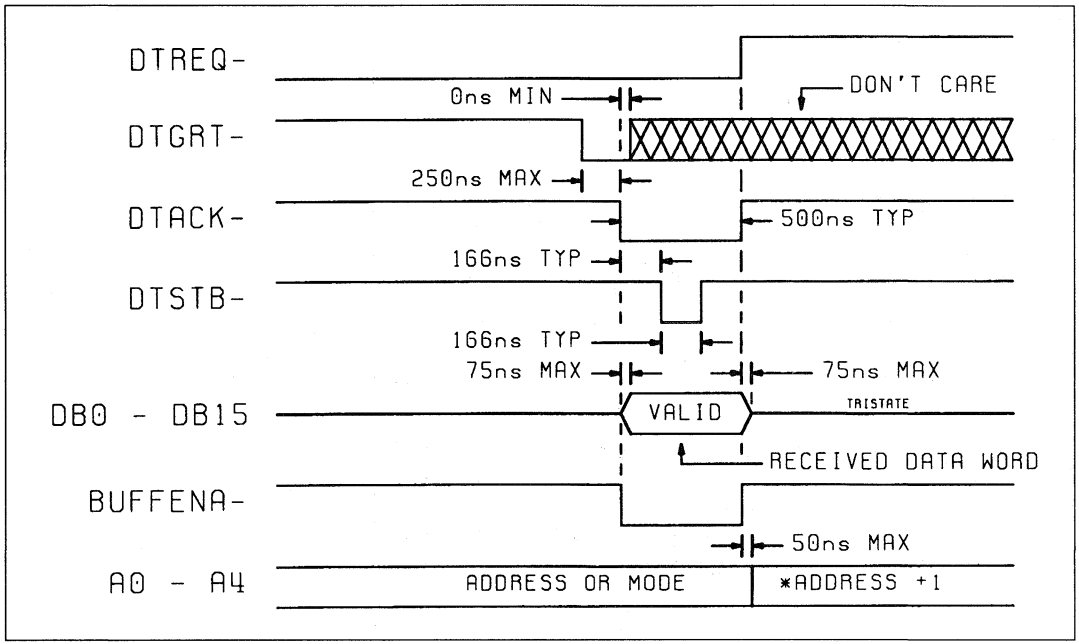


Figure 15: Data to Subsystem

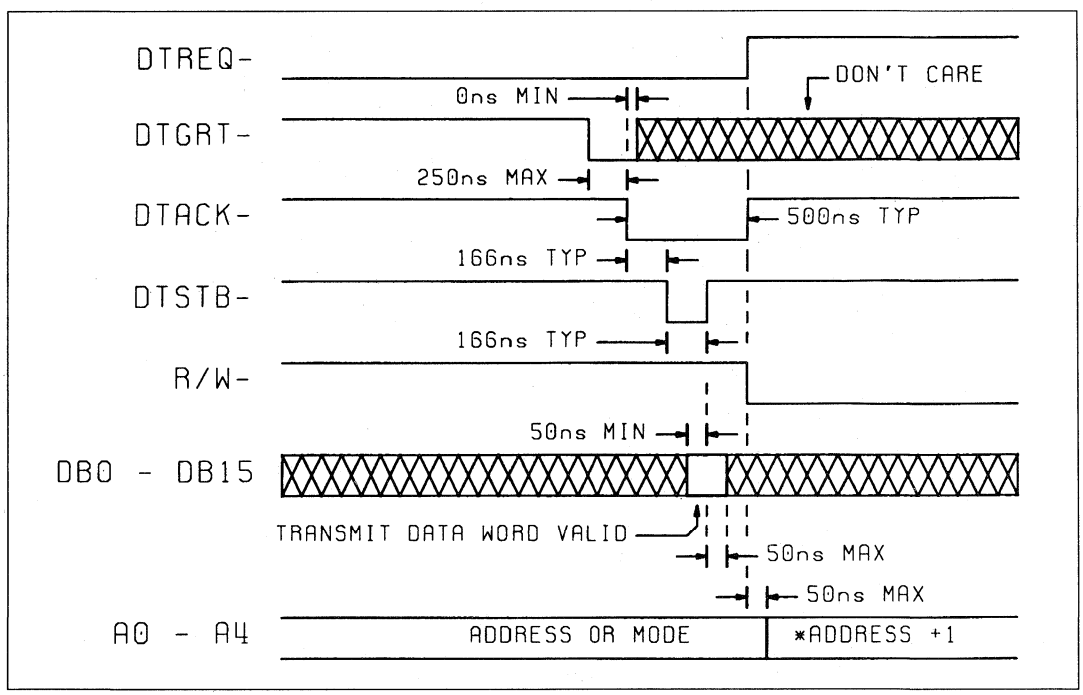


Figure 16: Data from Subsystem

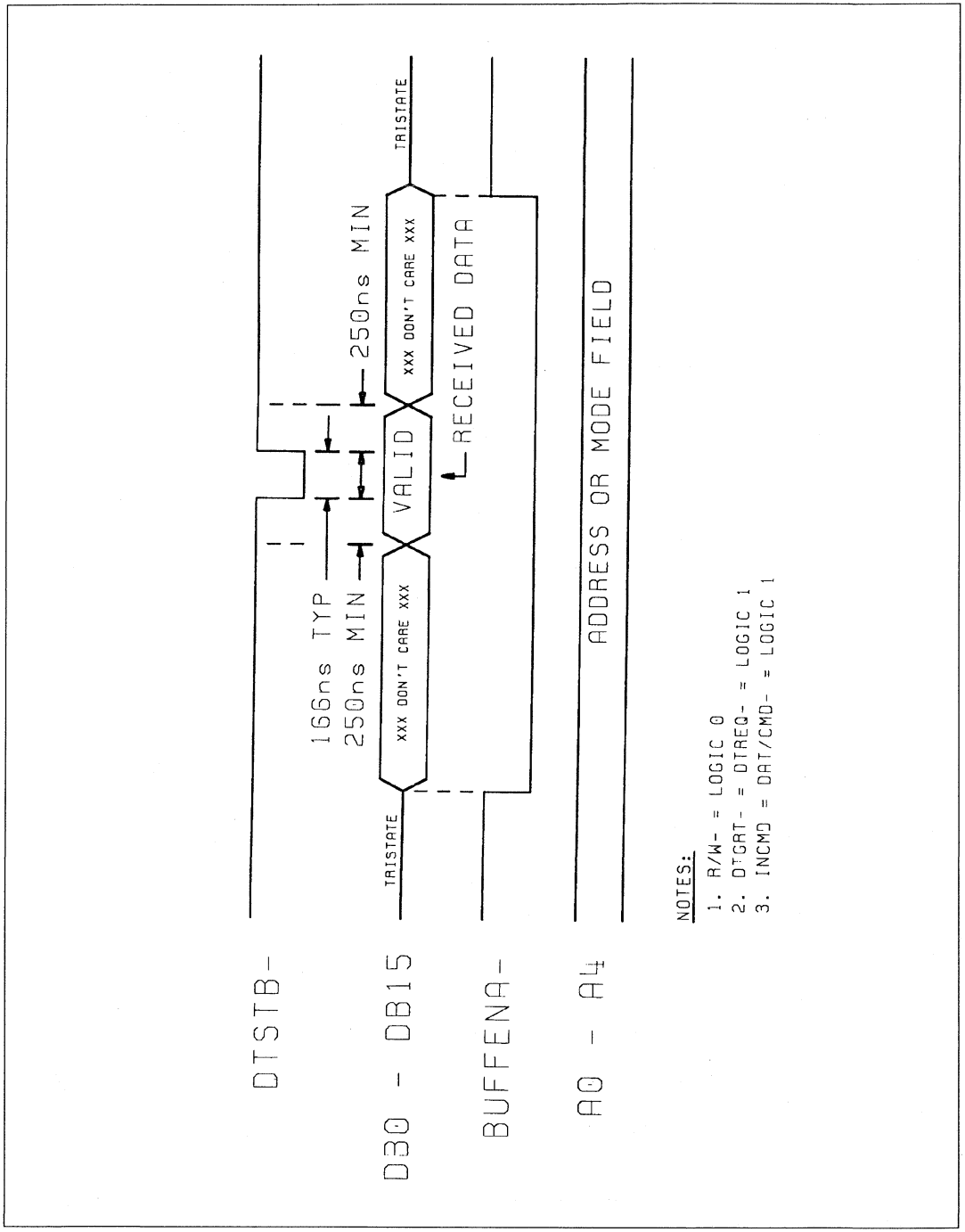
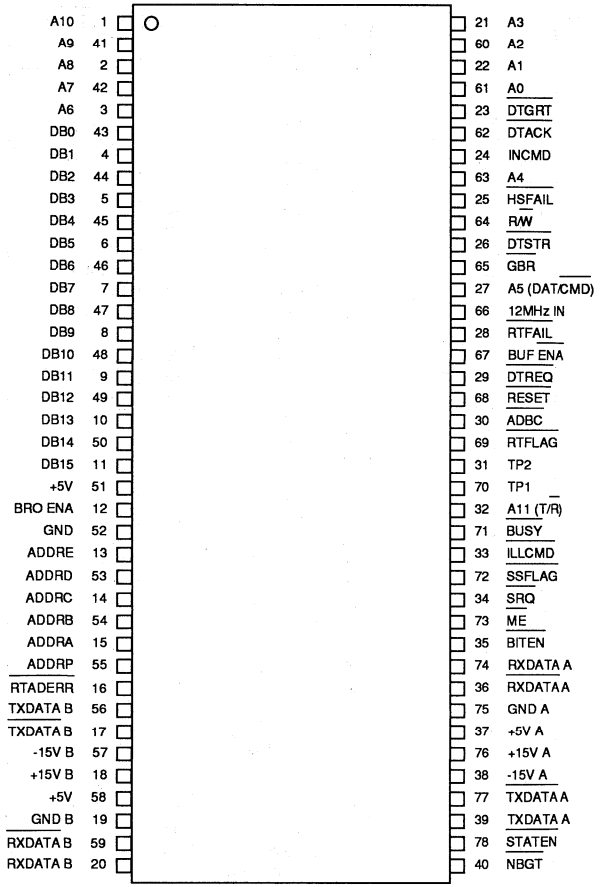


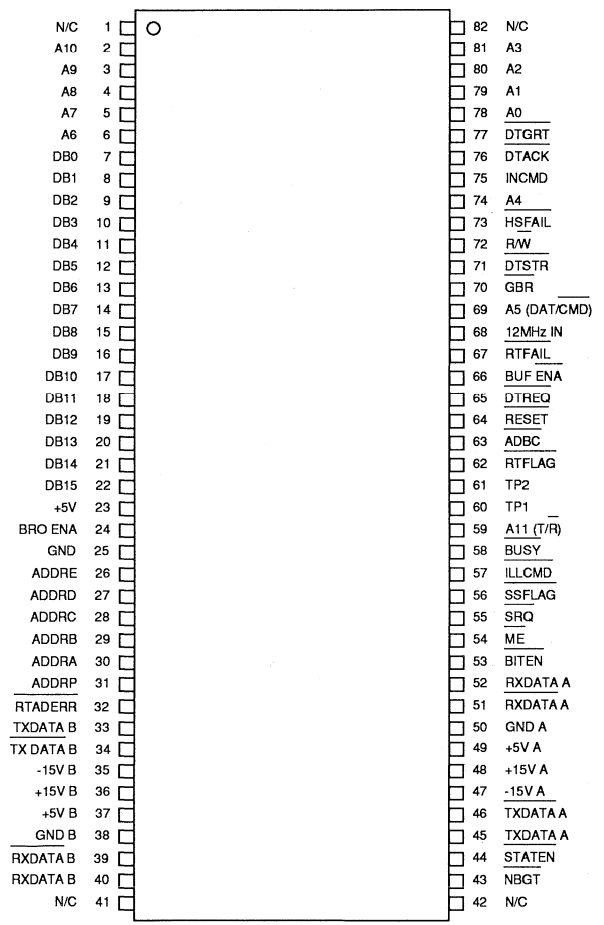
Figure 17: Data Transfers to Subsystem (No Handshake)



CT2512 PINOUT TABLE (DDIP)

PIN	FUNCTION	PIN	FUNCTION
1	A10	40	NBGT
2	A8	41	A9
3	A6	42	A7
4	DB1	43	DB0
5	DB3	44	DB2
6	DB5	45	DB4
7	DB7	46	DB6
8	DB9	47	DB8
9	DB11	48	DB10
10	DB13	49	DB12
11	DB15	50	DB14
12	BRO ENA	51	+5V
13	ADDRE	52	GND
14	ADDRC	53	ADDRD
15	ADDRA	54	ADDRB
16	RTADERR	55	ADDRP
17	TXDATA B	56	TXDATA B
18	+15V B	57	-15V A
19	GND B	58	+5V B
20	RXDATA B	59	RXDATA B
21	A3	60	A2
22	A1	61	A0
23	DTGRT	62	DTACK
24	INCMD	63	A4
25	HSFAIL	64	R/W
26	DTSTR	65	GBR
27	A5 (DAT/CMD)	66	12MHz IN
28	RTFAIL	67	BUF ENA
29	DTREQ	68	RESET
30	ADBC	69	RTFLAG
31	TP2 (NC)	70	TP1 (NC)
32	A11 (T/R)	71	BUSY
33	ILLCMD	72	SSFLAG
34	SRQ	73	ME
35	BITEN	74	RXDATA A
36	RXDATA A	75	GND A
37	+5V A	76	+15V A
38	-15V A	77	TXDATA A
39	TXDATA A	78	STATEN

Figure 18: DDIP Pin Connection Diagram - CT2512, and Pin-Out Table



CT2512 PINOUT TABLE (FLATPACK)

PIN	FUNCTION	PIN	FUNCTION
1	N/C	42	N/C
2	A10	43	$\overline{\text{NBGT}}$
3	A9	44	$\overline{\text{STATEN}}$
4	A8	45	TXDATA A
5	A7	46	$\overline{\text{TXDATA}}$ A
6	A6	47	-15V A
7	DB0	48	+15V A
8	DB1	49	+5V A
9	DB2	50	GND A
10	DB3	51	$\overline{\text{RXDATA}}$ A
11	DB4	52	RXDATA A
12	DB5	53	$\overline{\text{BITEN}}$
13	DB6	54	$\overline{\text{ME}}$
14	DB7	55	$\overline{\text{SRQ}}$
15	DB8	56	$\overline{\text{SSFLAG}}$
16	DB9	57	$\overline{\text{ILLCMD}}$
17	DB10	58	$\overline{\text{BUSY}}$
18	DB11	59	A11 (T/$\overline{\text{R}}$)
19	DB12	60	TP1
20	DB13	61	TP2
21	DB14	62	$\overline{\text{RTFLAG}}$
22	DB15	63	$\overline{\text{ADBC}}$
23	+5V	64	$\overline{\text{RESET}}$
24	BRO ENA	65	$\overline{\text{DTREQ}}$
25	GND	66	BUF $\overline{\text{ENA}}$
26	ADDRE	67	$\overline{\text{RTFAIL}}$
27	ADDRD	68	12MHz IN
28	ADDRC	69	A5 (DAT/$\overline{\text{CMD}}$)
29	ADDRB	70	$\overline{\text{GBR}}$
30	ADDRA	71	$\overline{\text{DTSTR}}$
31	ADDRP	72	R/$\overline{\text{W}}$
32	$\overline{\text{RTADERR}}$	73	$\overline{\text{HSFAIL}}$
33	TXDATA B	74	A4
34	$\overline{\text{TXDATA}}$ B	75	INCMD
35	-15V B	76	$\overline{\text{DTACK}}$
36	+15V B	77	$\overline{\text{DTGRT}}$
37	+5V B	78	A0
38	GND B	79	A1
39	$\overline{\text{RXDATA}}$ B	80	A2
40	RXDATA B	81	A3
41	N/C	82	N/C

Figure 19: Flatpack Pin Connection Diagram - CT2512, and Pin-Out Table

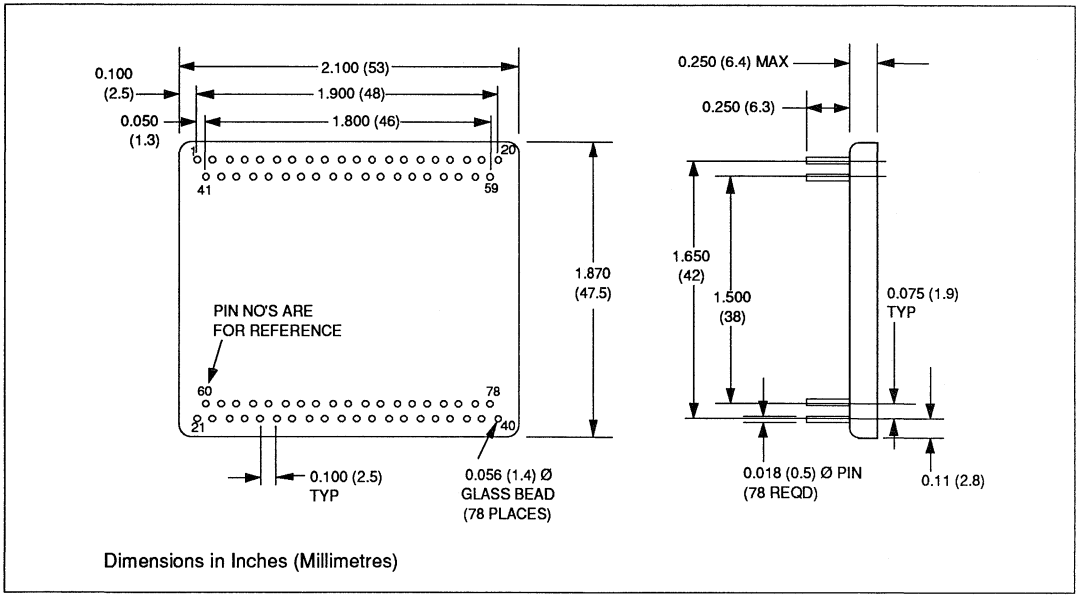


Figure 20: Mechanical Diagram - DDIP Configuration

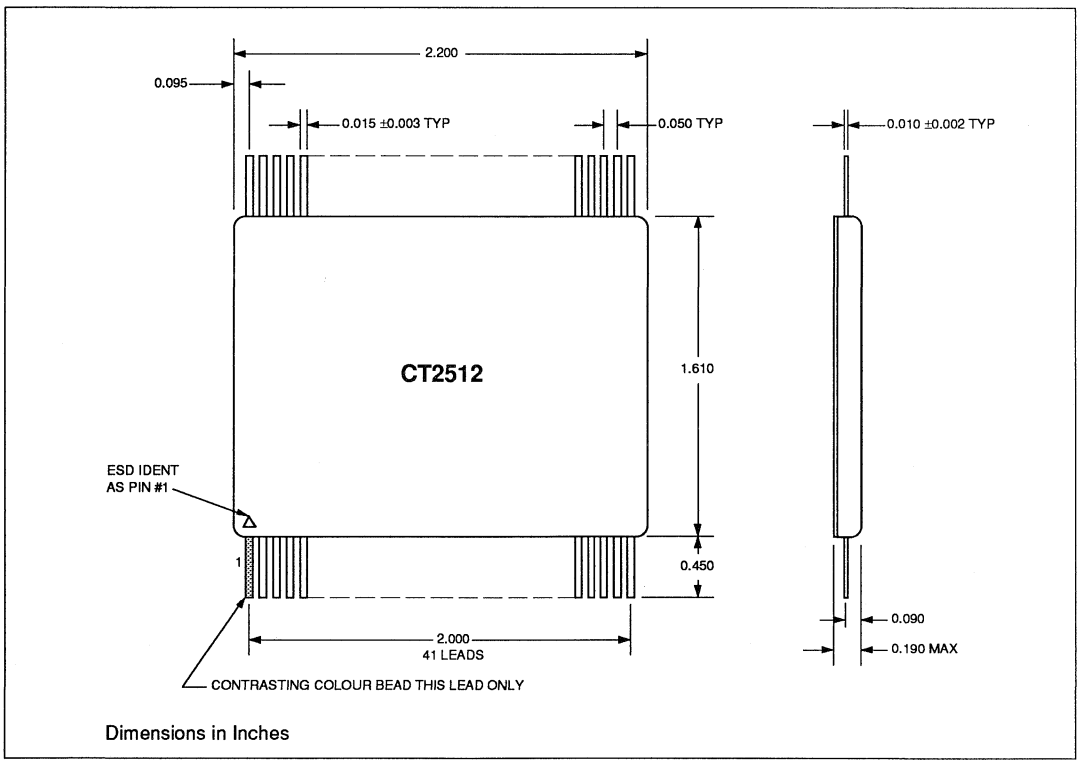


Figure 21: Mechanical Diagram - Flatpack Configuration

Section 4
Protocol

3091-1.3 November 1991

CT1602/10

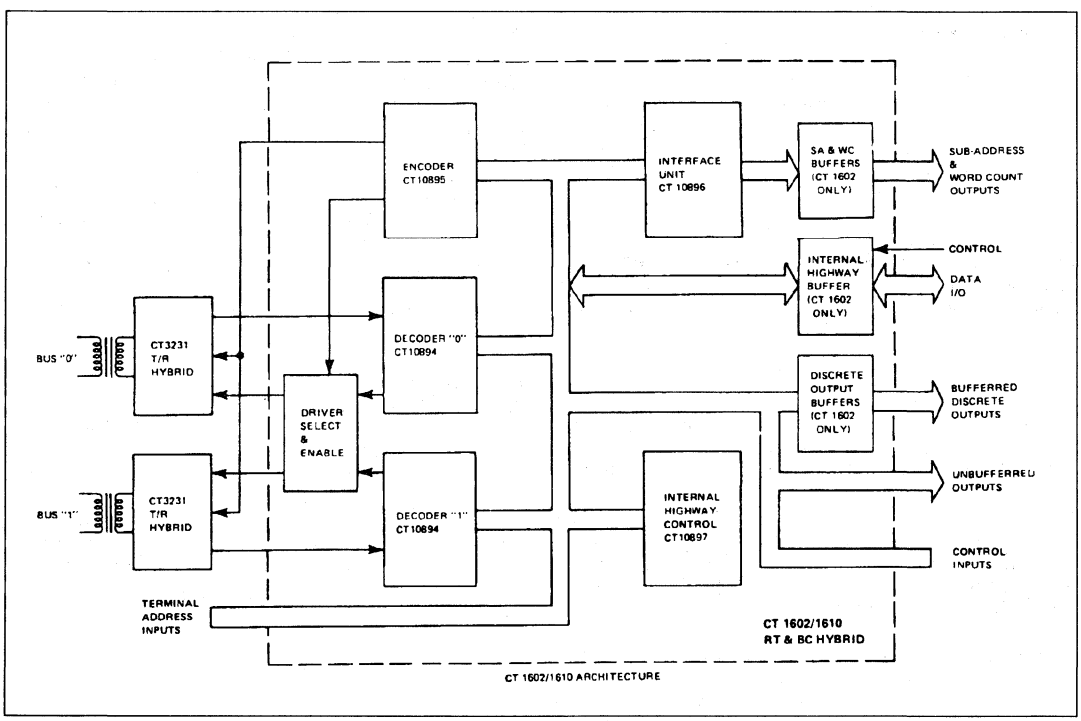
MIL-STD-1553B REMOTE TERMINAL, BUS CONTROLLER OR PASSIVE MONITOR HYBRIDS

The CT1602/CT1610 design incorporates five LSI chips that accomplish the dual redundant MIL-STD1553B Remote Terminal and/or Bus Controller Protocol Functions. Buffering has been added to the most commonly used output signals on the CT1602, minimizing external hardware requirements. The CT1610 contains no buffers resulting in very low power consumption. The CT1602/CT1610 connects directly to all GPS Driver/Receiver Units.

FEATURES

- Performs the complete dual-redundant Remote Terminal and Bus Controller Protocol Functions of MIL-STD-1553B
- Automatic switchover to superseding input commands
- Screened to applicable portions of MIL-STD-883 Level B
- 750 mW power consumption CT1602

  125 mW power consumption CT1610
- Small Size
- Available in plug-in or flatpack configuration
- Compatible with all GPS Driver/Receiver Units
- 5V DC operation
- -55° to +125°C operation



CT 1602/1610 ARCHITECTURE

REMOTE TERMINAL OPERATION

Receive Data Operation

All valid data words associated with a valid receive data command word for the RT are passed to the subsystem. The RT examines all command words from the bus and will respond to valid (i.e. correct Manchester, parity coding etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the data words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 us intervals. This applies to receive data words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words have been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these data words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

Transmit Data Operation

If the RT receives a valid transmit data command addressed to the RT, then the RT will request the data words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each data word, the next word is requested by the RT as soon as the transmission of the current word has commenced.

It is essential that the subsystem should provide all the data words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

Control of Data Transfers

This section describes the detailed operation of the data transfer mechanism between RT and subsystems. It covers the operations of the signals $\overline{\text{DTRQ}}$, $\overline{\text{DTAK}}$, IUSTB, H/$\overline{\text{L}}$, $\overline{\text{GBR}}$, $\overline{\text{NBGT}}$, TX/$\overline{\text{RX}}$ during receive data and transmit data transfers.

Figure 7 shows the operation of the data handshaking signals during a receive command with two data words. When the RT has fully checked the command word, $\overline{\text{NBGT}}$ is pulsed low, which can be used by the subsystem as an initialization signal. TX/$\overline{\text{RX}}$ will be set low indicating a receive command. When the first data word has been fully validated, $\overline{\text{DTRQ}}$ is set low. The subsystem must then reply within approximately 1.5 us by setting $\overline{\text{DTAK}}$ low. This indicates to the RT that the subsystem is ready to accept data The data word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{\text{L}}$ as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 12.

If the subsystem does not declare itself busy, then it must respond to DTRQ going low by setting DTAK low within approximately 1.5 us. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. DTRQ being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, GBR is pulsed low if the block is entirely correct and valid. This is used by the subsystem as permission to make use of the data block If no GBR signal is generated, then an error has been detected by the RT and the entire data block is invalid and no data words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical fashion but there will be a delay of approx 70 us between $\overline{\text{NBGT}}$ going low and $\overline{\text{DTRQ}}$ first going low. See Figure 10.

Figure 6 shows the operation of the data handshaking signals during transmit command with three, data words. As with the receive command discussed previously, $\overline{\text{NBGT}}$ is pulsed low if the command is valid and for the RT. TX/$\overline{\text{RX}}$ will be set high indicating a transmit data command. While the RT is transmitting its status word, it requests the first data word from the subsystem by setting $\overline{\text{DTRQ}}$ low. The subsystem must then reply within approximately 13.5 us by setting $\overline{\text{DTAK}}$ low. By setting $\overline{\text{DTAK}}$ low, the subsystem is indicating that it has the data word ready to pass to the RT. Once $\overline{\text{DTAK}}$ is set low by the subsystem, $\overline{\text{DTRQ}}$ should be used together with H/$\overline{\text{L}}$ and TX/$\overline{\text{RX}}$ to enable first the high byte and then the low byte of the data word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{\text{DTRQ}}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 11.

Additional Data Information Signals

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{\text{INCMD}}$, the subaddress lines SA0-4, the word count lines WC0-4 and current word count lines CWC0-4. Use of these signals is optional.

$\overline{\text{INCMD}}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, transmit/receive bit. and word count from the command word are all ma a vailable to the subsystem as SA0-4, TX/RX and WC0-4 respectively. They may be sampled when $\overline{\text{INCMD}}$ goes low and will remain valid while $\overline{\text{INCMD}}$ is low.

The subaddress is intended to be used by the subsystem as an address pointer for the data block Subaddress 0 and 31 are mode commands, and there can be no receive or transmit data blocks associated with these. (Any data word associated with a mode command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.

The TX/$\overline{RX}$ signal indicates the direction of data transfer across the RT - subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32 words.

The current word count is set to 0 at the beginning of a new message and is incremented following each data word transfer across the RT - subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer). It should be noted that there is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

Subsystem Use of Status Bits and Mode Commands

General Description

Use of the status bits and the mode commands is one of the most confusing aspects of MIL-STD-1553B. This is because much of their use is optional, and also because some involve only the RT while others involve both the RT and the subsystem.

The CT1602/CT1610 allows full use to be made of all the status bits, and also implements all the mode commands. The subsystem is given the opportunity to make use of status bits, and is only involved in mode commands which have a direct ir~lpact on the subsystem.

The mode commands in which the subsystem may be involved are Synchronize, Sychronize with data word, Transmit Vector Word, Reset and Dynamic Bus Control Allocation. The status bits to which the subsystem has access are Service Request, Busy, Subsystem Flag and Dynamic Bus Control Acceptance. Operation of each of these mode commands and of the status bits is described in the following sections.

The subsystem designer should note that all other mode commands and status bits are serviced internally by the RT, and the subsystem has no access to them. In particular, the terminal flag and message error status bits and BIT word contents are all controlled internally by the RT.

Synchronize Mode Commands

Once the RT has validated the command word and checked for the correct address, the $\overline{SYNC}$ line is set low. The signal WC4 will be set low for a Synchronize mode command Figure 16, and high for a Synchronize with data word mode command Figure 15. In a Synchronize with data word mode command, $\overline{SYNC}$ remains low during the time that the data word is received. Once the data word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/L as the byte indicator (high byte first followed by low byte). SYNC being low should be used on the enable to allow IUSTB to clock synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these mode commands, the $\overline{SYNC}$ signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figure 14 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word mode command. The RT requests data by setting $\overline{VECTEN}$ low. The subsystem should use H/L to enable first the high byte and then the low byte of the Vector word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{VECTEN}$ goes low. If the subsystem has not been designed to handle the Vector word mode command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the mode command, the RT will not be affected in any way by Vector word circuitry not being implemented in the subsystem. It will however transmit a data word as the Vector word, but this word will have no meaning.

Reset Mode Command

Figure 8 shows the relevant signal timings for an RT receiving a valid reset mode command. Once the command word has been fully validated and serviced, the $\overline{RESET}$ signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This mode command is intended for use with a terminal which has the capability of configuring itself into a bus controller on command from the bus. The line $\overline{DBCREQ}$ cannot go true unless the $\overline{DBCACC}$ line was true at the time of the valid command, i.e. tied low. For terminals acting only as RTs, the signal $\overline{DBCACC}$ should be tied high (inactive), and the signal $\overline{DBCREQ}$ should be ignored and left unconnected.

Use of the Busy Status Bit

The Busy Bit is used by the subsystem to indicate that it is not ready to handle data transfers either to or from the RT.

The RT sets the bit to logic one if the $\overline{\text{BUSY}}$ line from the subsystem is active low at the time of the second falling edge of INCLK after $\overline{\text{INCMD}}$ goes low. This is shown in Figure 13. Once the Busy bit is set, the RT will stop all receive and transmit data word transfers to and from the subsystem. The data transfers in the Synchronize with data word and Transmit Vector word mode commands are not affected by the Busy bit and will take place even if it has been set.

It should be noted that a minimum of 0.5 us subaddress decoding time is given to the subsystem before sening of status bits. This allows the subsystem to selectively set the Busy bit if for instance one subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of the Service Request Status Bit

The Service Request bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested.

The timing of the setting of this bit is the same as the Busy bit and is shown in Figure 13. Use of $\overline{\text{SERVREQ}}$ has no effect on the RT apart from sening the Service Request bit.

It should be noted that certain mode commands require that the last status word be transmitted by the RT instead of the current one, and therefore a currently set status bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{\text{SERVREQ}}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This status bit is used by the RT to indicate a subsystem fault condition. If the subsystem sets $\overline{\text{SSERR}}$ low at any time, the subsystem fault condition in the RT will be set, and the Subsystem Flag status bit will subsequently be set The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset mode command.

Dynamic Bus Control Acceptance Status Bit

$\overline{\text{DBCACC}}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{\text{DBCREQ}}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required then $\overline{\text{DBCACC}}$ must be tied high. $\overline{\text{DBCACC}}$ tied high inhibits $\overline{\text{DBCREQ}}$ and clears BIT TIME 18 in the status response.

Bus Driver/Receiver Interface

Receive Data

The decoder chip requires two TTL signals (PDIN & NDIN) to represent the data coming in from the bus. PDIN should be driven to a logic level '1' when the bus waveform exceeds a specified positive threshold and NDIN should be driven to a logic level '1' when a specified negative threshold is exceeded. During the quiet period on the bus both signals should be at the same logic level. All the bus receivers must be permanently enabled, the selection if the bus in use is done within the chip set.

Transmit Data

The signals generated by the encoder chip ($\overline{\text{PDOUT}}$ & $\overline{\text{NDOUT}}$) are of the same format as the receive data The only difference is that the TTL signals are negative logic, e.g. the signal is active when on logic level '0'. This means that when the encoder is quiet both $\overline{\text{PDOUT}}$ & $\overline{\text{NDOUT}}$ are at logic level '1'. Both the signals should be used in conjunction with $\overline{\text{TXEN}}$ and the appropriate driver enable, e.g. (CS0 - enable for bus 0). $\overline{\text{TXEN}}$ only enables the driver when it should be transmitting, and the driver enable routes the data on to the bus in use.

Figure 5 shows an example of a typical interface circuit between the CT1602/CT1610 and a driver/receiver unit.

BUS CONTROL OPERATION

To enable its use in a bus controller each chip in the chipset has additional logic within it. This logic can be enabled by pulling the pin labelled RT/$\overline{BC}$ low. Once the chipset is in bus control mode, all data transfers must be initiated by the bus control processor correctly commanding the chipset via the subsystem interface. In bus control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the CT1602 or CT1610 as a 1553B bus control interface, the bus control processor must be able to carry out four basic bus-related functions. Two inputs, BCOPA and BCOPB allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{BCOPSTB}$ input. $\overline{BCOPSTB}$ must only be strobed low when $\overline{NDRQ}$ is high. This is particularly important when two options are required during a single transfer.

With these options all message types and lengths can be handled. Normal BC/RT exchanges are carried out in the chipset option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{BCOPSTB}$. On receipt of the strobe, the CT1602/CT1610 loads the command word from an external latch using CWEN and H/$\overline{L}$ The command word is transmitted down the bus. The TX/$\overline{RX}$ bit is, however, considered by the chipset as being its inverse and so if a transmit command is sent to a RT, Figure 17, the chipset in BC mode believes it has been given a receive command. As the RT returns the requested number of data words plus its status, the BC chipset carries out a full validation check and passes the data into the subsystem using $\overline{DTRQ}$, $\overline{DTAK}$, H/$\overline{L}$, IUSTB and CWC as in RT operation. It also supplies GBR at the end of a valid transmission. Conversely, a receive command sent down the bus is interpreted by the BC chipset as a transmit command, and so the requisite data words are added to the command word, see Figure 18.

For mode commands, where a single command word is required, option one is selected by strobing $\overline{BCOPSTB}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the command word is loaded from the external latch using $\overline{CWEN}$ and H/$\overline{L}$, the correct sync and parity bits are added and the word transmitted, see Figure 20. Mode commands followed by a data word requires option two. Option two, selected by strobing $\overline{BCOPSTB}$ while BCOPA is low and BCOPB is high, loads a data word via $\overline{DWEN}$ and H/$\overline{L}$, adds sync and parity and transmits them to the bus, see Figure 21. If the mode code transmitted required the RT to return a data word, then selecting option three by strobing $\overline{BCOPSTB}$ when BCOPA and BCOPB are both high will identify that data word and if validated, output it to the subsystem interface using RMDSTB and H/$\overline{L}$ This allows data words resulting from mode codes to be identified differently from ordinary data words and routed accordingly, see Figure 22. All received status words are output to the subsystem interface using STATSTB and H/$\overline{L}$.

In BC option three, if the signal $\overline{PASMON}$ is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for command and status words or RMDSTB for data words.

RT to RT transfers require the transmission of two command words. A receive command to one RT is contiguously followed by a transmit command to the the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{BCOPSTB}$) for option zero must be delayed until $\overline{NDRQ}$ has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the bus control processor, see Figure 19.

Note: For all BC operations, BCOPA and BCOPB must remain valid and stable for a minimum of 1 us following the leading (negative going) edge of $\overline{BCOPSTB}$.

PIN DESCRIPTION CT1602 AND CT1610

Signal Mnemonic	Hybrid Sink or Source	Signal Description
RX DATA0/1	SINK	**Positive Date In**. This should be a TTL description of the positive, half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined positive threshold is exceeded on the bus.
RX DATA 0/1	SINK	**Negative Data In**. This should be a TTL description of the negative half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined negative threshold is exceeded on the bus.
TX INHIBIT 0/1	SOURCE	**Transmitter Enable**. Goes low when the transmitter is transmitting. Should be used to enable the bus drivers.
TX DATA	SOURCE	**Positive Data Out** - When this signal goes high the bus should be driven positive.
TX DATA	SOURCE	**Negative Data Out** - When this signal goes high the bus should be driven negative.
RTAD 0-4	SINK	**RT address lines** - These should be hardwired by the user. RTAD4 is the most significant bit.
RTADPAR	SINK	**RT address parity line** - This must be hardwired by the user to give odd parity.
BCSTEN 0/1	SINK	**Recognition of Broadcast command enable** - When low the recognition of broadcast command is prevented on the specified bus.
6MCK	SINK	**6 Megahertz master clock.**
IH 08 IH 19 IH 210 IH 311 IH 412 IH 513 IH 614 IH 715	SINK/SOURCE	**Internal Highway** - Bi-directional 8 bit highway on which 16 bit words are passed in two bytes. IH 715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
DTRQ	SOURCE	**Data Transfer Request** - Goes low to request a data transfer between the Chip Set and subsystem. Goes high at the end of the transfer.
DTAK	SINK	**Data Transfer Acknowledge** - Goes low to indicate that the subsystem is ready for the data transfer.
IUSTB	SOURCE	**Interface Unit Strobe** - This is a double pulse strobe used to transfer the two bytes of data

Signal Mnemonic	Hybrid Sink or Source	Signal Description
H/$\overline{L}$	SOURCE	**High/Low** - Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{GBR}$	SOURCE	**Good Block Received** - Pulses low for 500ns when a block of data has been received by the Chip Set and has passed all the validity and error checks.
$\overline{NBGT}$	SOURCE	**New Bus Grant** - Pulses low whenever a new command is accepted by the Chip Set.
TX/$\overline{RX}$	SOURCE	**Transmit/Receive** - The state of this line informs the subsystem whether it is to transmit or receive data The signal is valid while $\overline{INCMD}$ is low.
$\overline{INCMD}$	SOURCE	**In Command** - Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
WC 0-4	SOURCE	**Word Count** - These five lines specify the requested number of data words to be received or transmitted. Valid when $\overline{INCMD}$ is low.
SA 0-4	SOURCE	**Sub Address** - These five lines are a label for the data being transferred. Valid when $\overline{INCMD}$ is low.
CWC 0-4	SOURCE	**Current Word Count** - These five lines define which data word in the message is currently being transferred.
$\overline{SYNC}$	SOURCE	**Synchronize** - Goes lowwwhen a synchronize mode code is being serviced.
$\overline{VECTEN}$/ $\overline{DWEN}$	SOURCE	**Vector Word Enable/DataWord Enable** - In the RT mode, this signal is provided to enable the contents of the vector word latch (which is situated in the subsystem) onto the Chip Set's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
$\overline{RESET}$	SOURCE	**Reset** - This line pulses low for 500ns on completion of the servicing of a valid and legal mode command to reset remote terminal.
$\overline{SSERR}$	SINK	**Subsystem Error** - By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.
$\overline{BUSY}$	SINK	**Busy** - This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the Chip Set.
$\overline{SERVREQ}$	SINK	**Service Request** - This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{PASMON}}$	SINK	**Passive Monitor** - When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASMON}}$ remains low. All traffic on the bus will be handed, after validation, to the subsystem via STATSTB for status and commands words, and RMDSTB for data words.
$\overline{\text{BCOPSTB}}$	SINK	**Bus Controller Operation Strobe** - When functioning as a Bus Controller a low going pulse on this line will initiate the selected bus controller operation on the requested bus, using BCOPA&B and REQBUSA&B.
BCOPA	SINK	**Bus Control Operation A** - Least significant bit of the bus controller operation select lines.
BCOPB	SINK	**Bus Control Operation B** - Most significant bit of the bus controller operation select lines.
REQBUS A	SINK/SOURCE	**Request Bus A** - This line,wwhen in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, ie. they are sources. When in BC mode these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	SINK/SOURCE	**Request Bus B** - Most significant bit of the bus request lines. (See above for description.)
RT/$\overline{\text{BC}}$	SINK	**Remote Terminal/Bus Control** - This line when high causes the chip set to function as a remote terminal. When low the chip set functions as a bus controller or passive monitor.
$\overline{\text{DBCACC}}$	SINK	**Dynamic Bus Control Accept** - This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{\text{LTFAIL}}$	SOURCE	**Loop Test Fail** - This line goes low if any error in the transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{\text{ERROR}}$	SOURCE	**Error** - This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{\text{CMSYNC}}$ (RT mode) and also by $\overline{\text{RTO}}$ in the BC mode.
$\overline{\text{RTO}}$	SOURCE	**Reply Time Out** - This signal will pulse low whenever the reply time for a transmitting terminal has been exceeded. This line is intended for the bus controller use.
$\overline{\text{TXTO}}$	SOURCE	**Transmitter Time Out** - This line goes true if the transmitter time out limits are exceeded.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
INCLK	SOURCE	**Internal Clock (2 MHz)** - This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{EOT}}$	SOURCE	**End of Transmission** - Goes low if a valid sync plus two data bits do not appear in time to be contiguous with preceding word.
$\overline{\text{RTADER}}$	SOURCE	**Remote Terminal Address Error** - This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
$\overline{\text{HSFAIL}}$	SOURCE	**Handshake Failure** - This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the Chip Set/subsystem data transfer handshaking.
$\overline{\text{LSTCMD}}$/ $\overline{\text{CWEN}}$	SOURCE	**Last Command/Command Word Enable** - This line pulses low when servicing a valid and legal mode command to transmit last command. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a command word is required for transmission.
$\overline{\text{STATEN}}$/ STATSTB	SOURCE	**Status Enable/Status Strobe** - This line pulses low to enable the status word onto the internal highway for transmission. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses high, when in the Bus Control mode, to strobe received status words into the subsystem. When $\overline{\text{PASMON}}$ is true this line pulses high for Command and Status words.
$\overline{\text{BITEN}}$/ RMDSTB	SOURCE	**Built In Test Enable/Receive Mode Data Strobe** - This line pulses low when servicing a valid and legal mode command to transmit the internal BIT word. This signal is for information only and must not be used to enable data from the subsystem. This line also pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASMON}}$.
$\overline{\text{DWSYNC}}$	SOURCE	**Data Word Sync** - This line goes low if a data word sync and two Manchester biphase bits are valid.
$\overline{\text{CMSYNC}}$	SOURCE	**Command Word Sync** - This line goes low if a command word sync and two Manchester biphase bits are valid.
$\overline{\text{NDRQ}}$	SOURCE	**No Data Required** - This line goes low if the encoder transmit buffer is full i.e. another word is going to be transmitted. This signal is for information only and must not be used to enable data from the subsystem.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{PARER}}$	SOURCE	**Parity Error** - This line will pulse low if a parity error is detected by the decoder.
$\overline{\text{MANER}}$	SOURCE	**Manchester Error** - This line will pulse low if a Manchester error is detected by the decoder.
$\overline{\text{DBCREQ}}$	SOURCE	**Dynamic Bus Control Request** - This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the accept bit was set.
$\overline{\text{VALD}}$	SOURCE	**Valid Data** - This line will pulse low when a valid data word is received.
$\overline{\text{BUF INH}}$*	SINK	**Buffer Inhibit** - A low on this line causes the Buffered Signals to assume a high impedance state.
$\overline{\text{IH ENA}}$*	SINK	**Internal Highway Enable** - A low on this line enables the Internal Highway transceiver to transmit or receive data which is controlled by the IH DIR Line.
IH DIR*	SINK	**Internal Highway Direction** - Controls the direction of data through the Internal Highway Transceiver. High = To Subsystem A → B Low = From Subsystem B → A

* NOT USED ON CT1610

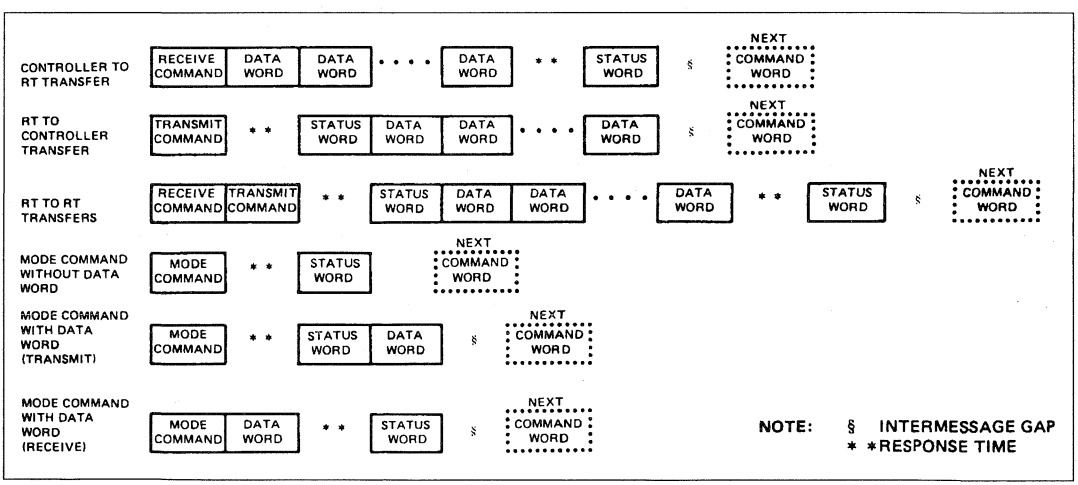


Figure 1: Typical Message Formats

T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	OverridelnhibitTerminal FlagBit	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	TransmitBITWord	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

NOTE: To be determined (TBD)

Figure 2: Assigned Mode Codes

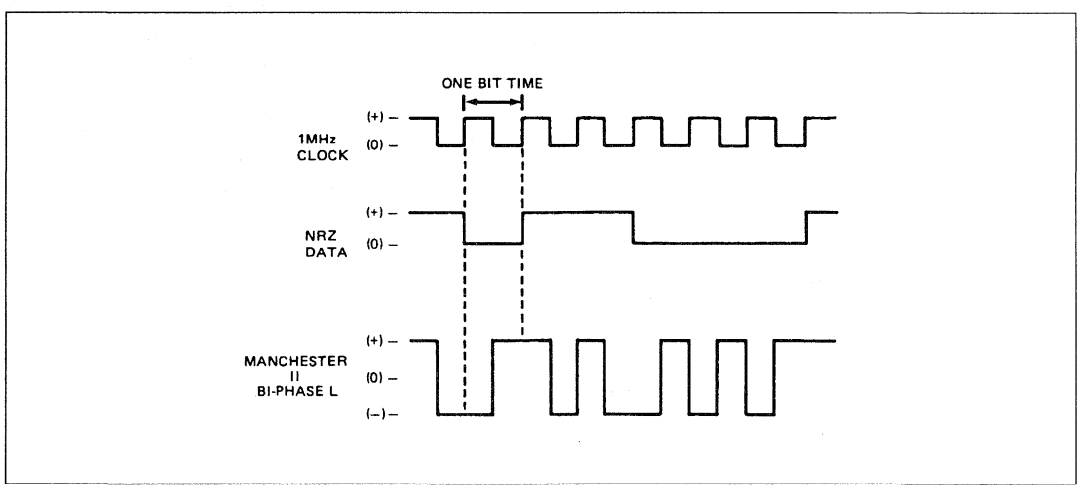


Figure 3: Data Encoding

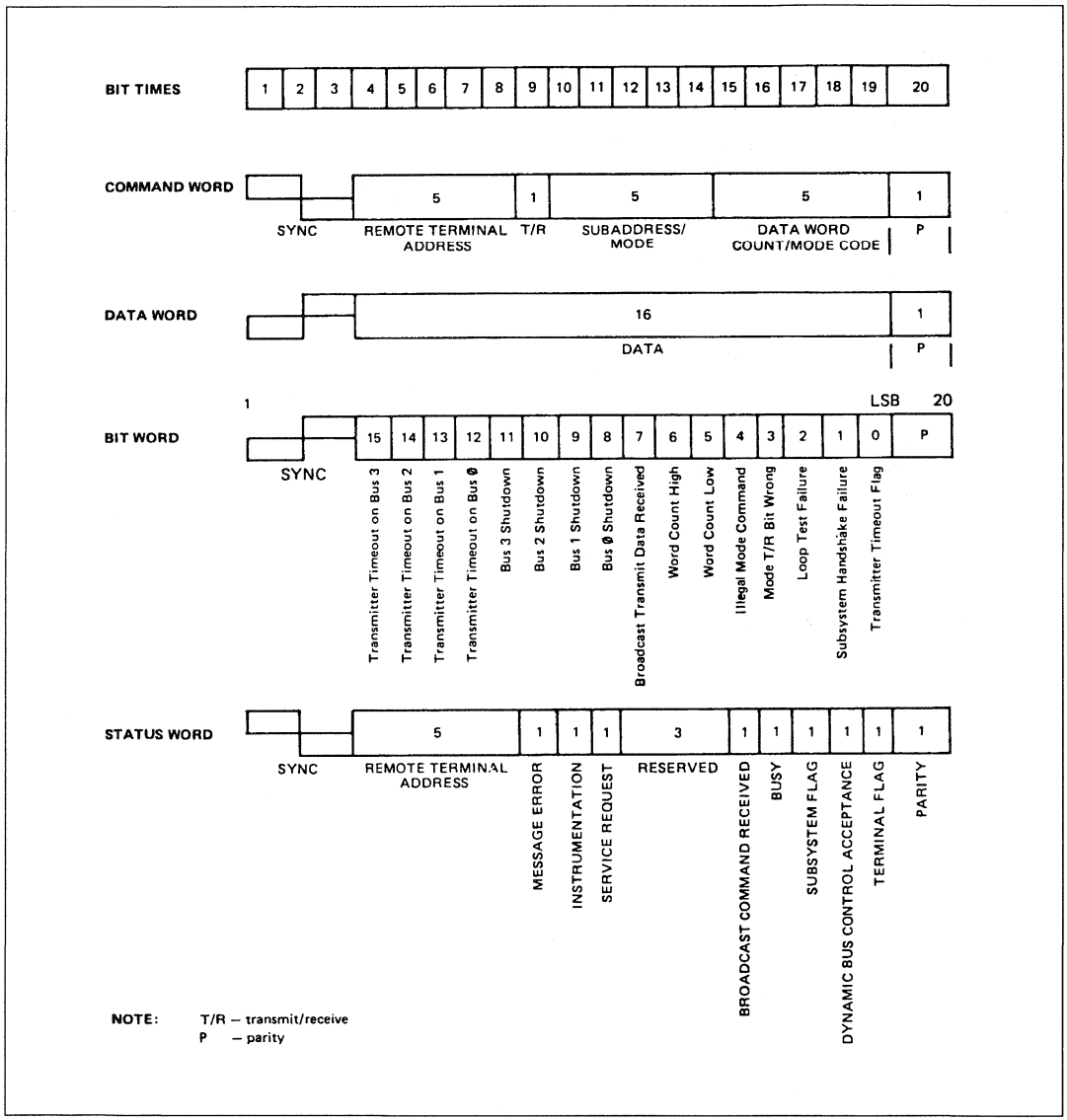


Figure 4: Word Formats

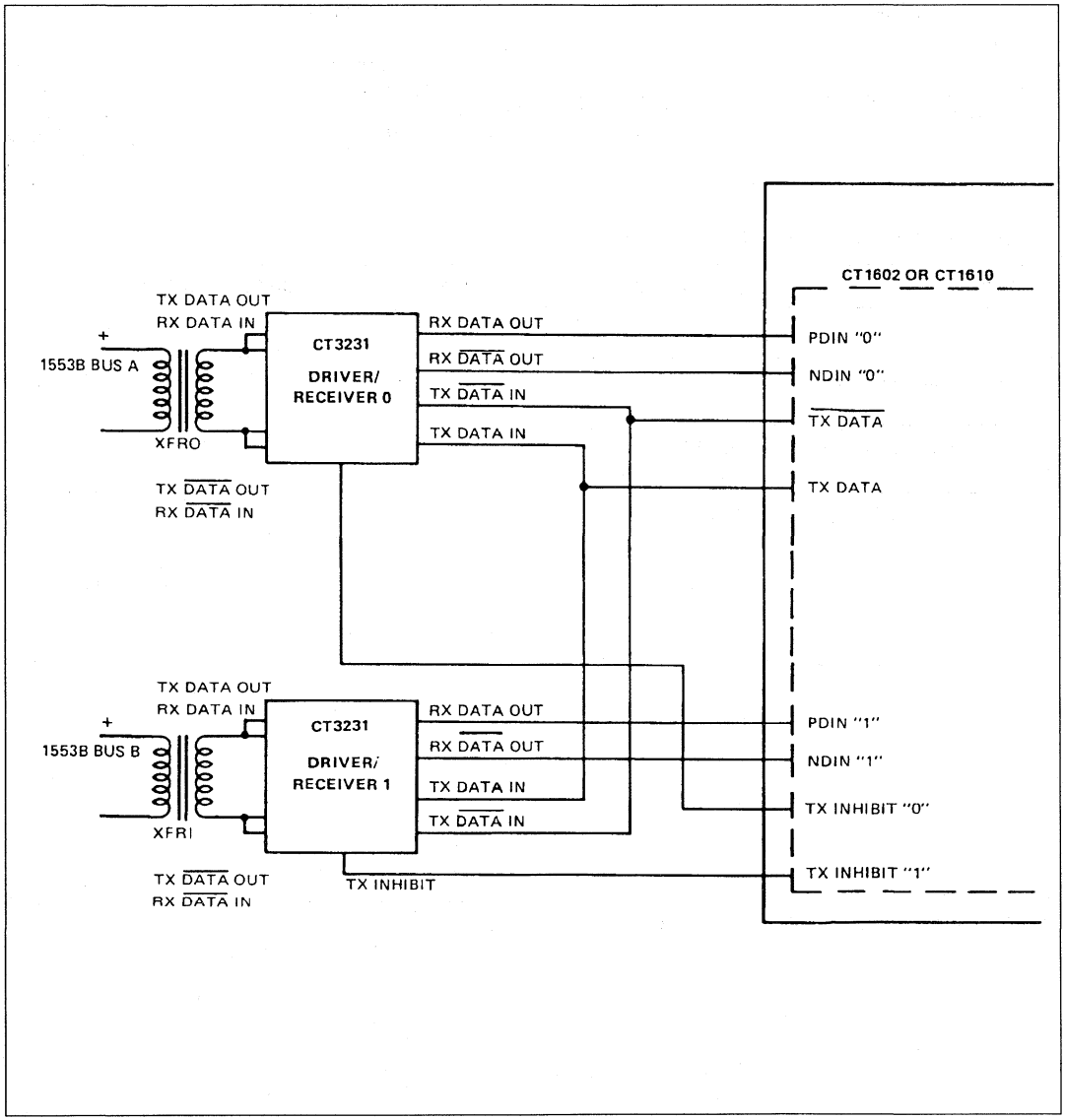


Figure 5: Examples of an interface between CT1602 or CT1610 and Driver/Receiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating free-air temperature	-55°C to +125°C
Storage temperature range	-65°C to +150°C

CLOCK REQUIREMENTS

Frequency	6.0 MHz
Stability -55° to +125°C	±0.01% (100ppm)
Maximum Asymmetry	60-40%
Rise/Fall Time	10 nsec max
Output level TTL	Logic "0" 0.4v max Logic "1" 2.4v min

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	COMMENTS
V_{CC}		4.5	5.5	V	
V_{IH} High - level input voltage	CMOS TTL	V_{CC}-1 2.0	V_{CC} V_{CC}	V V	
V_{IL} Low - level input voltage	CMOS TTL	0 0	1.0 0.7	V V	
V_{OH} High - level output voltage	V_{CC} = MIN I_{OH} = -800uA I_{OH} = -400 I_{OH} = -3mA	 2.4 2.4 2.4	 	 V V V	 LS32 LS241-LS244 (CT1602 Only)
V_{OL} Low - leveloutput voltage	V_{CC} = MIN I_{OL} = +2mA I_{OL} = +4mA I_{OL} = +12mA	 	 0.4 0.4 0.4	 V V V	 LS32 LS241-LS244 (CT1602 Only)
I_{IH} HIgh - level input current	V_{CC} = MAX V_{IH} = 2.4V	 -400 -20 -500	 5.0 20 0.0	 uA uA uA	 IH08-IH715 PULL-UPS
I_{IL} Low - level input current	V_{CC} = MAX V_{IL} = 0.4V	 -500 -200 -800	 0.0 0.0 -350	 uA uA uA	 IH08-IH715 PULL-UPS
I_{CC} Supply Current	V_{CC} = MAX, Fclk = 6MHz Outputs enabled and open CT1602 CT1610		 310 35	 mA mA	

NOTE:

ALL MAX/MIN VALUES SHOWN ARE FOR WORST CASE OPERATING CONDITIONS, WHERE APPROPRIATE, AT -55°C or +125°C.

1. **PULL-UPS** DENOTES: RTADD0-RTADD4, RTADDPAR, BUF_INH/, and IH_INH/
2. **LS32** DENOTES: TXDATA, TXDATA/, TXINH0, and TXINH1
3. **LS241-LS244** DENOTES: CWC0-4, SA0-4, IH08-IH715, SYNC/, IUSTB, TX-RX/, INCMD/, H-L/, STATEN/, EOT/, INCLK, NBGT/, DTRQ/, VECTEN/, and GBR/.

TIMING DIAGRAMS

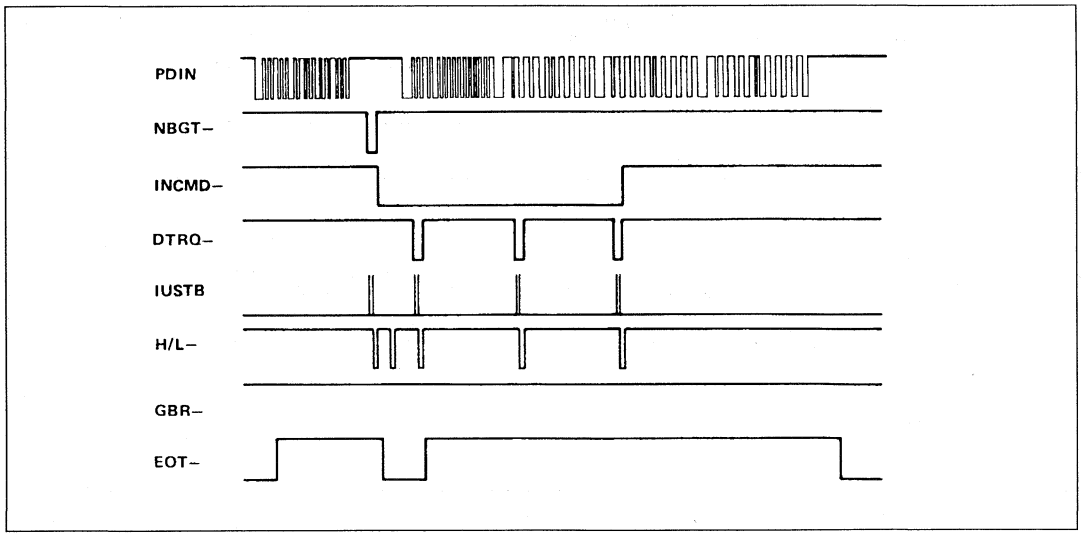


Figure 6: Transfer of Three Data Words from RT 03 to BC

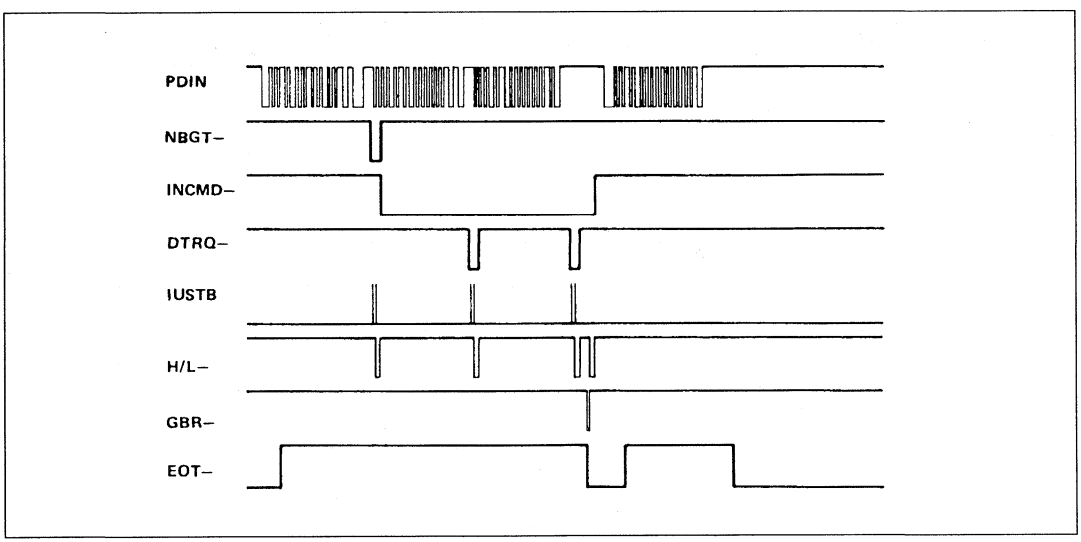


Figure 7: Transfer of Three Data Words from BC to RT 03

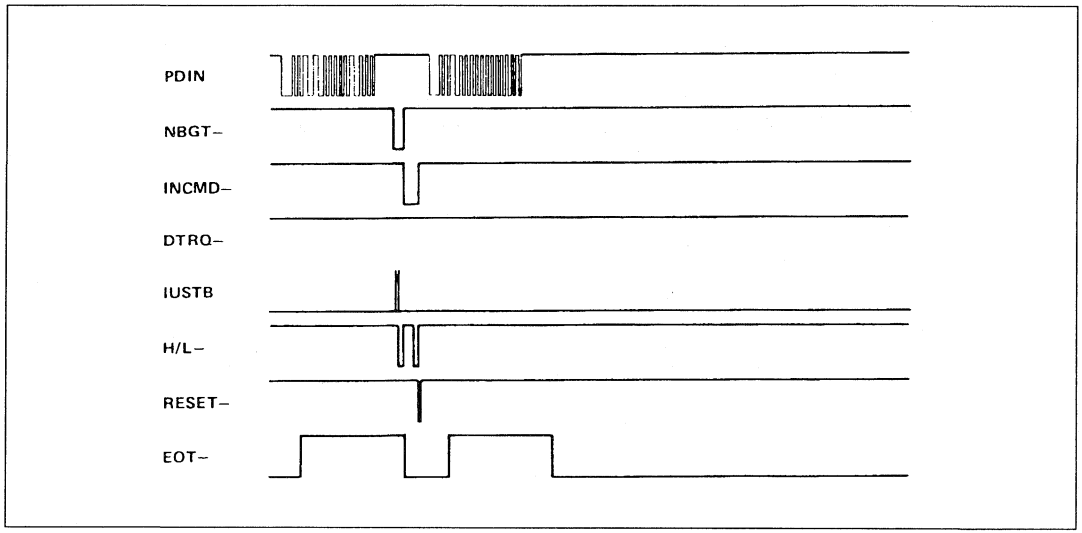


Figure 8: Mode Command Reset Remote Terminal

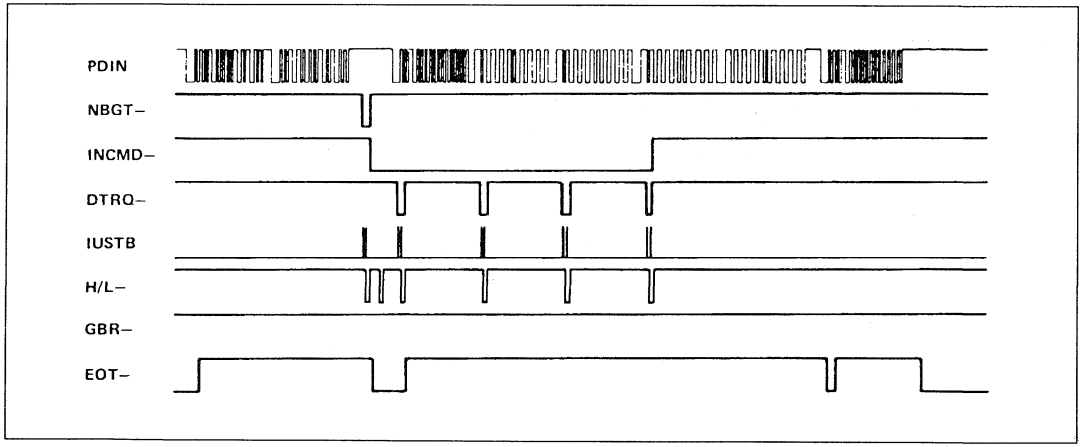


Figure 9: RT to RT Transfer of Four Data Words This RT Sending the Data

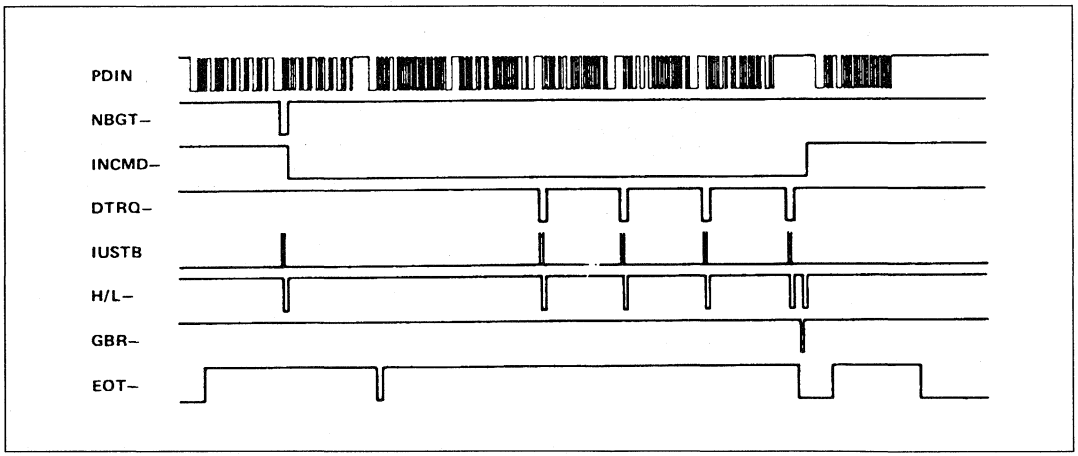


Figure 10: RT to RT Transfer of Four Data Words - This RT Receiving the Data

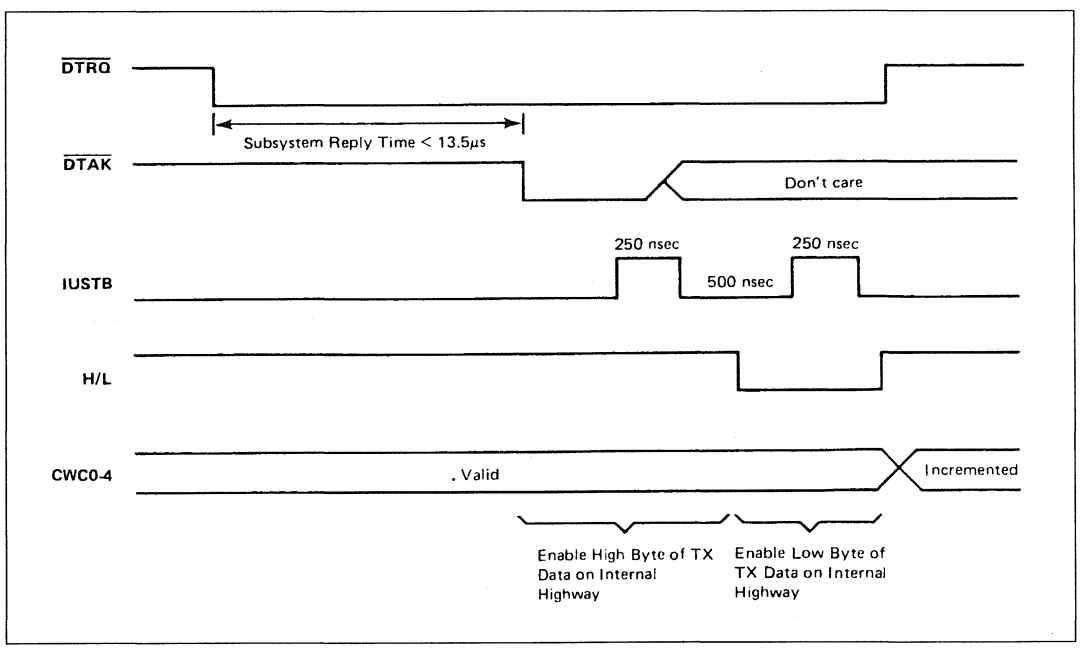


Figure 11: Handshaking for TX Data Transfers

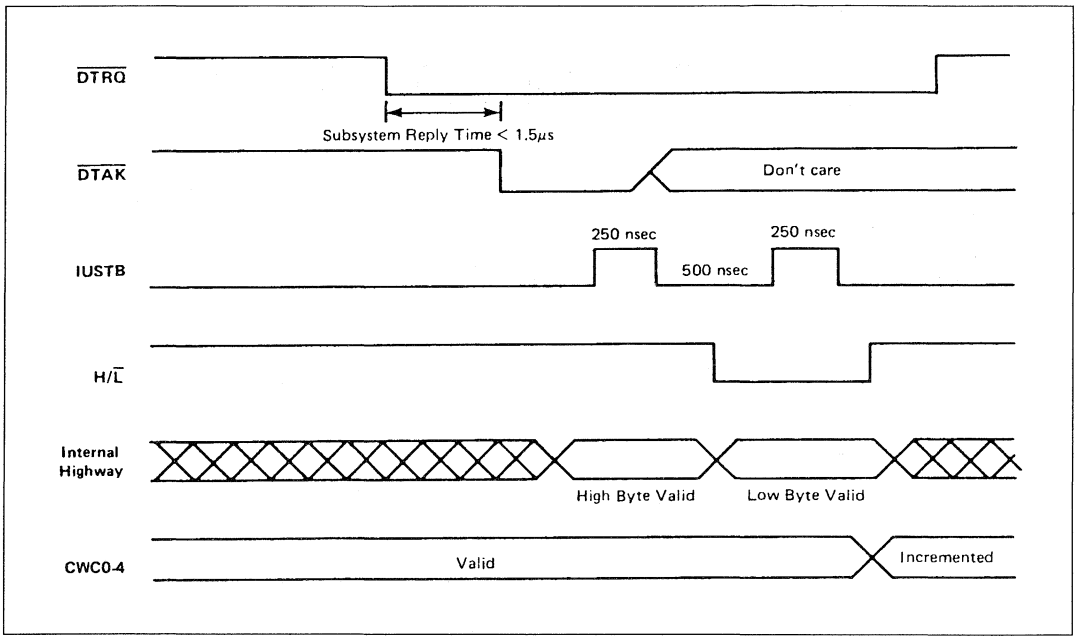


Figure 12: Handshaking for RX Data Transfers

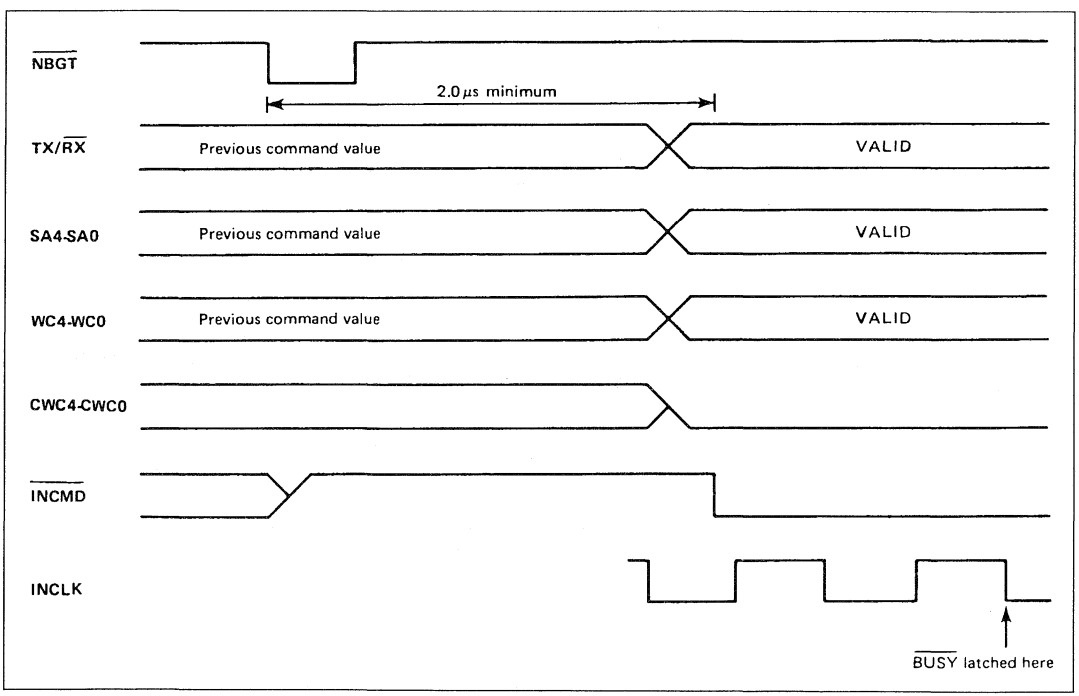


Figure 13: New Command Initialization

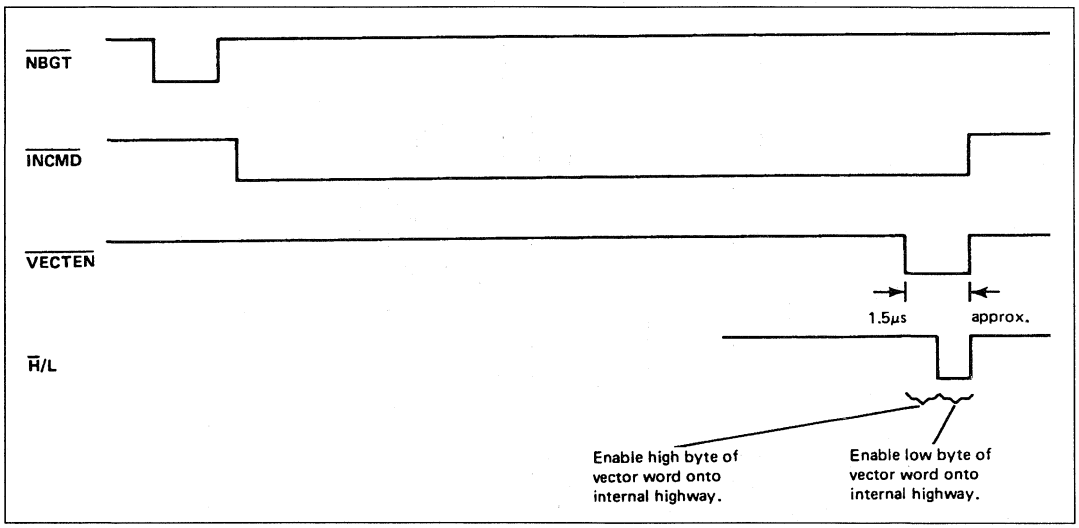


Figure 14: Transmit Vector Word Command

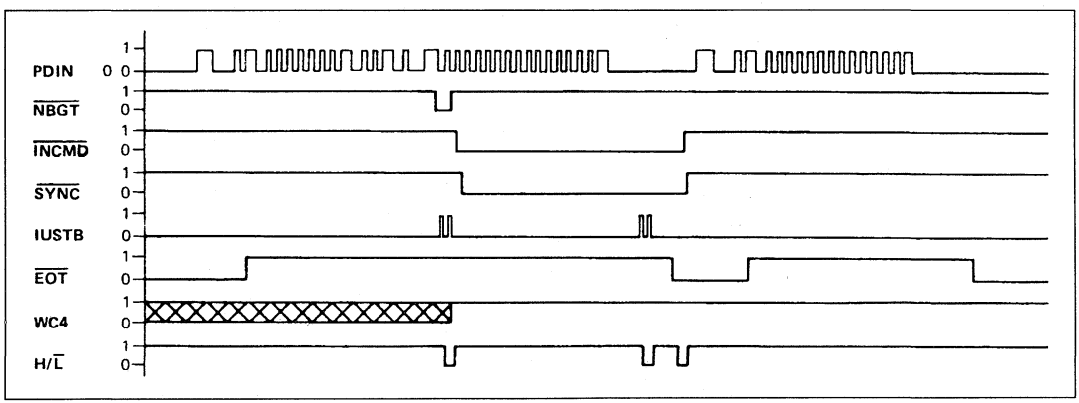


Figure 15: Synchronize (with data) Mode Command

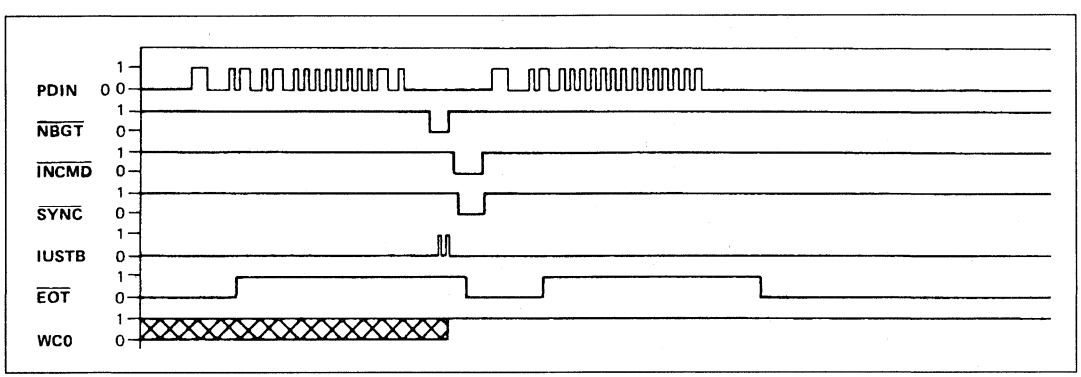


Figure 16: Synchronize (no data) Mode Command

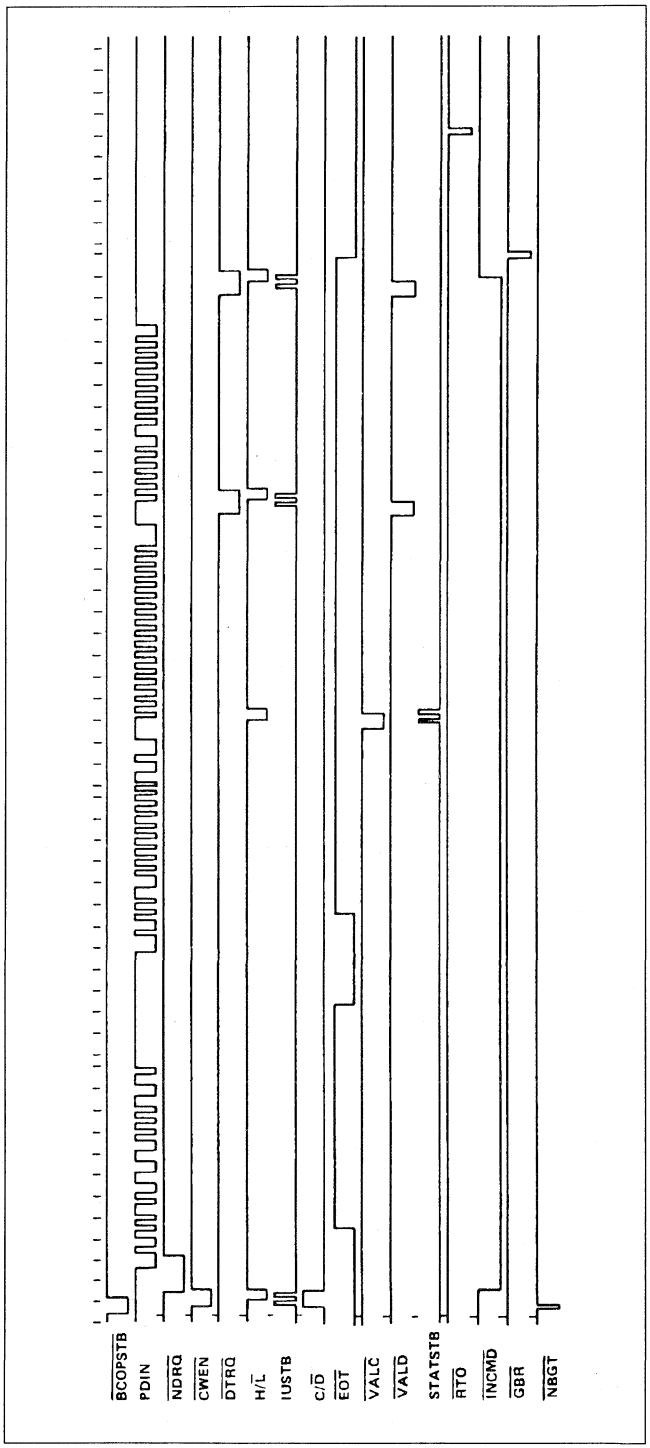


Figure 17: Bus Controller Sending Command to RT 10001 to Transmit Two Data Words

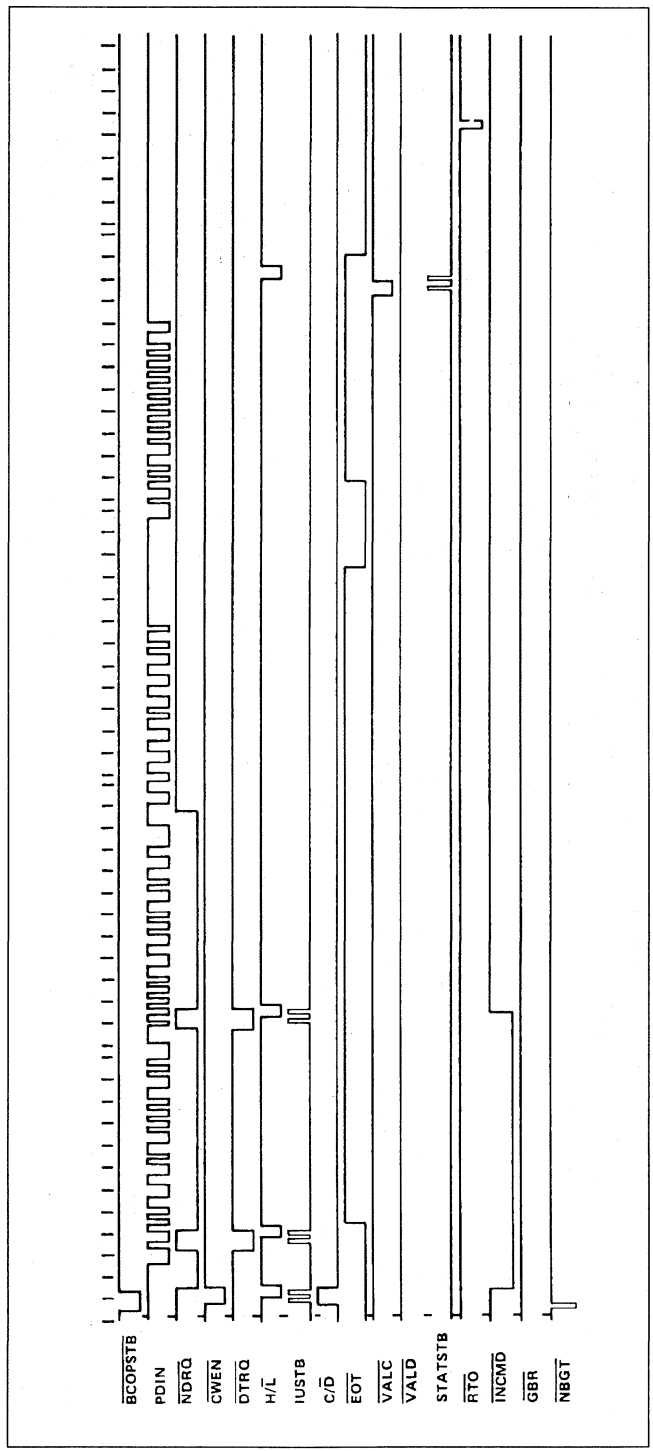


Figure 18: Bus Controller Sending Command to RT 10001 to Receive Two Data Words

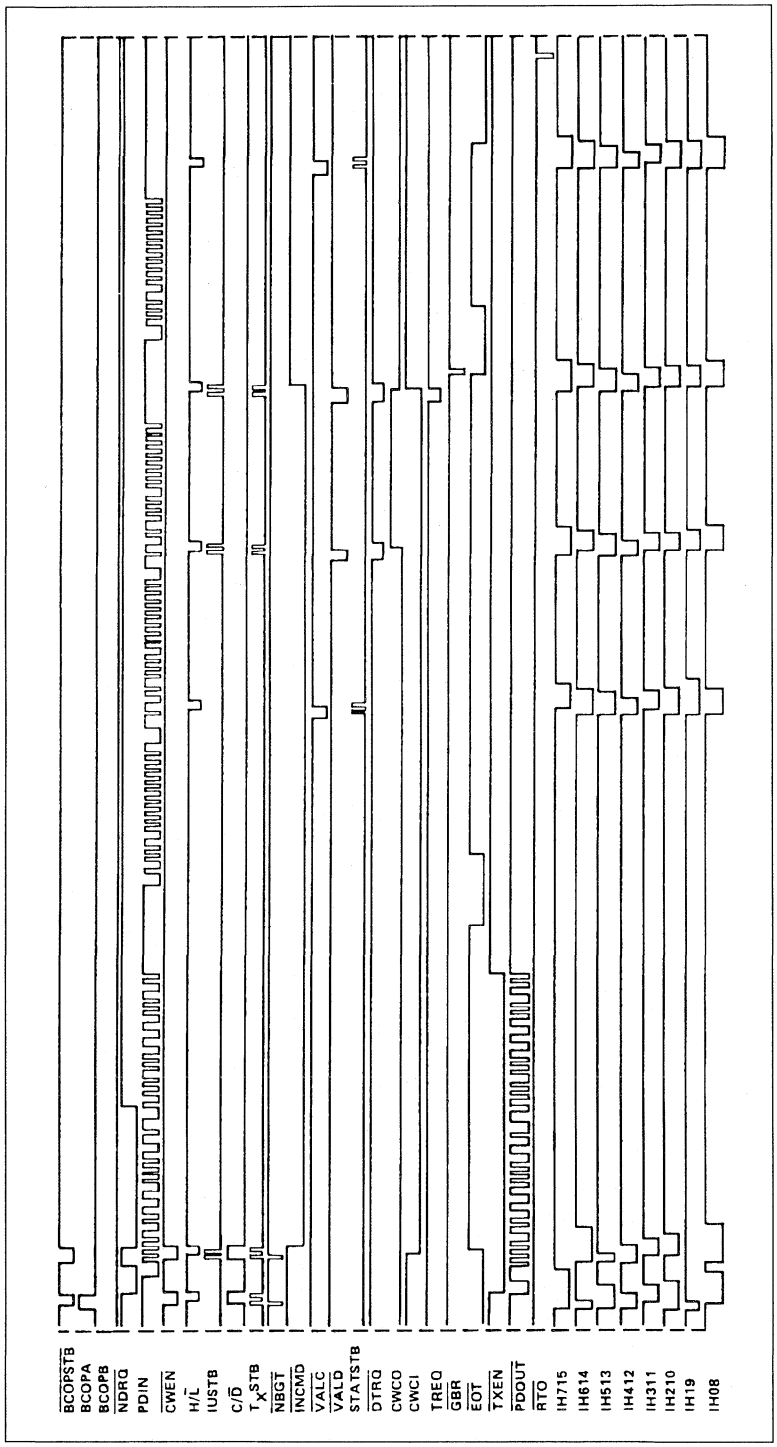


Figure 19: Bus Controller Commanding RT 10001 to Transmit Two Data Words to RTT 00001

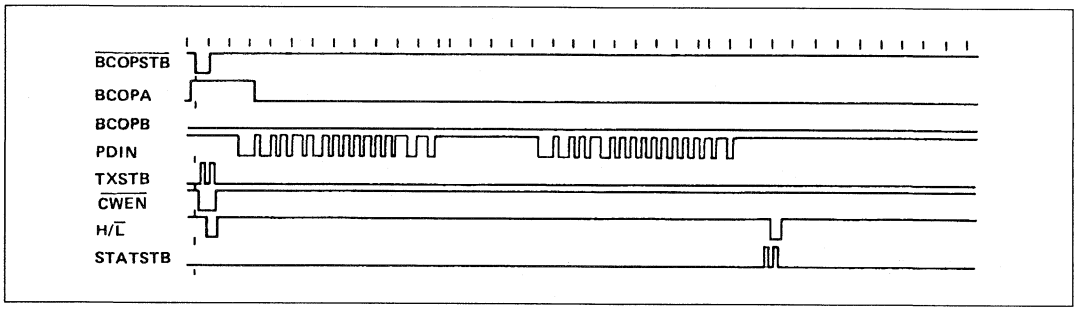


Figure 20: Bus Controller Sending Mode Command Transmit Status Word Mode Code 00010

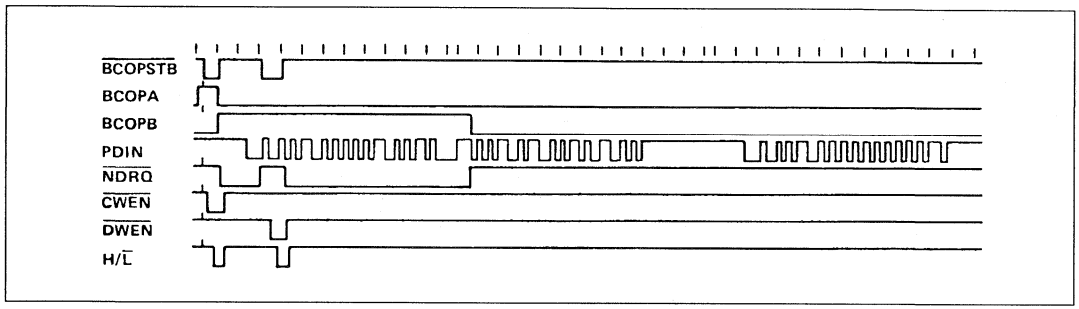


Figure 21: Bus Controller Sending Mode Command Synchronize Mode Code 1001

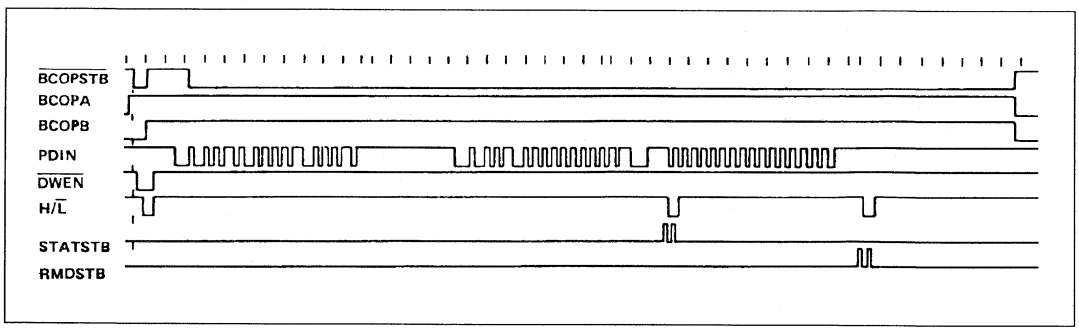
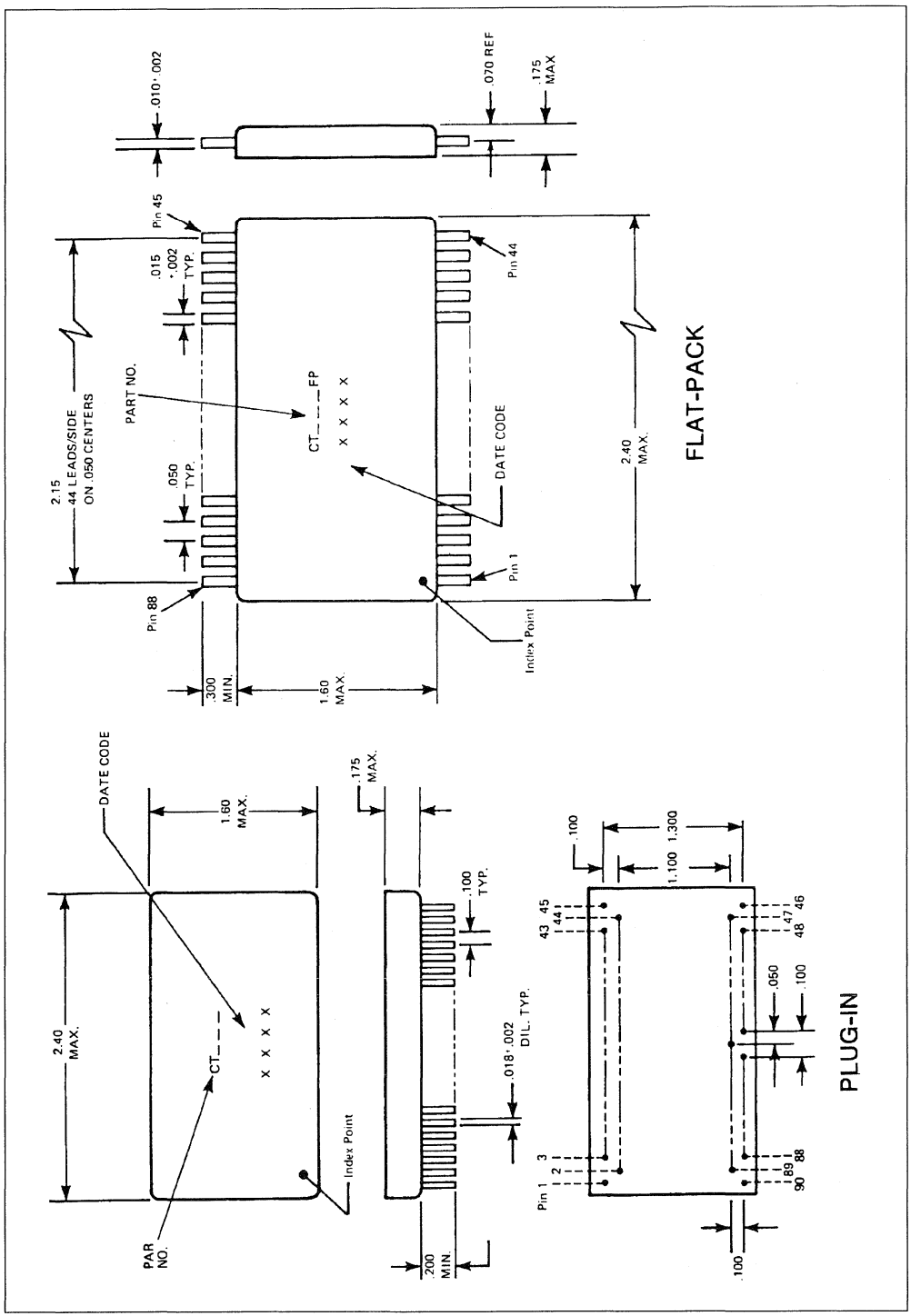


Figure 22: Bus Controller Sending Mode Command Transmit Vector Word Mode Code 10000



Package Outlines

PIN OUT

CT1610 and CT1602 Pin	CT1610FP and CT1602FP Pin	Function	CT1610 and CT1602 Pin	CT1610FP and CT1602FP Pin	Function
1	1	NC	46		NC
2	2	CWC 00 (LSB)	47	45	RTADPAR
3	3	SA 04 (MSB)	48	46	RTAD 00 (LSB)
4	4	SA 03	49	47	RTAD 01
5	5	SA 02	50	48	RTAD 02
6	6	CWC 04 (MSB)	51	49	RTAD 03
7	7	CWC 03	52	50	RTAD 04 (MSB)
8	8	CWC 02	53	51	CMSYNC*
9	9	CWC 01	54	52	DWSYNC*
10	10	GBR*	55	53	BCSTEN 00
11	11	H/L*	56	54	RX DATA 0
12	12	STATEN*/STATSTB	57	55	RX DATA* 0
13	13	EOT*	58	56	BCSTEN 01
14	14	SA 01	59	57	RTO*
15	15	SA 00 (LSB)	60	58	6 MCK
16	16	INCMD*	61	59	ERROR*
17	17	TX/RX*	62	60	LTFAIL*
18	18	DTRQ*	63	61	MANER*
19	19	VECTEN*/DWEN*	64	62	PARER*
20	20	NBGT*	65	63	VALD*
21	21	SYNC*	66	64	RTADER*
22	22	INCLK	67	65	RX DATA 01
23	23	IUSTB	68	66	RX DATA* 01
24 (2)	24 (2)	BUF INH*	69	67	+5 VIN
25	25	DTAK*	70	68	TX INHIBIT 01
26	26	BCOPA	71	69	TX INHIBIT 00
27	27	BCOPSTB*	72	70	TX DATA
28	28	BCOPB	73	71	TX DATA*
29	29	PASMON*	74	72	SERVREQ*
30	30	NDRQ*	75	73	TXTO*
31	31	REQBUSB	76	74	DBCACC*
32	32	REQBUSA	77	75	RESET*
33	33	COMMON & CASE	78	76	RT/BC*
34 (2)	34 (2)	IH DIR	79	77	DBCREQ*
35	35	NC	80	78	HSFAIL*
36 (2)	36 (2)	IH ENA*	81	79	LSTCMD*/CWEN*
37	37	IH 00/08 (LSB)	82	80	BITEN*/RMDSTB
38	38	IH 01/09	83	81	BUSY*
39	39	IH 02/10	84	82	WC 04 (MSB)
40	40	IH 03/11	85	83	WC 03
41	41	IH 04/12	86	84	WC 00 (LSB)
42	42	IH 05/13	87	85	SSERR*
43	43	IH 06/14	88	86	WC 02
44	44	IH 07/15 (MSB)	89	87	WC 01
45		NC	90	88	NC

KEY: * = True Low Signal
(2) = NO CONNECTION ON CT1610

3092-1.3 October 1991

CT1612

MIL-STD-1553B REMOTE TERMINAL, BUS CONTROLLER, OR PASSIVE MONITOR HYBRID WITH STATUS WORD CONTROL

GENERAL DESCRIPTION

The CT1612 design incorporates five LSI chips that accomplish the dual redundant MIL-STD-1553B Bus Controller and Remote Terminal Functions. A sixth LSI chip (CT7100) allows programming of the Terminal Flag and Subsystem Flag Status Bits and allows setting of the Message Error Bit by the Subsystem. The unit dissipates only 75mW and connects directly to all CTI single and dual transceivers. This CT1612 Data Sheet is designed to be used in conjunction with the GPS MIL-STD-1553B Monolithic Chip Set Booklet.

FEATURES

- Performs the complete dual-redundant Remote Terminal and Bus Controller Protocol Functions of MIL-STD-1553B
- Allows setting of the Message Error Bit on illegal commands
- Provides programmable control over Terminal Flag and Subsystem Flag Status Bits
- 75 mW typical power dissipation
- Compatible with all GPS Driver/Receiver Units
- Screened to applicable portions of MIL-STD-883 Level B
- Small size
- Available in plug-in or flatpack configuration
- 5V DC operation
- -55°C to +125°C operation

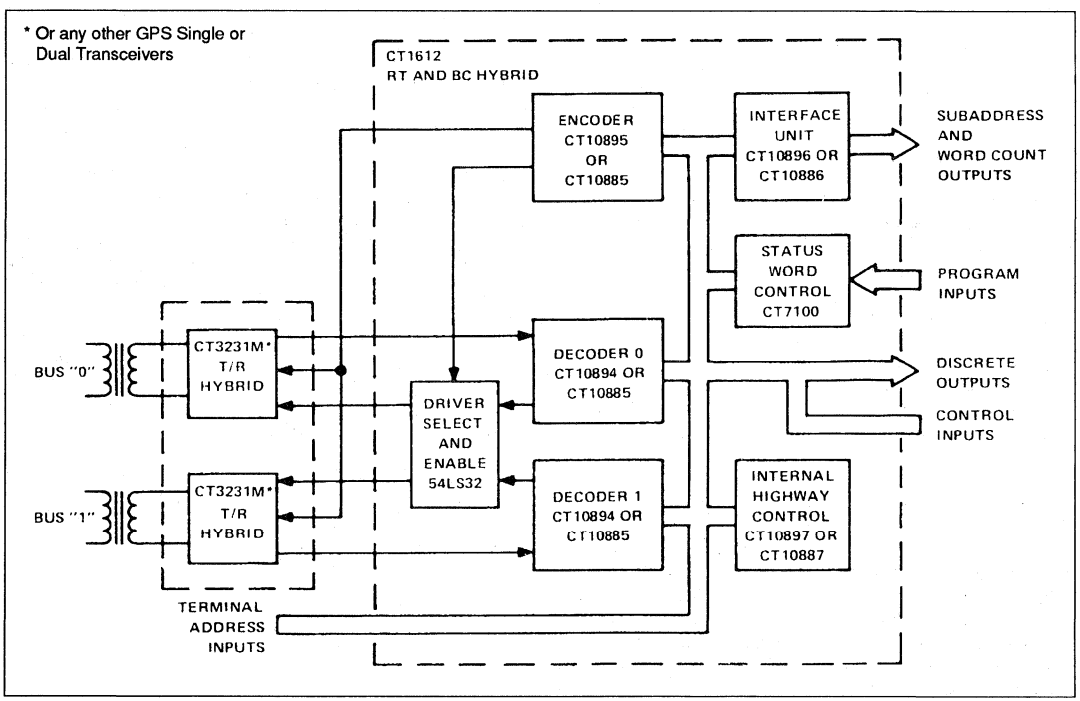


Figure 1: Functional Diagram

REMOTE TERMINAL OPERATION

RECEIVE DATA OPERATION

All valid Data Words associated with a valid Receive Data Command Word for the Remote Terminal (RT) are passed to the subsystem. The RT examines all Command Words from the bus and will respond to valid (i.e. correct Manchester, Parity Coding, etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the Data Words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 us Intervals. This applies to Receive Data Words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words has been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these Data Words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

TRANSMIT DATA OPERATION

If the RT receives a valid Transmit Data Command addressed to the RT, then the RT will request the Data Words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each Data Word, the next word is requestcd by the RT as soon as the transmission of tile current word has commenced.

It is essential that the subsystem should provide all the Data Words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

CONTROL OF DATA TRANSFERS

This section describes the detailed operation of the data transfer mechanism between the RT and subsystems. It covers the operations of the signals $\overline{DTRQ}$, $\overline{DTAK}$, IUSTB, H/$\overline{L}$, $\overline{GBR}$, $\overline{NBGT}$, and TX/$\overline{RX}$ during receive data and transmit data transfers.

Figure 6 shows the operation of the data handshaking signals during a Receive Command with two Data Words. When the RT has fully checked the Command Word, $\overline{NBGT}$ is pulsed low, which can be used by the subsystem as an initialization signal. TX/$\overline{RX}$ will be set low indicating a Receive Command; however, if $\overline{ENABLE}$ is held active (low), the TX/$\overline{RX}$ line will pulse to its opposite state for 80 to 300 ns starting from 100 to 300 ns after the falling edge of $\overline{INCMD}$, as shown in Figure 12. When the first Data Word has been fully validated, $\overline{DTRQ}$ is set low. The subsystem must then reply within approximately 1.5 us by setting $\overline{DTAK}$ low. This indicates to the RT that the subsystem is ready to accept data. The Data Word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{L}$ as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 11.

If the subsystem does not declare itself busy, then it must respond to $\overline{DTRQ}$ going low by setting $\overline{DTAK}$ low within approximately 1.5 us. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. $\overline{DTRQ}$ being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, $\overline{GBR}$ is pulsed low if the block isentirely correct and valid. This is used by the subsystem as permission to make use of the data block. If no $\overline{GBR}$ signal is generated, then an error has been detected by the RT and the entire data block is invalid and no Data Words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical fashion but there will be a delay of approximately 70 us between $\overline{NBGT}$ going low and $\overline{DTRQ}$ first going low. See Figure 9.

Figure 5 shows the operation of the data handshaking signals during Transmit Command with three Data Words. As with the Receive Command discussed previously, $\overline{NBGT}$ is pulsed low if the command is valid and for the RT. TX/$\overline{RX}$ will be set high indicating aTransmit Data Command; however, if $\overline{ENABLE}$ is held active (low), the TX/$\overline{RX}$ line will pulse to its opposite state for 80 to 300 ns starting from 100 to 300 ns after the falling edge of $\overline{INCMD}$, as shown in Figure 12. While the RT is transmitting its Status Word, it requests the first Data Word from the subsystem by setting $\overline{DTRQ}$ low. The subsystem must then reply within approximately 13.5 us by setting $\overline{DTAK}$ low. By setting $\overline{DTAK}$ low, the subsystem is indicating that it has the Data Word ready to pass to the RT. Once $\overline{DTAK}$ is set low by the subsystem, $\overline{DTRQ}$ should be used together with H/$\overline{L}$ and TX/$\overline{RX}$ to enable first the high byte and then the low byte of the Data Word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{DTRQ}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 10.

ADDITIONAL DATA INFORMATION SIGNALS

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{INCMD}$, the subaddress lines SA0-SA4,the word count lines WC0-WC4, and current word count lines CWC0-CWC4. Use of these signals is optional.

$\overline{INCMD}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, Transmit/Receive Bit, and word count from the Command Word are all made available to the subsystem as SA0-SA4, TX/$\overline{RX}$, and WC0WC4, respectively. They may be sampled when $\overline{INCMD}$ goes low and will remain valid while INCMD is low, except as noted for TX/RX in the preceding section.

The subaddress is intended to be used by the subsystem as an address pointer for the data block. Subaddress 0 and 31 are Mode Commands, and there can be no receive or transmit data blocks associated with these. (Any Data Word associated with a Mode Command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.)

The TX/$\overline{RX}$ signal indicates the direction of data transfer across the RT-subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32

The current word count is set to 0 at the beginning of a new message and is incremented following each Data Word transfer across the RT-subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer.) There is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

SUBSYSTEM USE OF STATUS BITS AND MODE COMMANDS

General Description

The CT1612 allows full use to be made of all the Status Bits, and also implements all the Mode Commands. Inclusion of the CT7100 array allows external programming of the Terminal Flag and Subsystem Flag Bits olus setting of the Message Error Bit on reception of an illegal command when externally decoded. The subsystem is given the opportunity to make use of Status Bits, and is only involved in Mode Commands which have a direct impact on the subsystem.

The Mode Commands in which the subsystem may be involved are Synchronize, Synchronize with Data Word, Transmit Vector Word, Reset, and Dynamic Bus Control Allocation. The Status Bits to which the subsystem has access, or control are Service Request, Busy, Dynamic Bus Control Acceptance, Terminal Flag, Subsystem Flag, and Message Error Bit. Operation of each of these Mode Commands and of the Status Bits is described in the following sections.

All other Mode Commands are serviced internally by the RT. The Terminal Flag and Message Error Status Bits and BIT Word contents are controlled by the RT; however the subsystem has the option to set the Message Error Bit and to control the reset conditions for the Terminal Flag and Subsystem Flag Bits in the Status Word, and the Transmitter Timeout, Subsystem Handshake, and Loop Test Fail Bits in the BIT Word.

Synchronize Mode Commands

Once the RT has val idated the Command Word and checked for the correct address, the $\overline{SYNC}$ line is set low. The signal WC4 will be set low for Synchronize Mode Command (Figure 15) and high for a Synchronize with Data Word Mode Command (Figure 14). In a Synchronize With Date Word Mode Command, $\overline{SYNC}$ remains low during the time that the Data Word is received. Once the Data Word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{L}$ as the byte indicator (high byte first followed by low byte). $\overline{SYNC}$ being low should be used on the enable to allow IUSTB to clock Synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these Mode Commands, the $\overline{SYNC}$ signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figure 13 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word Mode Command. The RT requests data by setting $\overline{VECTEN}$ low. The subsystem should use H/$\overline{L}$ to enable first the high byte and then the low byte of the Vector Word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector Word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{VECTEN}$ goes low. If the subsystem has not been designed to handle the Vector Word Mode Command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the Mode Command, the RT will not be affected in any way by Vector Word circuitry not being implemented in the subsystem. It will however transmit a Data Word as the Vector Word, but this word will have no meaning.

Reset Mode Command

Figure 7 shows the relevant signal timings for an RT receiving a valid Reset Mode Command. Once the command Word has been fully validated and serviced, the $\overline{RESET}$ signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This Mode Command is intended for use with a terminal which has the capability of configuring itself into a Bus Controller on command from the bus. The line $\overline{DBCREQ}$ cannot go true unless the $\overline{DBCACC}$ line was true at the time of the valid command (i.e. tied low). For terminals acting only as RTs, the signal $\overline{DBCACC}$ should be tied high (inactive), and signal $\overline{DBCREQ}$ should be ignored and left unconnected.

Use of Busy Status Bit

The Busy Bit is used by the subsystem to indicate that il is not ready to handle data transfers either to or from the RT .

The RT sets the bit to logic "1" if the $\overline{\text{BUSY}}$ line from the subsystem is active low at the time of the second falling edge of INCLK after $\overline{\text{INCMD}}$ goes low. This is shown in Figure 12. Once the Busy Bit is set, the RT will stop all Receive and Transmit Data Word transfers to and from the subsystem.The data transfers in the Synchronize with Data Word and Transmit Vector Word Mode Commands are not affected by the Busy Bit and will take place even if it has been set.

It should be noted that minimum of 0.5 us subaddress decoding time is given to the subsystem before setting of Status Bits. This allows the subsystem to selectively set the Busy Bit if for instance one subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of Service Request Status Bit

The Service Request Bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested

The timing of the setting of this bit is the same as the Busy Bit and is shown in Figure 12. Use of $\overline{\text{SERVREQ}}$ has no effect on the RT apart from setting the Service Request Bit .

It should be noted that certain Mode Commands require that the last Status Word be transmitted by the RT instead of the current one, and therefore a currently set Status Bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{\text{SERVREQ}}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This Status Bit is used by the RT to indicate a subsystem fault condition If the subsystem sets $\overline{\text{SSERR}}$ low, the subsystem fault condition in the RT will be set, and the Subsystem Flag Status Bit will subsequently be set. The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset Mode Command or as described in the Optional Status Word Control section. It should be noted that if $\overline{\text{ENABLE}}$ has been selected (held low) and a subsystem fault is to be reported by pulling $\overline{\text{SSERR}}$ low, then the $\overline{\text{SSERR}}$ line must be latched low until the fault condition no longer exists.

Dynamic Bus Control Acceptance Status Bit

$\overline{\text{DBCACC}}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{\text{DBCREQ}}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required, then $\overline{\text{DBCACC}}$ must be tied high. $\overline{\text{DBCACC}}$ tied high inhibits $\overline{\text{DBCREQ}}$ and clears BIT TIME 18 in the status response.

OPTIONAL STATUS WORD CONTROL

Message Error Bit

The CT1612 monitors all receptions for errors and sets the Message Error Bit as prescribed in MIL-STD-1553B. The subsystem designer may, however, exercise the option of monitoring for illegal commands and forcing the Message Error Bit to be set.

The word count and subaddress lines for the current comrnand are valid when $\overline{\text{INCMD}}$ goes low. The subsystem must then determine whether or not the word count or subaddress is to be considered illegal by the RT. If either of them is considered illegal, the subsystem must produce a positive-going pulse called MEREQ. The positive-going edge of MEREQ must occur within 500 ns of the falling edge of $\overline{\text{INCMD}}$.

Subsystem Flag and Terminal Flag Bits

The conditions that cause the Subsystem Flag and Terminal Flag Bits in the Status Word to be reset may be controlled by the subsystem using the $\overline{\text{ENABLE}}$, $\overline{\text{BIT DECODE}}$, $\overline{\text{NEXT STATUS}}$, and $\overline{\text{STATUS UPDATE}}$ inputs. If $\overline{\text{ENABLE}}$ is inactive (high), then the Terminal Flag and Subsystem Flag behavior is the same as described in the CTI MIL-STD-1553B Monolithic Chip Set Booklet (i.e. the other three option lines are disabled). If $\overline{\text{ENABLE}}$ is held low, then the three options described below are available and are essentially independent. Any, all, or none may be selected. Also, reporting of faults by the subsystern requires that $\overline{\text{SSERR}}$ be latched (not pulsed) low until the fault is cleared.

Resetting SSF and TF on Receipt of Valid Commands

If $\overline{\text{ENABLE}}$ is selected and the other three option lines are held high, then the Status Word Register will be reset on receipt of any valid command with the exception of Transmit Status and Transmit Last Command. Note that in this mode, the TF will never be seen in the Status Word, and the SSF will only be seen if $\overline{\text{SSERR}}$ is latched low. Also note that the SSF will not be seen in response to Transmit Status or Transmit Last Command if the preceding Status Word was clear, regardless of actions taken Oll the $\overline{\text{SSERR}}$ line after the clear status transmission.

Status Register Update at Fault Occurrence

If $\overline{\text{STATUS UPDATE}}$ is selected (held low), then the TF or SSF will appear in response to a Transmit Status or Transmit Last Command issued as the first command after the fault occurs. Any other command (except as noted in the Preserving the BIT Word section) will reset the TF and SSF. Repeated Transmit Status or Transmit Last Command immediately following the fault will continue to show the TF and/or SSF in the Status Word. Note that this behavior may not rneet the "letter-of-the spec" as described in MIL-STD-1553B, but is considered the "preferred" behavior by some users.

TF and SSF Reporting in the Next Status Word After the Fault

If $\overline{\text{NEXT STATUS}}$ is selected (held low), then the TF or SSF will appear in response to the very next valid command after the fault except for Transmit Status or Transmit Last Command. The flag(s) will be reset on receipt of any valid command following the status transmission with the flag(s) set except for Transmit Status, Transmit Last Command, or as noted in the following section on Preserving the BIT Word.

Preserving the BIT Word

In order to preserve the Transmitter Timeout Flag, Subsystem Handshake Failure, and Loop Test Failure Bits in the BIT Word, it is necessary to select $\overline{\text{BIT DECODE}}$ (hold it low). This will prevent resetting those bits if the Transmit Bit Word Mode Command immediately follows the fault or follows a Transmit Last Command or Transmit Status immediately following the fault. It will also prevent resetting the TF and SSF Bits in the Status Word. Any other valid commands will cause those BIT Word Bits and the Status Word Bits to be reset.

BUS DRIVER/RECEIVER INTERFACE

Receive Data

The decoder chip requires two TTL signals (PDIN and NDIN) to represent the data coming in from the bus. PDIN should be driven to a logic level "1" when the bus waveform exceeds a specified positive threshold and NDIN should be driven to a logic level "1" when a specified negative threshold is exceeded. During the quiet period on the bus, the signals should be at the same logic level. All the Bus Receivers must be permanently enabled, the selection of the bus in use is done within the chip set.

Transmit Data

The signals generated by the encoder chip ($\overline{\text{PDOUT}}$ and $\overline{\text{NDOUT}}$) are of the same format as the receive data. The only difference is that the TTL signals are negative logic (e.g. the signal is active when on logic level "0"). This means that when the encoder is quiet both $\overline{\text{PDOUT}}$ and $\overline{\text{NDOUT}}$ are at logic level "1". TX INHIBIT 0 and TX INHIBIT 1 enable the appropriate driver when it should be transmitting.

Figure 4 shows an example of a typical interface circuit between CT1612 and a driver/receiver unit.

BUS CONTROLLER OPERATION

To enable its use as a Bus Controller each chip in the chip set has additional logic within it. This logic can be enabled by pulling the pin labeled RT/$\overline{\text{BC}}$ low. Once the chip set is in Bus Control mode, all data transfers must be initiated by the Bus Control processor correctly commanding the chip set via the subsystem interface. In Bus Control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the CT1612 as a 1553B Bus Control interface, the Bus Control processor must be able to carry out four basic bus-related functions. Two inputs (BCOPA and BCOPB) allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{\text{BCOPSTB}}$ input. $\overline{\text{BCOPSTB}}$ must only be strobed low when $\overline{\text{NDRQ}}$ is high. This is particularly important when two options are required during a single transfer.

With these options all message types and lengths can be handled Normal BC/RT exchanges are carried out in the chip set option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{\text{BCOPSTB}}$. On receipt of the strobe, the CT1612 loads the Command Word from an external latch using $\overline{\text{CWEN}}$ and H/$\overline{\text{L}}$. The Command Word is transmitted down the bus. The TX/$\overline{\text{RX}}$ Bit is, however, considered by the chip set as being its inverse and so, if a Transmit Command is sent to an RT (Figure 16), the chip set in BC mode believes it has been given a Receive Command. As the RT returns the requested number of Data Words plus its status, the BC chip set carries out a full validation check and passesthe data into the subsystem using $\overline{\text{DTRQ}}$, $\overline{\text{DTAK}}$, H/$\overline{\text{L}}$, IUSTB, and CWC as in RT operation. It also supplies $\overline{\text{GBR}}$ at the endoof a valid transmission. Conversely, a Receive Command sent down the bus is interpreted by the BC chip set as a Transmit Command, and so the requisite Data Words are added to the Command Word (Fignre 17).

For Mode Commands, where a single Command Word is required, option one is selected by strobing $\overline{\text{BCOPSTB}}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the Command Word is loaded from the external latch using $\overline{\text{CWEN}}$ and H/$\overline{\text{L}}$, the correct Sync and Parity Bits are added and the word transmitted (Figure 19). Mode Commands followed by a Data Word require option two. Option two, selected by strobing $\overline{\text{BCOPSTB}}$ while BCOPA is low and BCOPB is high, loads a Data Word via $\overline{\text{DWEN}}$ and H/$\overline{\text{L}}$, adds Sync and Parity,and transmits them to the bus (Figure 20). If the mode code transmitted required the RT to return a Data Word, then selecting option three by strobing $\overline{\text{BCOPSTB}}$ when BCOPA and BCOPB are both high will identify that Data Word and if validated, output it to the subsystem interface using RMDSTB and H/$\overline{\text{L}}$. This allows Data Words resulting from mode codes to be identified differently from ordinary Data Words and routed accordingly (Figure 21). All received Status Words are output to the subsystem interface using STATSTB and H/$\overline{\text{L}}$.

In BC option three, if the signal $\overline{\text{PASMON}}$ is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for Command and Status Words or RMDSTB for Data Words.

RT to RT transfers require the transmission of two Command Words. A Receive Command to one RT is continguously followed by a Transmit Command to the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{\text{BCOPSTB}}$) for option zero must be delayed until $\overline{\text{NDRQ}}$ has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the Bus Controller processor (Figure 18).

NOTE: For all BC operations, BCOPA and BCOPB must remain valid and stable for a minimum of 1 us following the leading (negative-going) edge of $\overline{\text{BCOPSTB}}$.

PIN DESCRIPTION CT1612

Signal Mnemonic	Hybrid Sink or Source	Signal Description
BCOPA	SINK	Bus Control Operation A. Least significant bit of the Bus Controller operation select lines.
BCOPB	SINK	Bus Control Operation B. Most significant bit of the Bus Controller operation select lines.
$\overline{\text{BCOPSTB}}$	SINK	Bus Controller Operation Strobe. When functioning as a Bus Controller, a low-going pulse on this line will initiate the selected Bus Controller operation on the requested bus, using BCOPA&B and REQBUSA&B.
BCSTEN 0/1	SINK	Broadcast Enable. When low, the recognition of Broadcast Command is prevented on the specified bus.
$\overline{\text{BIT DECODE}}$	SINK	Built-In Test Decode. When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the BIT Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
$\overline{\text{BITEN}}$/RMDSTB	SOURCE	Built-In Test Enable/Receive Mode Data Strobe. This line pulses low when servicing a valid and legal Mode Command to transmit the internal BIT Word. This signal is for information only and must not be used to enable data from the subsystem. This line also double pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASMON}}$.
$\overline{\text{BUSY}}$	SINK	Busy. This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the chip set.
C/$\overline{\text{D}}$		Command/Data. Internal signal, not available to user.
$\overline{\text{CMSYNC}}$	SOURCE	Command Word Sync. This line goes low if a Command Word Sync and two Manchester Biphase Bits are valid.
CWC0-CWC4	SOURCE	Current Word Count. These five lines define which Data Word in the message is currently being transferred.
$\overline{\text{CWEN}}$		See $\overline{\text{LSTCMD/CWEN}}$.
$\overline{\text{DBCACC}}$	SINK	Dynamic Bus Control Accept. This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{\text{DBCREQ}}$	SOURCE	Dynamic Bus Control Request. This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the Accept Bit was set.
$\overline{\text{DTAK}}$	SINK	Data Transfer Acknowledge. Should be set low to indicate that the subsystem is ready for the data transfer.
$\overline{\text{DTRQ}}$	SOURCE	Data Transfer Request. Goes low to request a data transfer between the chip set and subsystem. Goes high at end of the transfer.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{DWEN}}$		See $\overline{\text{VECTEN/DWEN}}$.
$\overline{\text{DWSYNC}}$	SOURCE	Data Word Sync. This line goes low if a Data Word Sync and two Manchester Biphase Bits are valid.
$\overline{\text{ENABLE}}$	SINK	Enable. When held low, enables Bit Decode, Next Status, and Status Update program lines.
$\overline{\text{EOT}}$	SOURCE	End of Transmission. Goes low if a valid sync plus two Data Bits do not appear in time to be contiguous with preceding word.
$\overline{\text{ERROR}}$	SOURCE	Error. This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{\text{CMSYNC}}$ (RT mode) and also by $\overline{\text{RTO}}$ in the Bus Control mode.
$\overline{\text{GBR}}$	SOURCE	Good Block Received. Pulses low for 500 ns when a block of data has been received by the chip set and has passed all the validity and error checks.
H/$\overline{\text{L}}$	SOURCE	High/Low. Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{\text{HSFAIL}}$	SOURCE	Handshake Failure This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the chip set/subsystem data transfer handshaking .
IH08, IH19, IH210, IH311, IH412, IH513, IH614, IH715	SINK/ SOURCE	Internal Highway. Bidirectional 8-bit highway on which 16-bit words are passed in two bytes. IH715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
INCLK	SOURCE	Internal Clock (2 MHz). This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{INCMD}}$	SOURCE	In Command. Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
IUSTB	SOURCE	Interface Unit Strobe. This is a double pulse strobe used to transfer the two bytes of data.
$\overline{\text{LSTCMD/CWEN}}$	SOURCE	Last Command/Command Word Enable. This line pulses low when servicing a valid and legal Mode Command to Transmit Last Command. When in RT mode, this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a Command Word is required for transmission.
$\overline{\text{LTFAIL}}$	SOURCE	Loop Test Fail. This line goes low if any error in the terminal's own transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{\text{MANER}}$	SOURCE	Manchester Error. This line will pulse low if a Manchester error is detected by the decoder.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
MEREQ	SINK	Message Error Request. Positive-going edge will cause Message Error Bit in Status Word to be set.
$\overline{\text{NBGT}}$	SOURCE	New Bus Grant. Pulses low whenever a new command is accepted by the chip set.
$\overline{\text{NDRQ}}$	SOURCE	No Data Required. This line goes low if the encoder transmit buffer is full (i.e. another word is going to be transmitted). This signal is for information only and must not be used to enable data from the subsystem.
$\overline{\text{NEXT STAT}}$	SINK	Next Status. When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
$\overline{\text{PARER}}$	SOURCE	Parity Error. This line will pulse low if a parity error is detected by the decoder.
$\overline{\text{PASMON}}$	SINK	Passive Monitor. When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASMON}}$ remains low. All traffic on the bus will be handed, after validation,to the subsystem via STATSTB for Status and Commands Words, and RMDSTB for Data Words.
PDIN		Same as RX DATA.
$\overline{\text{PDOUT}}$		Same as TX DATA.
REQBUS A	SINK/ SOURCE	Request Bus A. This line, when in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, i.e. they are sources. When in Bus Control mode, these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	SINK/ SOURCE	Request Bus B. Most significant bit of the bus request lines. (See above for description.) Should be held low for BC operation and ignored for RT operation.
$\overline{\text{RESET}}$	SOURCE	Reset. This line pulses low for 500 ns on completion of the servicing of a valid and legal Mode Command to reset the RT.
RMDSTB		See $\overline{\text{BITEN}}$/RMDSTB.
RTAD0-RTAD4	SINK	RT Address Lines. These should be hardwired by the user. RTAD4 is most significant bit.
$\overline{\text{RTADER}}$	SOURCE	Remote Terminal Address Error. This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
RTADPAR	SINK	RT Address Parity. This must be hardwired by the user to give odd parity.
RT/$\overline{\text{BC}}$	SINK	Remote Terminal/Bus Control. This line, when high, causes the chip set to function as a remote terminal. When low, the chip set functions as a Bus Controller or Passive Monitor.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{RTO}}$	SOURCE	Reply Time Out. This signal will pulse low whenever quiet bus time has exceeded the reply time for a transmitting terminal. This line is intended for the Bus Controller use.
RX DATA 0/1	SINK	Positive Data In. This should be a TTL description of the positive half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined positive threshold is exceeded on the bus.
RX $\overline{\text{DATA}}$ 0/1	SINK	Negative Data In. This should be a TTL description of the negative half of the Manchester code data on the bus. It should be driven to a logic level "1" when a predetermined negative threshold is exceeded on the bus.
SA0-SA4	SOURCE	Subaddress. These five lines are a label for the data being transferred. Valid when $\overline{\text{INCMD}}$ is low.
$\overline{\text{SERVREQ}}$	SINK	Service Request. This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.
$\overline{\text{SSERR}}$	SINK	Subsystem Error. By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.
$\overline{\text{STATEN}}$/ STATSTB	SOURCE	Status Enable/Status Strobe. This line pulses low to enable the Status Word onto the internal highway for transmission. When in RT mode, this line must not be used to enable data from the subsystem. This line also double pulses high, when in the Bus Control mode, to strobe received Status Words into the subsystem. When $\overline{\text{PASMON}}$ is true, this line double pulses high for Command and Status Words.
$\overline{\text{STAT UPDATE}}$	SINK	Status Update. When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence.
$\overline{\text{SYNC}}$	SOURCE	Synchronize. Goes low when a Synchronize mode code is being serviced.
TREQ		Internal signal, not available to user.
TX DATA	SOURCE	Positive Data Out. When this signal goes high, the bus should be driven positive.
TX $\overline{\text{DATA}}$	SOURCE	Negative Data Out. When this signal goes high, the bus should be driven negative.
$\overline{\text{TXEN}}$		Transmitter Enable. Goes to a logic "0" when transmitting. Used to enable the bus drivers via TX INHIBIT. Internal signal, not available to user.
TX INHIBIT 0/1	SOURCE	Transmitter Enable. Goes low when the transmitter is transmitting. Should be used to enable the bus drivers.
TX/$\overline{\text{RX}}$	SOURCE	Transmit/Receive. The state of this line informs the subsystem whether it is to transmit or receive data. The signal is valid while $\overline{\text{INCMD}}$ is low.

Signal Mnemonic	Hybrid Sink or Source	Signal Description
$\overline{\text{TXTO}}$	SOURCE	Transmitter Time Out. This line goes low if the transmitter time out limits are exceeded.
$\overline{\text{VALC}}$		Valid Command. Internal signal, not available to user.
$\overline{\text{VALD}}$	SOURCE	Valid Data. This line will pulse low when a valid Data Word is received.
$\overline{\text{VECTEN}}$/ $\overline{\text{DWEN}}$	SOURCE	Vector Word Enable/Data Word Enable. In the RT mode, this signal is provided to enable the contents of the Vector Word latch (which is situated in the subsystem) onto the chip set's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
WC0-WC4	SOURCE	Word Count. These five lines specify the requested number of Data Words to be received or transmitted. Valid when $\overline{\text{INCMD}}$ is low.
6 MCK	SIN K	6 MHz Master Clock.

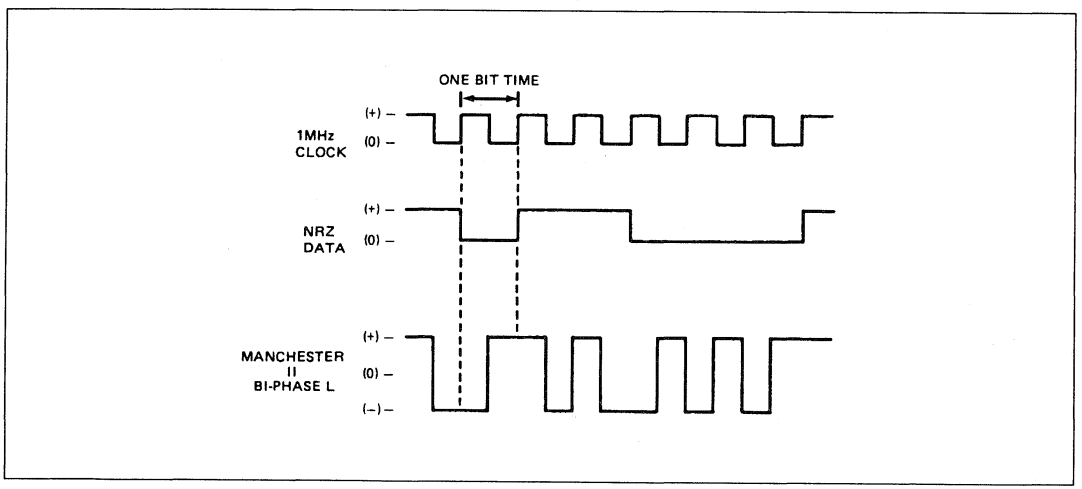


Figure 2: Data Encoding

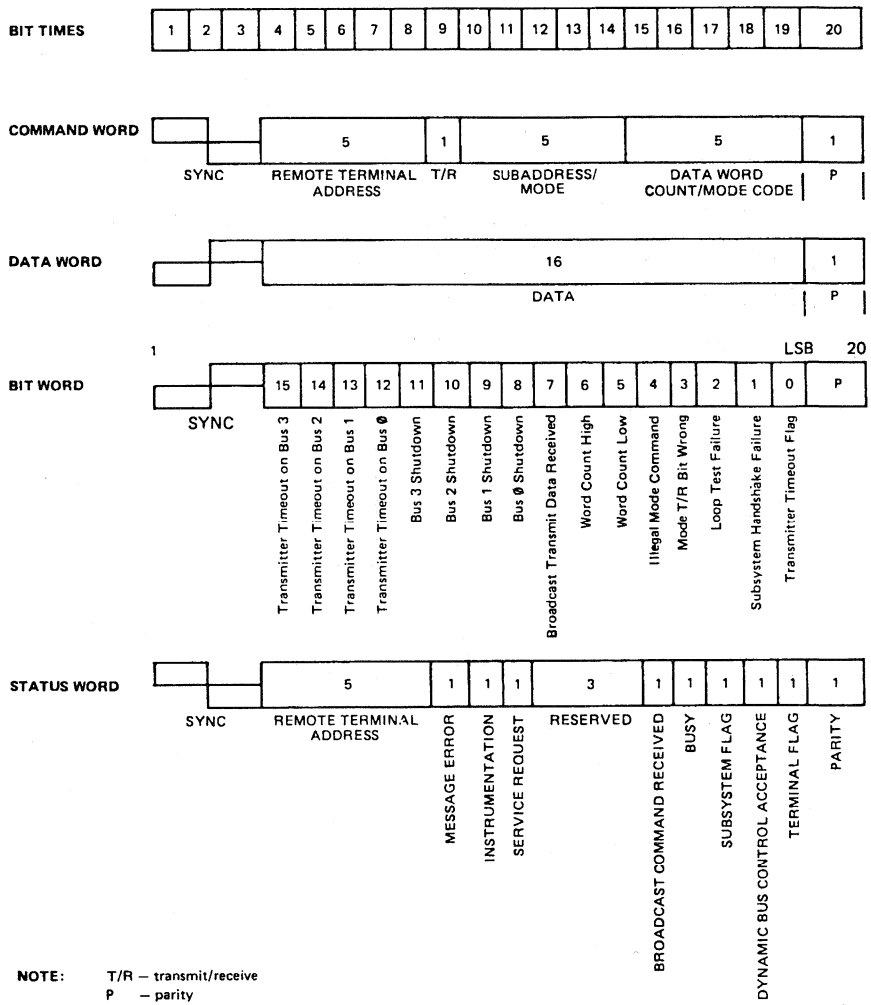


Figure 3: Word Formats

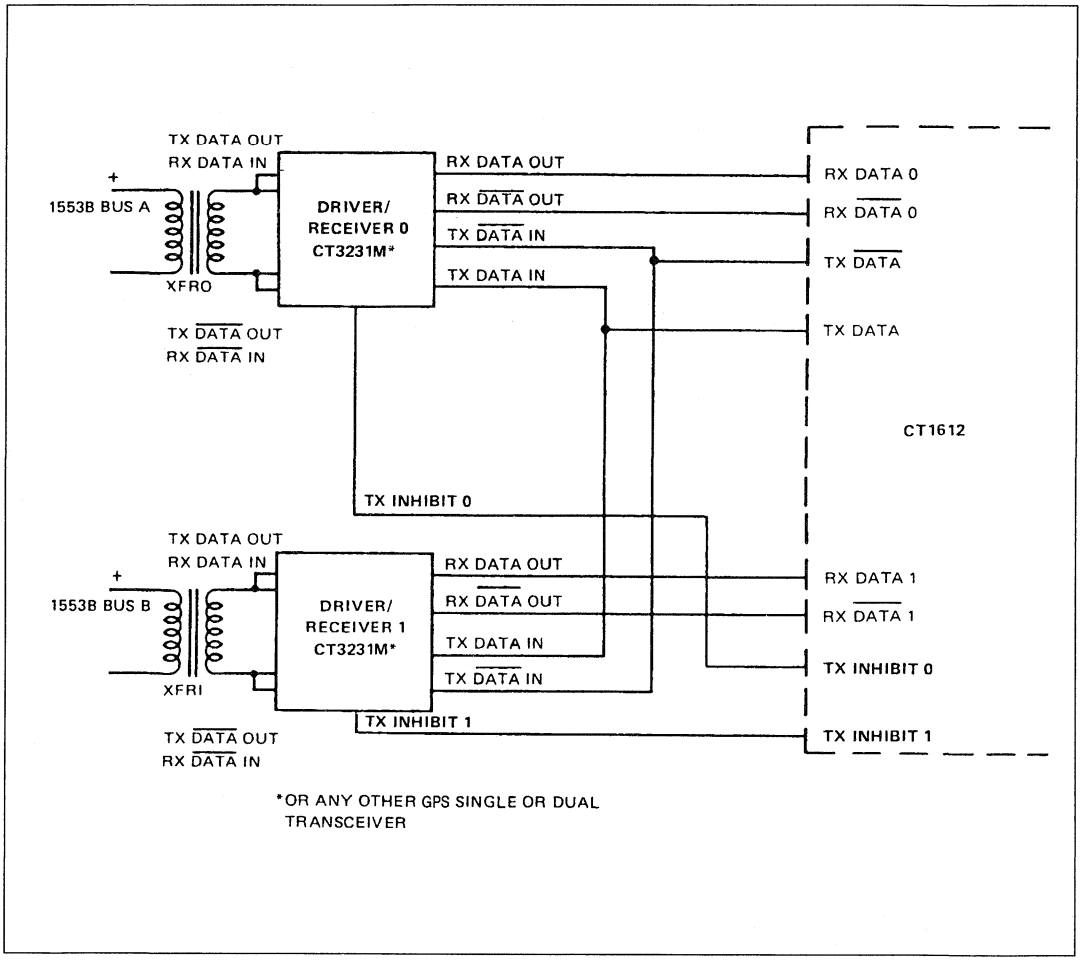


Figure 4: Examples of an interface between CT1612 and Driver/Receiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating free-air temperature	-55°C to +125°C
Storage temperature range	-65°C to +150°C

CLOCK REQUIREMENTS

Frequency	6.0 MHz
Stability -55° to +125°C	±0.01% (100ppm)
Maximum Asymmetry	60-40%
Rise/Fall Time	10 ns max
Output level TTL	Logic "0" 0.4v max Logic "1" 2.4v min

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNIT
SUPPLY VOLTAGE V_{CC}	4.5	5.0	5.5	V
HIGH LEVEL OUTPUT CURRENT I_{OH} 54LS32 (TTL) CT10894, CT10895, CT10896, CT10897 (CMOS)			 -400 -0.8	 uA mA
LOW-LEVEL OUTPUT CURRENT I_{OL} 54LS32 (TTL) CT10894, CT10895, CT10896, CT10897 (CMOS)			 4 2	 mA mA

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH} High - level input voltage	CMOS TTL	V_{CC}-1 2.0		V_{CC} V_{CC}	V V
V_{IL} Low - level input voltage	CMOS TTL	0 0		1.0 0.7	V V
V_{OH} High - level output voltage	V_{CC} = MIN I_{OH} = I_{OH} MAX CMOS TTL	 V_{CC}-0.5 2.4		 	 V V
V_{OL} Low - level output voltage	V_{CC} = MAX I_{OL} = I_{OL} MAX CMOS TTL			 0.5 0.4	 V V
I_{IH} High - level input current	V_{CC} = MAX, V_I = 0.4V PINS 45-50		-200 -400	-400 -500	uA uA
I_{IL} Low - level input current	V_{CC} = MAX, V_I = 2.4V PINS 45-50		-250 -640	-500 -800	uA uA
I_{CC} Supply Current	V_{CC} = MAX, All Inputs High			40	mA

NOTE: ALL MAX/MIN VALUES SHOWN ARE FOR WORST CASE OPERATING CONDITIONS, WHERE APPROPRIATE, AT -55°C or +125°C.

TIMING DIAGRAMS

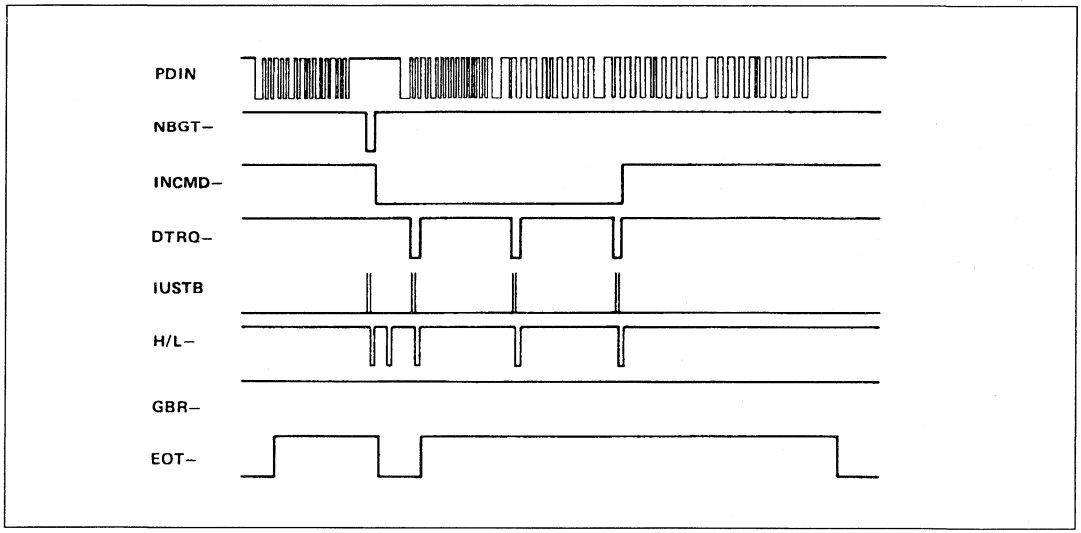


Figure 5: Transfer of Three Data Words from RT 03 to BC

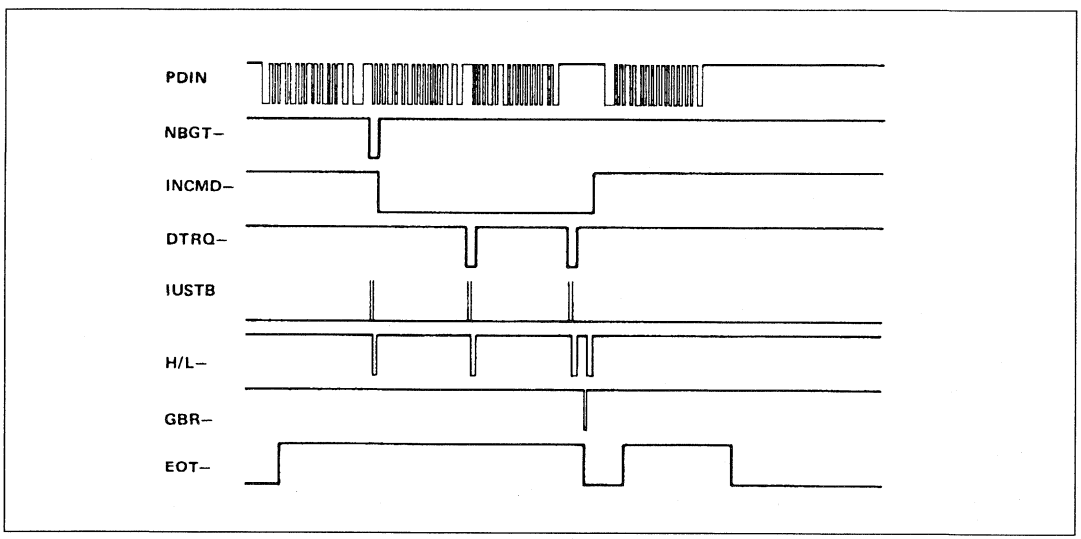


Figure 6: Transfer of Two Data Words from BC to RT 03

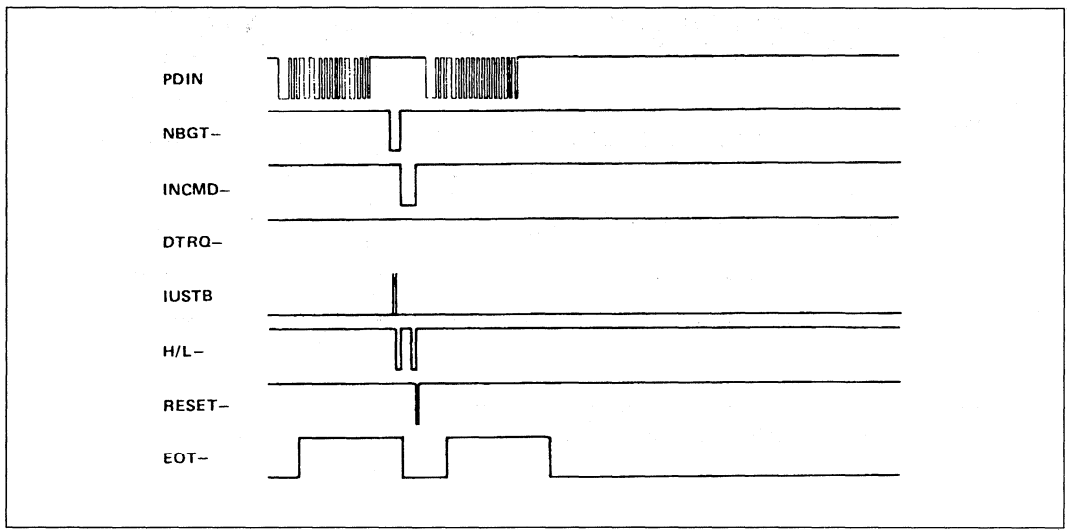


Figure 7: Mode Command Reset Remote Terminal

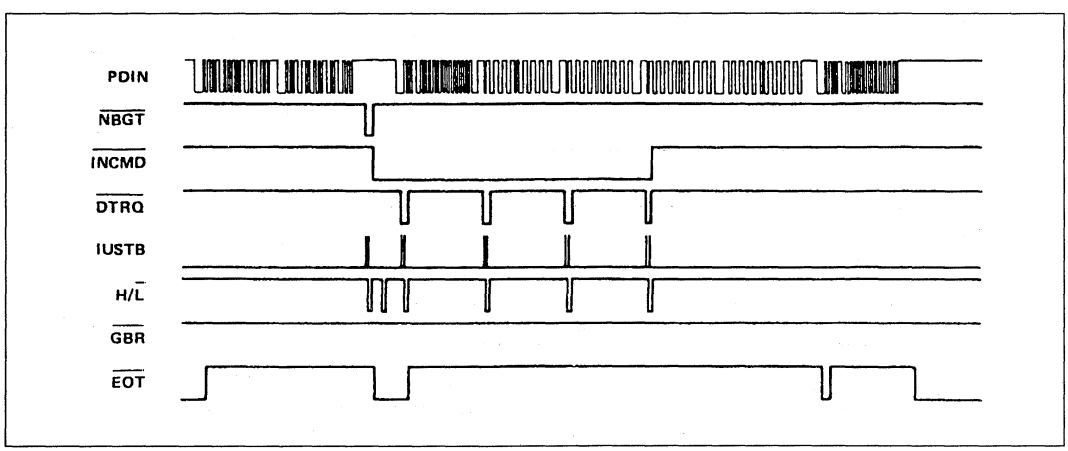


Figure 8: RT to RT Transfer of Four Data Words - This RT Sending the Data

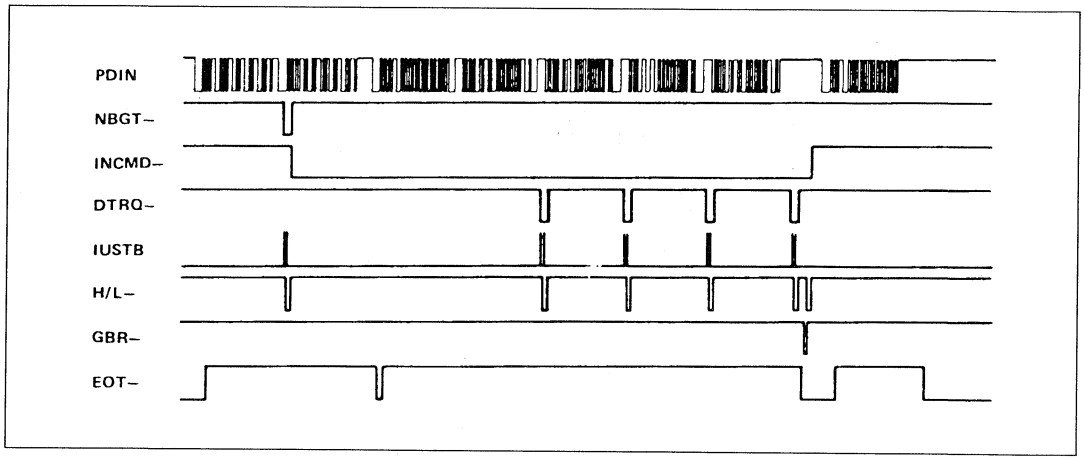


Figure 9: RT to RT Transfer of Four Data Words - This RT Receiving Data

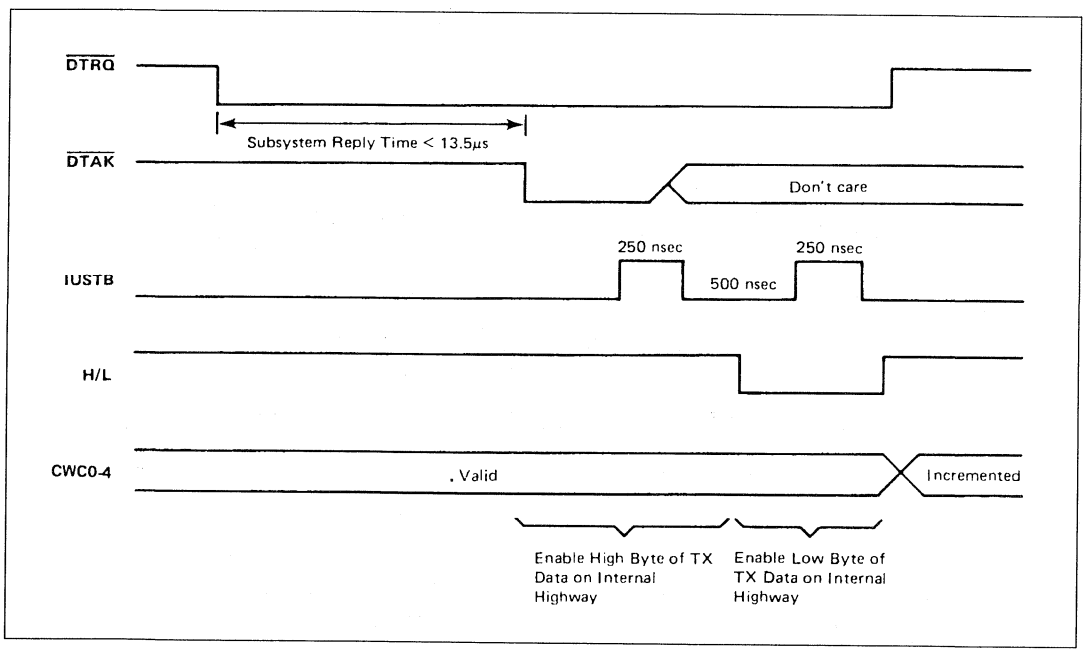


Figure 10: Handshaking for TX Data Transfers

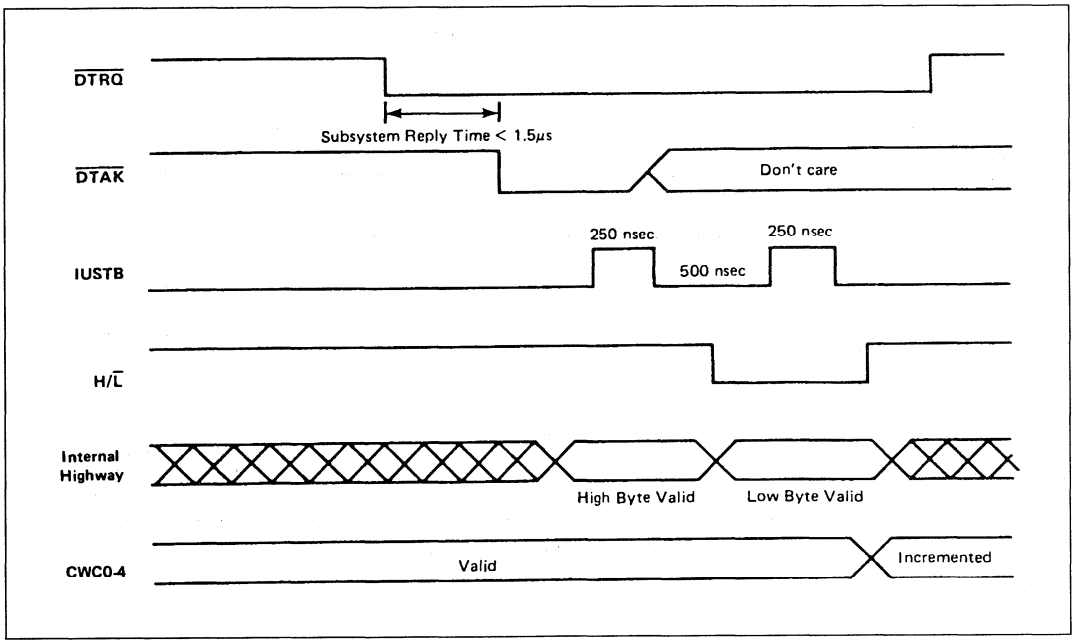


Figure 11: Handshaking for RX Data Transfers

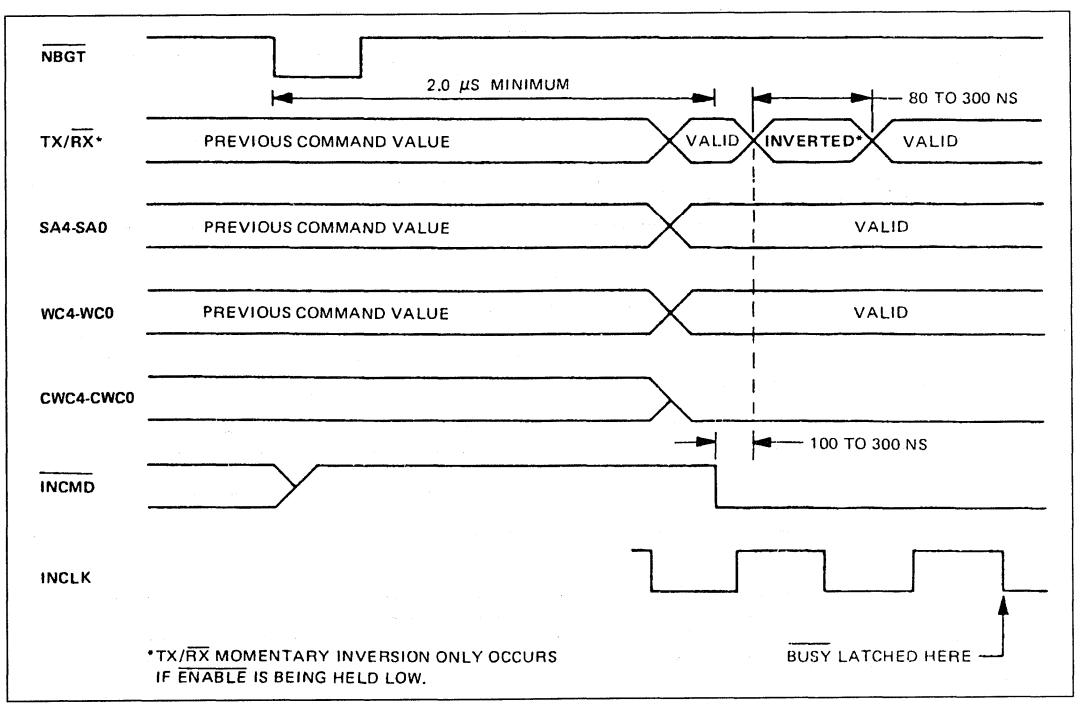


Figure 12: New Command Initialization

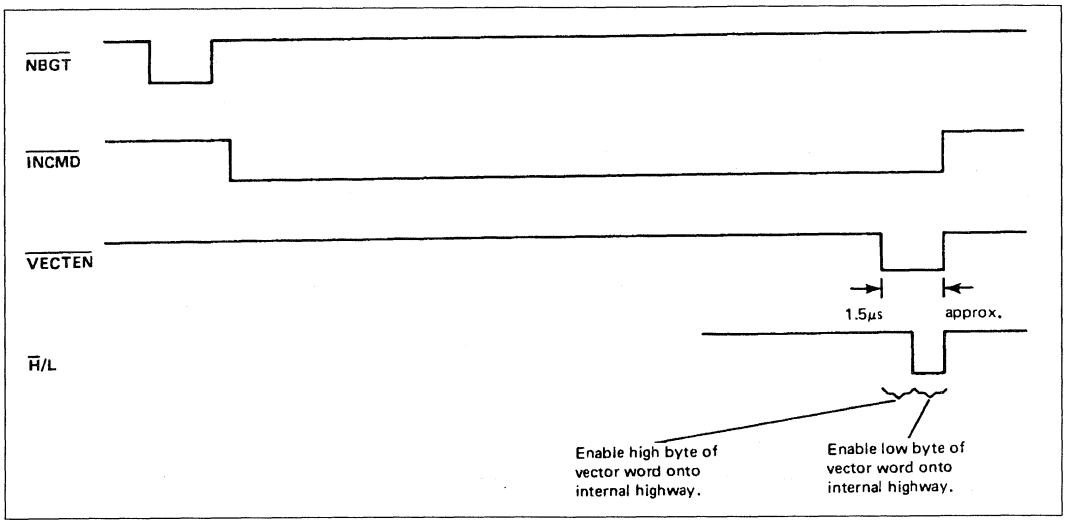


Figure 13: Transmit Vector Word Command

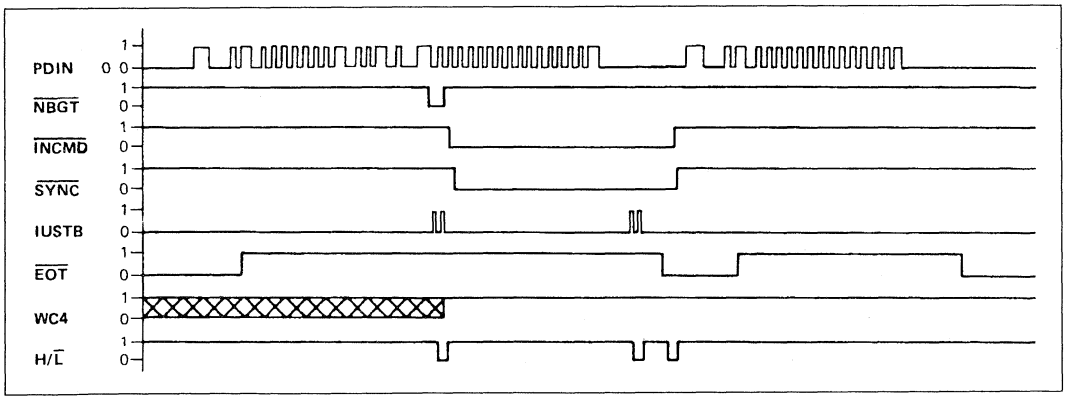


Figure 14: Synchronize (with data) Mode Command

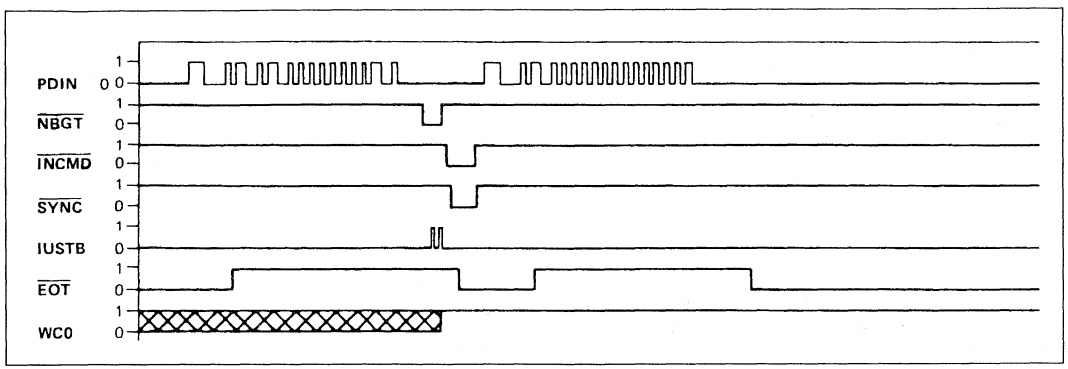


Figure 15: Synchronize (no data) Mode Command

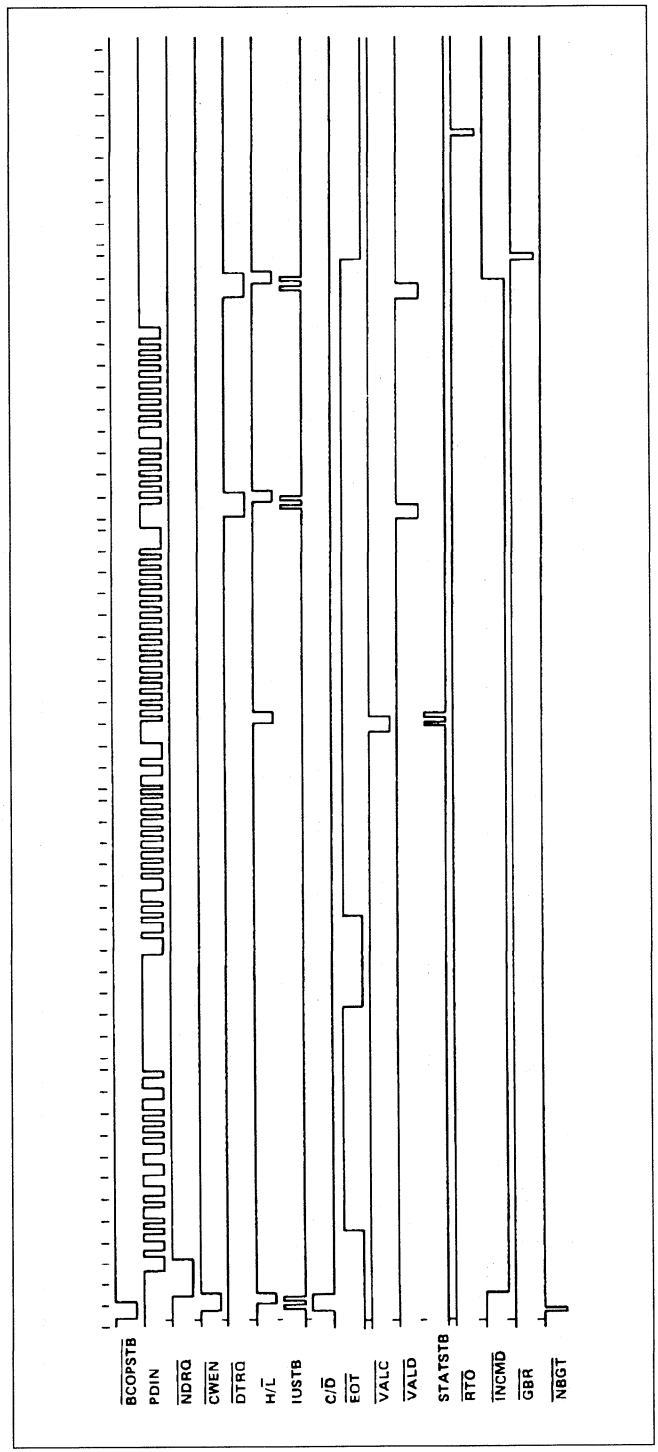


Figure 16: Bus Controller Sending Command to RT 10001 to Transmit Two Data Words

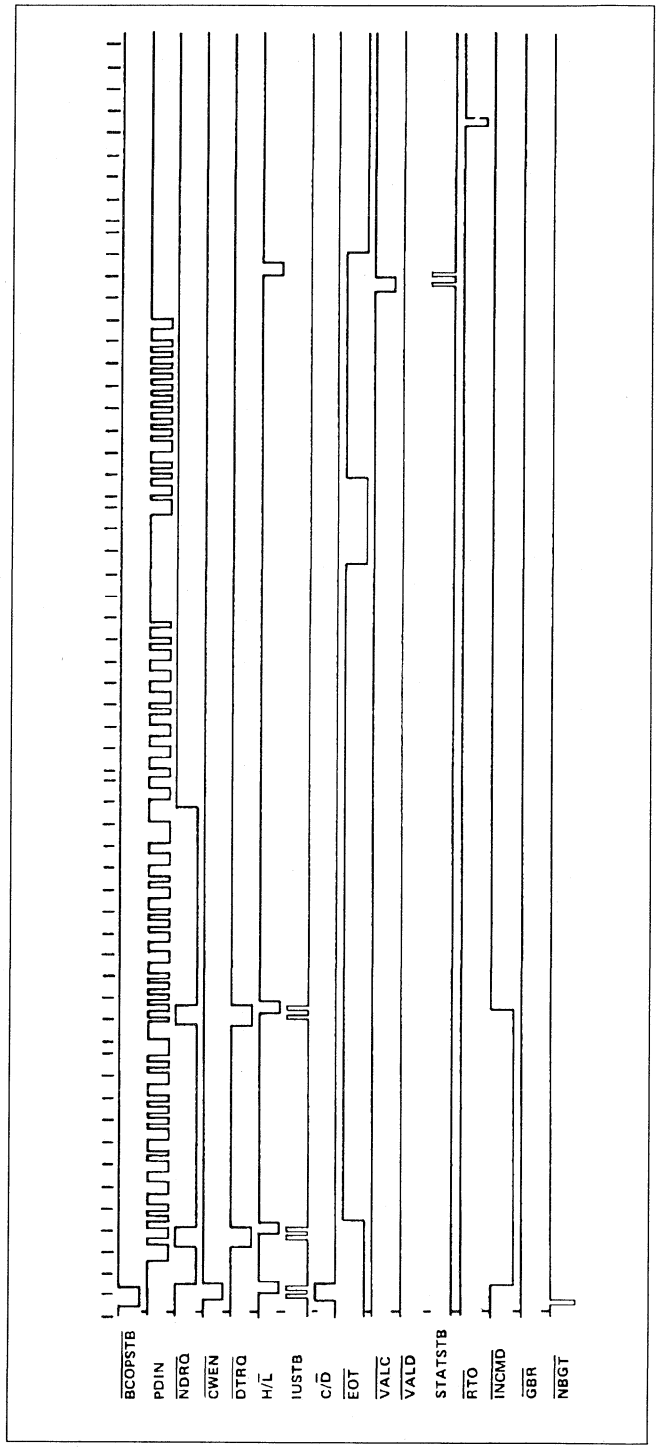


Figure 17: Bus Controller Sending Command to RT 10001 to Receive Two Data Words

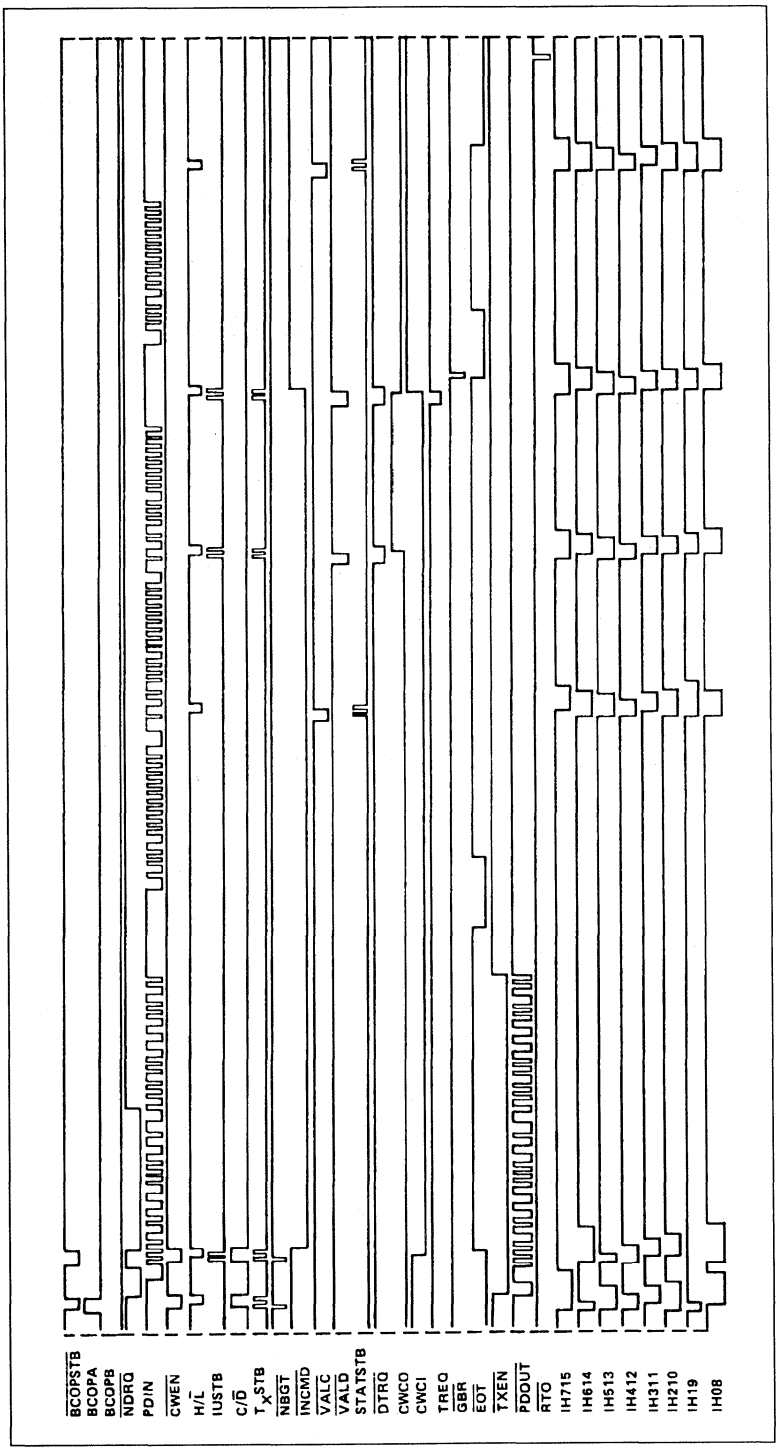


Figure 18: Bus Controller Commanding RT 10001 to Transmit Two Data Words to RTT 00001

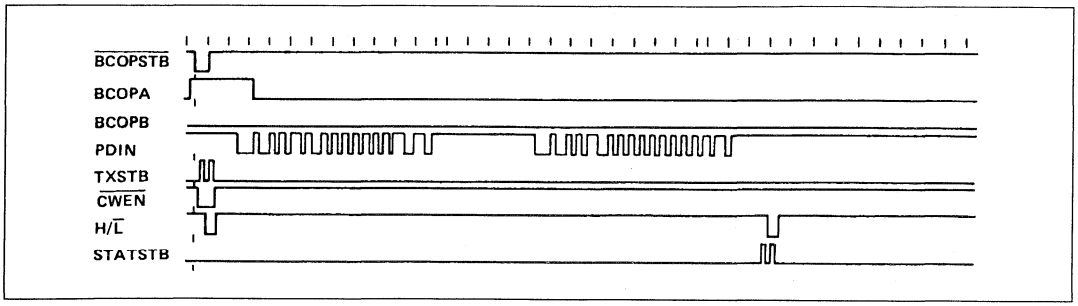


Figure 19: Bus Controller Sending Mode Command Transmit Status Word Mode Code 00010

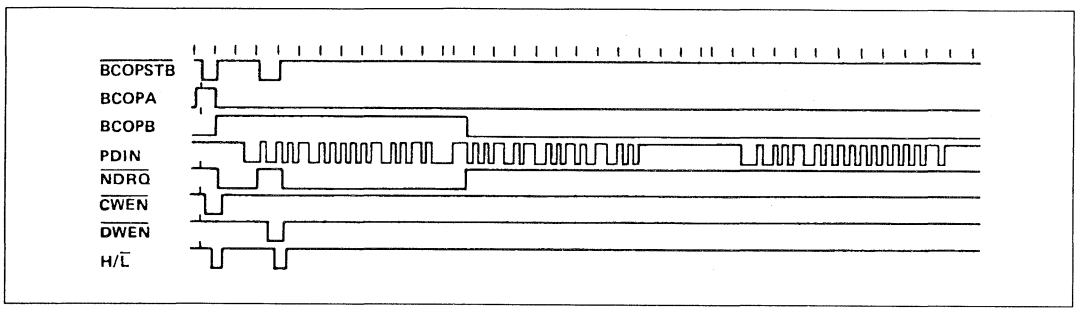


Figure 20: Bus Controller Sending Mode Command Synchronize Mode Code 10001

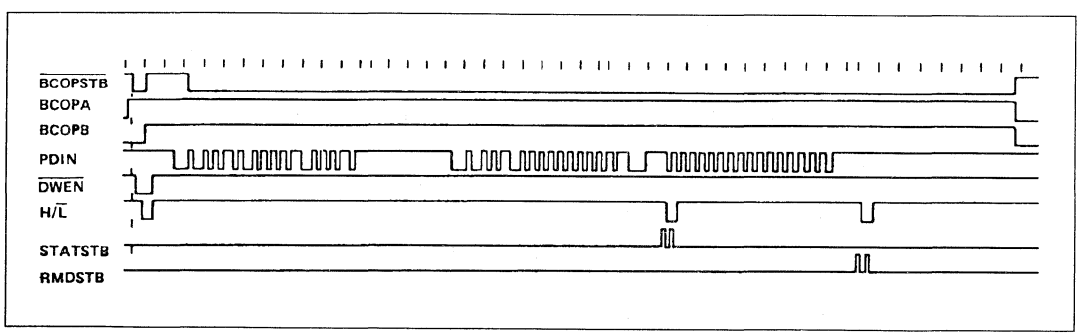


Figure 21: Bus Controller Sending Mode Command Transmit Vector Word Mode Code 10000

PIN DESCRIPTION

CT1612 Pin	CT1612FP Pin	Function
1	1	$\overline{\text{BIT DECODE}}$
2	2	CWC0 (LSB)
3	3	SA4 (MSB)
4	4	SA3
5	5	SA2
6	6	CWC4 (MSB)
7	7	CWC3
8	8	CWC2
9	9	CWC1
10	10	$\overline{\text{GBR}}$
11	11	H/$\overline{\text{L}}$
12	12	$\overline{\text{STATEN}}$/STATSTB
13	13	$\overline{\text{EOT}}$
14	14	SA1
15	15	SA0 (LSB)
16	16	$\overline{\text{INCMD}}$
17	17	TX/$\overline{\text{RX}}$
18	18	$\overline{\text{DTRQ}}$
19	19	$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$
20	20	$\overline{\text{NBGT}}$
21	21	$\overline{\text{SYNC}}$
22	22	INCLK
23	23	IUSTB
24	24	$\overline{\text{NEXT STAT}}$
25	25	$\overline{\text{DTAK}}$
26	26	BCOPA
27	27	$\overline{\text{BCOPSTB}}$
28	28	BCOPB
29	29	$\overline{\text{PASMON}}$
30	30	$\overline{\text{NDRQ}}$
31	31	REQBUSB
32	32	REQBUSA
33	33	COMMON AND CASE
34	34	$\overline{\text{ENABLE}}$
35	35	$\overline{\text{STAT UPDATE}}$
36	36	MEREQ
37	37	IH08 (LSB)
38	38	IH19
39	39	IH210
40	40	IH311
41	41	IH412
42	42	IH513
43	43	IH614
44	44	IH715 (MSB)
45		NC

CT1612 Pin	CT1612FP Pin	Function
46		NC
47	45	RTADPAR
48	46	RTAD0 (LSB)
49	47	RTAD1
50	48	RTAD2
51	49	RTAD3
52	50	RTAD4 (MSB)
53	51	$\overline{\text{CMSYNC}}$
54	52	$\overline{\text{DWSYNC}}$
55	53	BCSTEN 0
56	54	RX DATA 0
57	55	RX $\overline{\text{DATA}}$ 0
58	56	BCSTEN 1
59	57	$\overline{\text{RT0}}$
60	58	6 MCK
61	59	$\overline{\text{ERROR}}$
62	60	$\overline{\text{LTFAIL}}$
63	61	$\overline{\text{MANER}}$
64	62	$\overline{\text{PARER}}$
65	63	$\overline{\text{VALD}}$
66	64	$\overline{\text{RTADER}}$
67	65	RX DATA 1
68	66	RX $\overline{\text{DATA}}$ 1
69	67	+5 VIN
70	68	TX INHIBIT 1
71	69	TX INHIBIT 0
72	70	TX DATA
73	71	TX $\overline{\text{DATA}}$
74	72	$\overline{\text{SERVREQ}}$
75	73	$\overline{\text{TXT0}}$
76	74	$\overline{\text{DBCACC}}$
77	75	$\overline{\text{RESET}}$
78	76	RT/$\overline{\text{BC}}$
79	77	$\overline{\text{DBCREQ}}$
80	78	$\overline{\text{HSFAIL}}$
81	79	$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$
82	80	$\overline{\text{BITEN}}$/RMDSTB
83	81	$\overline{\text{BUSY}}$
84	82	WC4 (MSB)
85	83	WC3
86	84	WC0 (LSB)
87	85	$\overline{\text{SSERR}}$
88	86	WC2
89	87	WC1
90	88	NC

PACKAGE OUTLINES

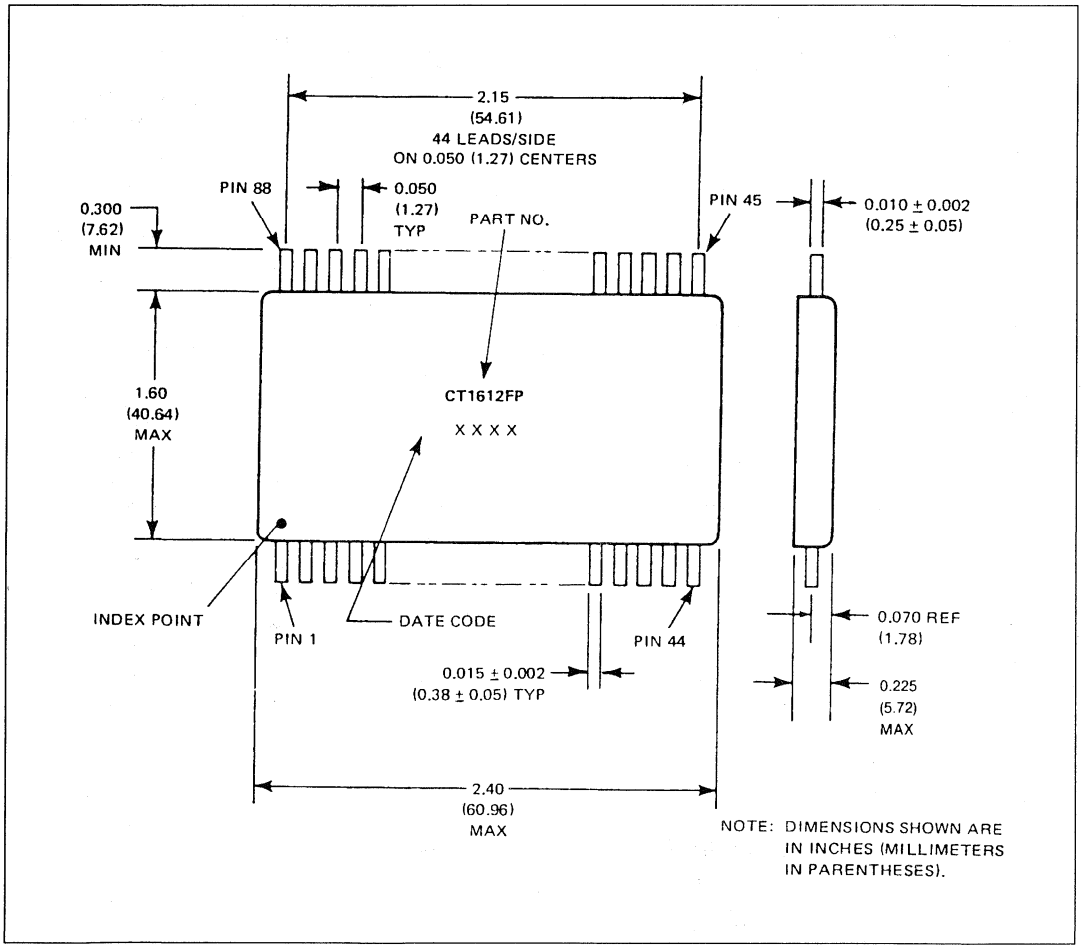


Figure 22: Flat Pack

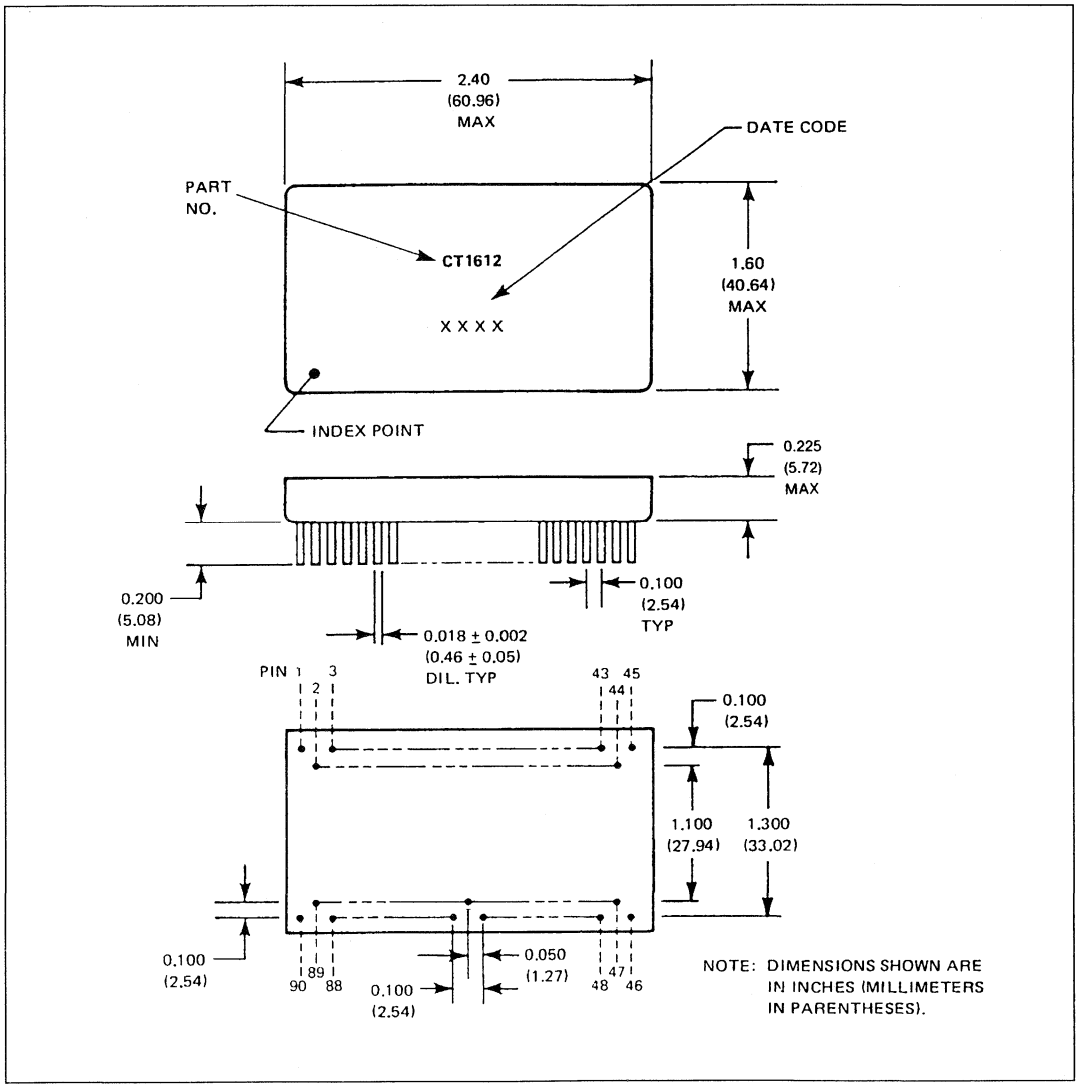


Figure 23: Plug-In

DS3064-1.1 July 1991

CT1990

MIL-STD-1553B REMOTE TERMINAL BUS CONTROLLER

(Supersedes H65 all versions)

The CT1990 device is a monolithic CMOS integrated circuit which performs the dual redundant MIL-STD-1553B bus controller remote terminal functions. This device is functionally compatible with the CT1612/MRTU53053 device, and is available as a form, and functional alternative to this unit.

By virtue of its monolithic nature, the CT1990 is available in a PIN GRID ARRAY (PGA) format and as a result provides further savings in space.

The CT1990 allows programming of the terminal flag, subsystem flag and message error status bits by the host subsystem.

The unit will connect directly with all existing GEC Plessy Semiconductor's single and dual transceivers and with the MCT1611 subsystem interface device.

Please contact the Sales Office for further information.

FEATURES

- Performs the complete dual-redundant remote terminal and bus controller protocol functions of MIL-STD-1553B
- Allows setting of the message error bit on illegal commands
- Provides programmable control over terminal flag and subsystem flag status bits
- Compatible with all GEC Plessey Semiconductor's driver/receiver units
- Small Size
- Available in Plug-In, Flatpack or PGA
- 5V DC Operation
- -55°C to +125°C Operation
- Digital or analogue loopback test capability (PGA only)

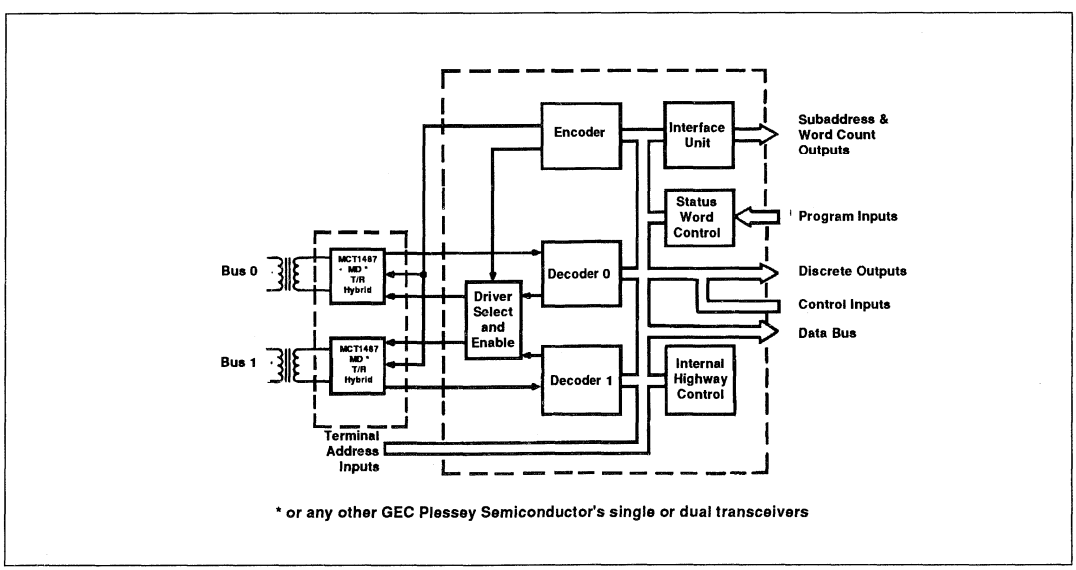


Figure 1: Functional Diagram

ADVANCE INFORMATION

3100-1.3 November 1991

CT2565

MIL-STD-1553 HYBRID BUS CONTROLLER REMOTE TERMINAL AND MONITOR

GENERAL DESCRIPTION

The CT2565 is a dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal (RT), and Bus Monitor, (BM) Bus packaged in a 1.9" x 2.1" hermetic hybrid. It provides the interface between a MIL-STD-1553 dual redundant serial data bus transceiver, (GPS's CT1487D for example). Utilizing GPS custom monolithic ICs, the CT2565 provides operation as a Bus Controller, Remote Terminal or a Bus Monitor (BM).

The CT2565 provides a 16 bit Tri-State parallel data bus and DMA handshaking for subsystem transfers. Message transfer timing (as well as DMA address and control lines) are provided internally. Interface control lines are common for both BC and RT operation.

The CT2565 implements all of the MIL-STD-1553 mode codes and any mode code may be defined as illegal by an externally selected ROM code.

Complete error detection capability is provided, for both BC and RT modes, including response time, timing gaps, sync, parity, Manchester, word count and bit count. Additionally, in the BC mode, the status word is checked for proper address and the setting of the bit flags.

The hybrid is screened in accordance with the requirements of MIL-STD-883 and operates over the full military temperature range of -55°C to +125°C.

FEATURES

- Second source compatible to the BUS-65600
- Dual redundant
- Selectable BC or RT operation
- 1.9" x 2.1" hybrid package
- 16 bit microprocessor compatibility. DMA subsystem message transfers.
- Status word check for valid address and presence of bit flags
- RTU illegal mode codes externally selectable
- BC and RT error detection for response time, timing gaps, sync parity, manchester, word count and bit count
- Continuous built-in-test

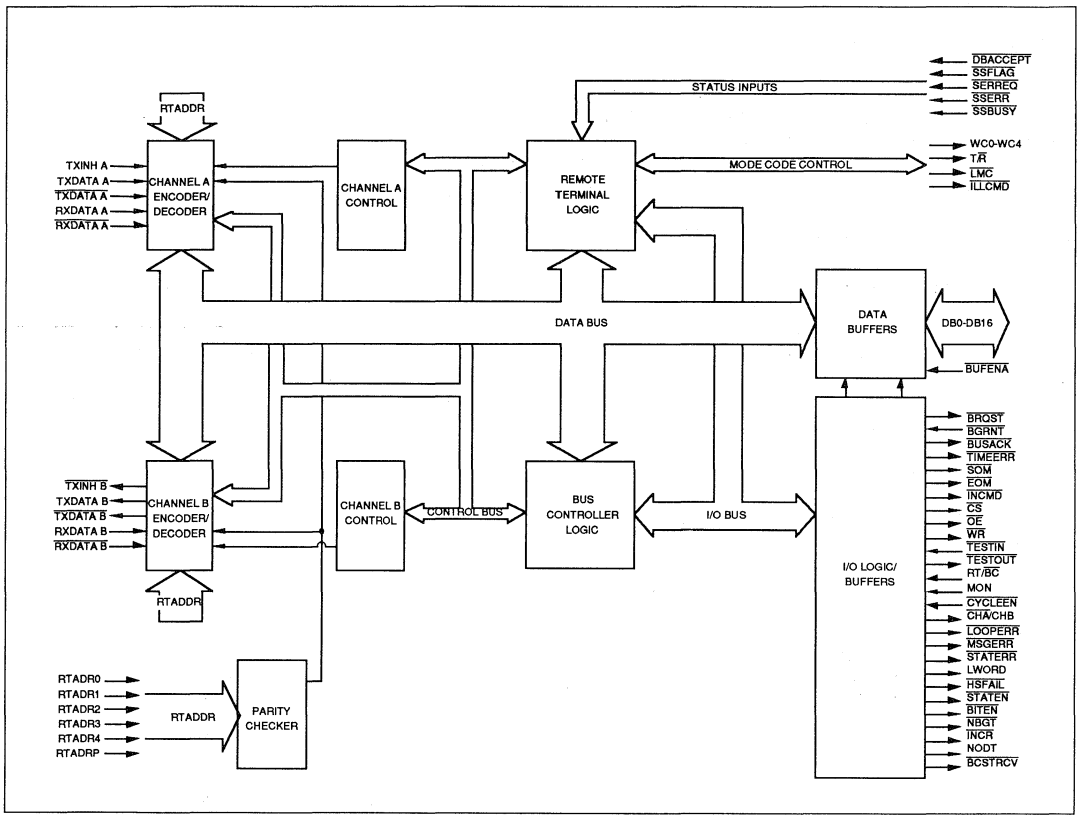


Figure 1: Block Diagram

PIN FUNCTION TABLE

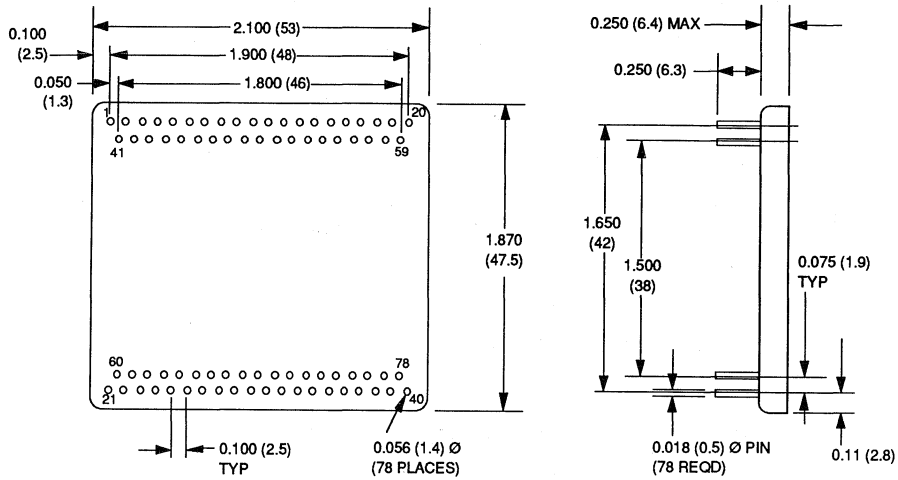
Pin No	Symbol	Description
1	RT/$\overline{BC}$	Mode Select input - logic "1" for RT mode, logic "0" for BC mode.
2	MON	Monitor mode enable. When unit is operating as a BC, a logic "1" will select monitor mode.
3	$\overline{STATEN}$	Output signal in RT mode that indicates status word is being transferred on the internal bus.
4	$\overline{TIMEERR}$	Output signal indicating a no-response timeout has occurred during BC operation or during a RT to RT transfer in the RT mode.
5	$\overline{HSFAIL}$	Output in RT mode indicating the DMA transfer did not occur in time to allow proper operation on the 1553 bus.
6	$\overline{DBACCEPT}$	Input signal used to set DBACCEPT bit in status reglster for response to a valid mode command on the 1553 bus.
7	$\overline{SSFLAG}$	Input which controls the SSFLAG bit in the status register.
8	$\overline{SEREQ}$	Input which controls the service request bit in the status word.
9	$\overline{INCMD}$	Output signal indicating the RT is currently in a message transfer sequence.
10	$\overline{SSER}$	Input which controls the subsystem error bit in the status register.
11	$\overline{TESTOUT}$	Output used to test the failsafe timer during factorv testlng.
12	WC1	WC bit 1 - latchedooutput of command word.
13	WC3	WC bit 3 - latched output of command word.
14	TXINHB	Transmitter inhibit output for channel B.
15	T/$\overline{R}$	Output indicatingT/$\overline{R}$ bit of current command word in RT mode.
16	$\overline{CHA}$/CHB	Output indicating current selected channel (0 = Channel A).
17	$\overline{CS}$	Chip Select output for subsystem memory control.
18	$\overline{OE}$	Output Enable output for subsystem memory control.
19	$\overline{DTREQ}$	Output signal used to initiate transfer to/from subsystem.
20	+5V	+5 Volt DC input.
21	DB0	Least significant bit - 16 bit parallel data bus.
22	DB2	Bit 2 of data bus.
23	DB4	Bit 4 of data bus.
24	DB6	Bit 6 of data bus.
25	DB8	Bit 8 of data bus.
26	GB10	Bit 10 of data bus.

Pin No	Symbol	Description
27	DB12	Bit 12 of data bus.
28	DB14	Bit 14 of data bus.
29	LWORD	Lastword output during BC mode indicates last data word of the current message transfer has been transferred on the parallel bus.
30	$\overline{\text{MSGERR}}$	Output signal which indicates an error occurred during the current message sequence.
31	TXDATA A	Bipolar serial data output to positive inputoof bus transcelver.
32	$\overline{\text{RXDATA A}}$	Bipolar serial input Rom negative output of bus transceiver.
33	RTADP	Parity bit input for RT address.
34	RTAD1	Bit 1 of RT address input.
35	RTAD3	Bit 3 of RT address input.
36	$\overline{\text{RESET}}$	System reset input - resets all inputs in module.
37	$\overline{\text{TXDATA B}}$	Bipolar serial data output to negative input bus transceiver.
38	RXDATA B	Bipolar serial data input Rom positive output of bus transceiver.
39	12MHz	12MHz TTL clock input.
40	GROUND	Signal ground.
41	$\overline{\text{CYCLEEN}}$	Cycle enable input Logic "0" initiates bus controller message transfer operation.
42	$\overline{\text{NBGT}}$	New bus grant outputfrom RT indicates beginning of message transfer sequence.
43	$\overline{\text{BITEN}}$	Built In Test enable output indicates RT is transferring BIT word on internal 16 bit bus.
44	$\overline{\text{WR}}$	Write enable output for control of subsystem memory.
45	$\overline{\text{DTGRNT}}$	Bus request input in response to $\overline{\text{DTREQ}}$. Allows BC/RT to transfer data to subsystem.
46	$\overline{\text{LOOPERR}}$	Loop error output. Logic "0" indicates failure of loop back transmitted data.
47	$\overline{\text{SSBUSY}}$	Subsystem busy input for RT status word.
48	$\overline{\text{ILLCMD}}$	Illegal command input to RT, used to block RT response to an illegal command.
49	$\overline{\text{INCR}}$	Increment output pulse. Goes LOW at the completion of each word transfer to/from subsystem. Can increment external address counter.
50	FRAME	Frame ground-electrically isolated from signal ground.
51	WC0	LSB of current command word count field.
52	WC2	Bit 2 of word count field.

Pin No	Symbol	Description
53	WC4	Bit 4 of word count field.
54	TXINHA	Transmitter inhibit output signal for Channel A.
55	$\overline{\text{LMC}}$	Latched ModeCommand. Logic "0" indicates current word command is a mode code word, WC0-WC4.
56	$\overline{\text{TESTIN}}$	Factory test input-enable fail safe counter for selected channel.
57	$\overline{\text{EOM}}$	End of message output. Logic "0" occurs when BC/RT message is completed.
58	$\overline{\text{BUFENA}}$	Buffer enable input, may be driven LOW by $\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ if subsystem must read bit or Status words. Enables internal 16 bit bus onto subsystem bus.
59	$\overline{\text{DTACK}}$	Bus acknowledge output. LOW during DMA Handshake, in response to $\overline{\text{DTRGRNT}}$.
60	DB1	Bit 1 of 16 bit parallel bus.
61	DB3	Bit 3 of 16 bit parallel bus.
62	DB5	Bit 5 of 16 bit parallel bus.
63	DB7	Bit 7 of 16 bit parallel bus.
64	DB9	Bit 9 of 16 bit parallel bus.
65	DB11	Bit 11 of 16 bit parallel bus.
66	DB13	Bit 13 of 16 bit parallel bus.
67	DB15	Bit 15 of 16 bit parallel bus.
68	$\overline{\text{STATERR}}$	BC output indicates one or more bits set or address mismatch in a received status word.
69	$\overline{\text{TXDATA A}}$	Bipolar serial data output to negative input of bus transcelver.
70	RXDATA A	Bipolar serial data input from positive output of bus transceiver.
71	NODT	Nodata input. Logic "1" indicatesthe 1553 bus is idle; LOW means device front end is active.
72	RTADO	LSB of 5 bit RT address.
73	RTAD2	Bit 2 of RT address.
74	RTAD4	Bit 4 of RT address.
75	$\overline{\text{BCSTRCV}}$	Broadcast receive O/P means the current command was a broadcast command.
76	TXDATA B	Bipolar serial output to positive input of bus transceiver.
77	$\overline{\text{RXDATA B}}$	Bipolar serial input from negative output of bus transceiver.
78	$\overline{\text{SOM}}$	Start of message output indicates beginning of RT/BC message transfer sequence.

NOTE: All input connections represent 1 LS TTL load.
All output connections are CMOS and will drive 2 LS TTL loads.

PACKAGE OUTLINE



Dimensions in Inches (Millimetres)

AN3192-1.2 December 1991

MA805

FUNCTION AND TIMING INFORMATION

INTRODUCTION

Scope

This guide is intended to supplement the MA805 Data Sheet (DS3043-1) and explains only the standard 1553B functions.

Section 1	Describes INITIALISATION of the MA805 and the two modes of RESET HARD and SOFT.
Section 2	Describes the sequences that govern the transfer of data to and from the SUBSYSTEM; the concept of the STATUS MODIFIER word; the significance of GTB and the treatment of ERRORS. Timing diagrams for all control signals are provided.
Section 3	Details the set up and hold times required for all HIGHWAY words to and from the SUBSYSTEM.
Section 4	Gives the RESPONSE time of the MA805.
Section 5	Explains the effect of overriding commands and its effect on the handshake control signals. Also explains handshake operation.
Section 6	Explains access to MA805 registers.
Section 7	Describes the MA805's ability to read the BIT word from the SUBSYSTEM (EXTERNAL) and the interaction of other mode codes.
APPENDIX A	Provides a useful reference to 1553B formats and mode codes.
APPENDIX B	Example of Memory Map for the MA805.

PRINCIPLES OF OPERATION

The MA805 RT is INITIALISED under SUBSYSTEM control by reading the INITWORD from the HIGHWAY (H0: H15). The RT address is contained in the INITWORD and is continually checked during operation for ODD parity. If this should ever be corrupted the MA805 will be forced into a RESET condition and wait for the SUBSYSTEM to provide the INITWORD. This is normally a 16 bit word but can be reduced if not all functions are required. It is also possible for the SUBSYSTEM to clear internal flags and registers without providing the INITWORD (SOFT-RESET).

All valid words are transferred to the SUBSYSTEM over a 16 BIT 3 STATE HIGHWAY (H0:H15), under SUBSYSTEM control using a hard wired HANDSHAKE protocol. All transfer sequences start with a control word (CONTWORD). This CONTWORD can be used to MAP the data to user memory.

All transfers are governed by fixed sequences which are under MA805 control. These are referred to as COMMAND OUT DATAOUT, DATAIN. This time structured control avoids the possibility of the SUBSYSTEM contravening 1553B protocol. During the COMMAND OUT sequence, the COMMAND word is tranferred to the SUBSYSTEM and the SUBSYSTEM must then provide a STATMOD word. This gives the SUBSYSTEM control over the ALLOWING of RESERVED mode codes or the setting of any bits in the STATUS word, e.g. ME. DATAOUT and DATAIN sequences control the transfer of DATAWORDS to and from the SUBSYSTEM.

Completion of ERROR free transfers between the terminal and subsystem are indicated by the pulsing of a dedicated pin (GTB). This signal is synchronised with the termination of HREQB.

The SUBSYSTEM has access to the internal registers: INITWORD, STATUS, BITWORD and LAST COMMAND, upon demand or automatically after every VALID command. This can provide valuable diagnostic information. This function is controlled by a dedicated pin (IRWB). For this register transfer GTB is not applicable and is therefore not pulsed.

The SUBSYSTEM can select the source of the BIT word to be from the SUBSYSTEM itself instead of from the MA805 internal register. This selection is made during INITIALISATION. Its function could be to interchange bit positions within the BIT word for system compatability with other vendors.

Finally, OWN transmissions from the MA805 to the 1553B bus are checked by a LOOPTEST, and transmissions greater than 33 words are terminated by operation of a timeout counter.

Throughout this document the convention used in naming signals is to use a B suffix to indicate active low signal, e.g. HACKB = Highway ACKnowledge. The absence of the suffix indicates an active high signal.

1. INITIALISATION + RESET

1. Power on Reset.
2. Mode Code Reset.
3. Subsystem Initiated Reset.
   (i) HARD (+ INITWORD)
   (ii) SOFT (NO INITWORD)

1.1 POWER ON RESET

Ref. FIG 1.1
Outputs HREQB
RESETB
Inputs HACKB
HO:H15 (INITWORD)
CK: CLOCK

Operation:
The MA805 powers up with HREQB=0 and RESETB = 0. The internal POR period T-POR must then elapse. The MA805 then reads the INITWORD once only after the SUBSYSTEM has driven HACKB = 0. The INITWORD is then checked for ODD parity in the RT ADDRESS field (ADDO: ADD4, PARITY). If this is not true then the cycle repeats after Time T-INIT (refer to table 1) has elapsed, (without the POR period T-POR), i.e., HREQB and RESETB are SET=0 by the MA805. The terminal is available to the Bus Controller only after time T-INIT has elapsed. The address is continually monitored for ODD parity. SOFT reset is NOT available at power up.

N.B. There is no timeout on the handshake for this sequence. The user is only limited by 1553B protocol that requires the RESET to be completed within 5mS.

1.2 MODE CODE RESET

Ref. FIG 1.2
Outputs HREQB
RESETB
Inputs HACKB
H0:H15 (INITWORD)

Operation:
Normal COMMAND servicing is first completed as indicated by GTB = O.

The RESET sequence is then started as for power up reset except the internal POR timer is not used.

TA = -55°C to 125°C VDD = 5V+10%, CL = 50pf and ITTL load.

Symbol	Definition	Limits			Units
		Min	Typ	Max	
T-POR	Power on Reset	40		100	us
T-RESET	Reset Cycle		1.2	1.5	us
T-INIT	805 held in initialised State		7.5	8.0	us
T-VAL	Initword valid on highway		1.2	1.5	ns
T-HK-VAL	Delay from HACKB to supplying valid initword	0		500	ns
T-RES-HRH	Delay from RESETB going inactive to HREQB going inactive			150	ns
T-RES-HRL	Delay from RESETB going active to H R EQB going active			150	ns
T-LATCH	Overlap to ensure 805 latches RESETB = 0	500			ns
T-HR-GT (Reset)	HREQB to GTB		24		us
T-GT-HR	GTB to HREQB		500		ns
T-HR	HREQB pulse width following MODE CODE Reset		500		ns

Table 1: AC Electrical Characteristics

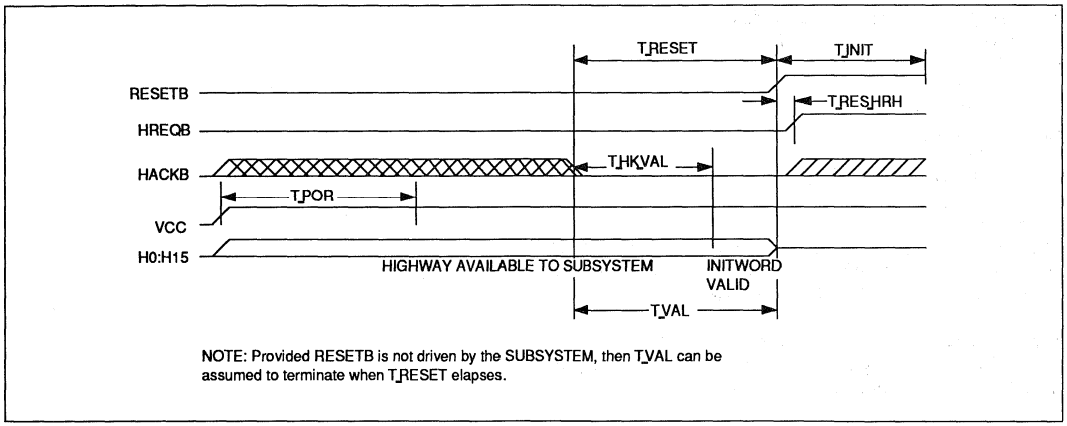


Figure 1.1: Power on Reset

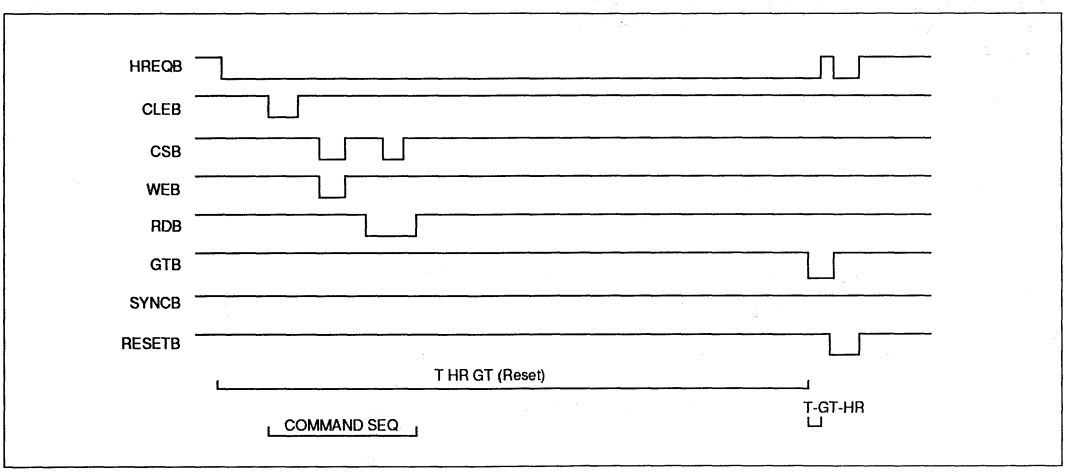


Figure 1.2a: Reset

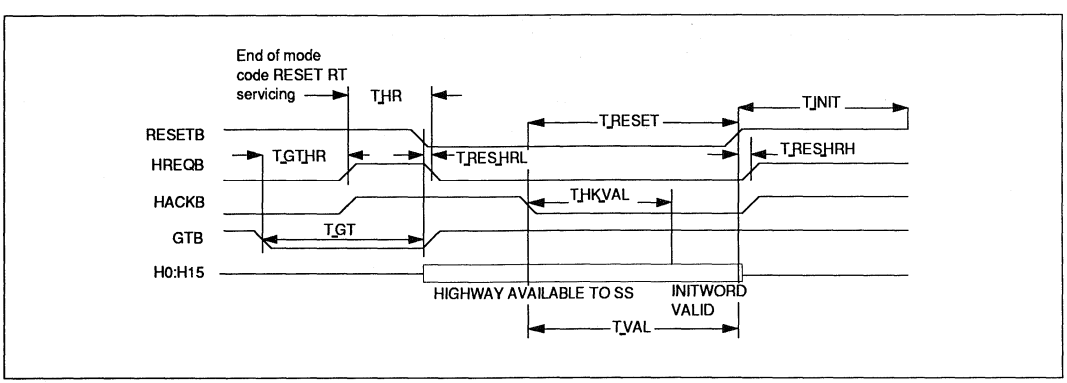


Figure 1.2b: Mode Code Reset (after Mode Code Reset RT servicing)

1.3 SUBSYSTEM INITIATED RESET

(i) With INIT Word (HARD RESET)
Ref. FIG 1.3
Outputs HREQB
RESETB
Inputs HACKB
RESETB
H0:H15 (INITWORD)

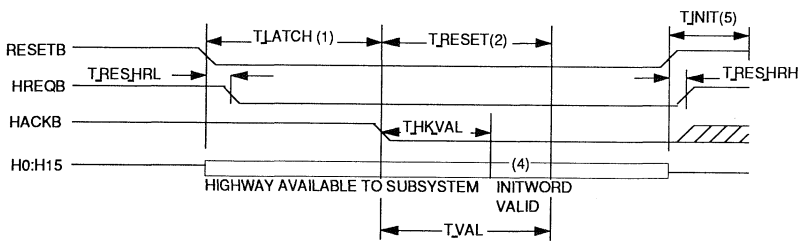
Operation:
At any time the SUBSYSTEM is able to force the MA805 RT into the RESET state by driving RESETB=0. The MA805 remains in this state until the SUBSYSTEM drives HACKB=0.

The MA805 will then latch the RESETB signal and itself drive RESETB =0 for a further time T-RESET. The MA805 will then read the INITWORD from the HIGHWAY (H0:H15).

HACKB must remain Set=0 until time T-RESET has elapsed.

(ii) Without INIT Word (SOFT RESET) The SUBSYSTEM is able to clear the internal registers (except INITWORD) and flags (e.g., TF, ME) by pulsing RESETB, minimum pulse width = 100ns, and driving HACKB=1.

The SUBSYSTEM does not set HACKB.



Notes:
1. RESETB driven by SUBSYSTEM
2. RESETB driven by MA805 (latched)
3. RESETB shown extended, driven by SUBSYSTEM only
4. The INITWORD is loaded into the MA805. This *occurs once only* during T_RESET
5. The MA805 is still off-line during this period when T INIT has elapsed the address is checked for 000 parity and the terminal is again available to the Bus Controller.

Figure 1.3: Subsystem Initiated Reset

SUBSYSTEM INTERFACE

2. SUBSYSTEM TRANSFERS

The 1553 bus messages are of the form shown in Appendix A. Figures 2.1 to 2.12 show examples of the subsystem waveforms in response to these messages and assume that HREQB and HACKB provide a normal handshake.

There is a direct relationship between the command word and data words of the 1553 bus message and subsystem sequences. The command word of the 1553 message causes the subsystem Command sequence (Figure 2.1). Data words of a Receive message give subsystem "Data Out" sequences (Figure 2.2). Data words of a transmit message cause subsystem "Data In" sequences (Figure 2.3).

Various errors (e.g Manchester encoding errors, handshake failure) cause the subsystem sequences to terminate immediately.

The format for the 1553 bus words are shown in Appendix A.

NB. The terminal will ignore messages that have any error in the command word.

Note that for transmit last status, and transmit last command mode codes there is no communication at all with the subsystem.

Subsystem Command Sequence (Figure 2.1)

The command sequence has three parts:
1) Control Word
2) Command Word
3) Status Modifier

1) The control word provides essential information about the message and is timed by CLEB. CLEB can be used to load external control latches with the control word. (See data sheet for the interpretation of individual bits). The latched word can then be used to control the addressing for the command sequence, or processing of the message by decoding the top 5 BITS of the control word.

2) The command word is then sent (CSB with WEB). This word is made available for the subsystem user to be able to take particular action for different commands if required.

3) The status modifier is requested from the subsystem. This adds flexibility and permits the subsystem to influence the status response of the remote terminal. The detail for each bit is given in the data sheet.

Note that SETMEB and SETBUSYB both shorten the message by preventing data transfers. When ALLOWB is inactive (i.e. the mode code is not being recognised by the MA805 or its subsystem) the associated data word transfer for reserved mode codes with data are also prevented.

Subsystem Data In Sequence (Figure 2.3)

The "Data In" sequence obtains data from the subsystem for transmission and has two parts:

1) Control Word
2) Data

The sequence is repeated for each data word transferred.

The control word is timed by the CLEB pulse. The control word contains the subaddress and Data word count information. The data word count field has an incrementing value from zero up to the number of words to be transferred less one. The control word is latched by the subsystem and the subaddress field concatenated with the incrementing word count provide 10 BIT memory addressing.

The data word is timed by CSB and RDB pulses.

Subsystem Data Out Sequence (Figure 2.2)

The "Data Out" sequence passes data from a received command to the subsystem and has two parts:

1) Control Word
2) Data

The sequence is repeated for each data word transferred.

The control word is timed by the CLEB pulse. The control word contains the subaddress and Data word count information. The data word count field has an incrementing value from zero up to the number of words to be transferred less one. The control word is latched by the subsystem and the subaddress concatenated with the incrementing word count field provide 10 BIT memory addressing.

The data word is timed by CSB and WEB pulses.

Good Transaction

At the end of a message a signal GTB is pulsed low if the transfers to or from the subsystem have been completed without error.

The timing of GTB is such that the rising edge of HREQB can be used to strobe GTB into a latch. The latched GTB signal can then be used to initiate further subsystem activity as required.

GTB will be absent for the following reasons:

a) Failed word or message validation (including reserve mode codeswwithout ALLOWB).
b) SETMEB or SETBUSYB BIT set in subsystem status modifier word.
c) Failed subsystem handshake.
d) Overriding commands terminating a previous command prematurely.

Memory Mapping

The subaddress field (5 BITS) contained in the command word is forwarded as part of the control word for data transfers to the subsystem. This subaddress field can be used to select a 32 word block of memory. The word count field of the control word (5 BITS) is used to select an address within the 32 word block (Figure 2.0).

If the read signal is also used as part of the address (giving a total of 11 BITS) all data transfers will have their own specific area of memory.

The data transfers associated with mode codes also have special addresses.

A subaddress field of 00 or 1F indicates a mode code. For mode codes with data, the subaddress field in the control word for the data transfer is always made 1F (HEX). The word count field for the data transfer contains the mode code number. Mode codes with data are in the the range of 10-1F (HEX) (see assigned Mode Code List - Appendix A).

All messages can therefore be mapped into memory.
(See Appendix B)

TIMING DIAGRAMS

The possible 1553B messages and their corresponding subsystem sequences are summarised below:

RECEIVE COMMAND
(INCLUDING BROADCAST) (Figure 2.4)
(a) Command Sequence
(b) Data Out (repeated)

TRANSMIT COMMAND (Figure 2.5)
(a) Command Sequence
(b) Data In (repeated)

RECEIVE COMMAND RT-RT
(INCLUDING BROADCAST) (Figure 2.6)
(a) Command Sequence
(b) Data Out (repeated)

TRANSMIT COMMAND RT-RT (Figure 2.7)
(a) Command Sequence
(b) Data In (repeated)

TRANSMIT MODE CODE (NO DATA) (Figure 2.8)
(a) Command Sequence
(b) RESET See Section 1

TRANSMIT MODE CODE+DATA (Figure 2.9)
(a) Command Sequence
(b) Data In

TRANSMIT INTERNAL BIT WORD (Figure 2.10)
(a) Command Sequence

RECEIVE MODE CODE + DATA (Figure 2.11)
(a) Command Sequence
(b) Data Out Sequence

RESET MODE CODE (Figure 2.12)
(a) Command Sequence
(b) Reset (See Section 1.2)

Timings

The timing signal names are derived from shortened mnemonics of the full signal name. Additionally R(receive), T(transmit), RT(RT-RT transfers), COM(command sequence), DI(Data In sequence) DO(Data Out sequence) are used.

Timings between active low pulses are from leading edge to leading edge.

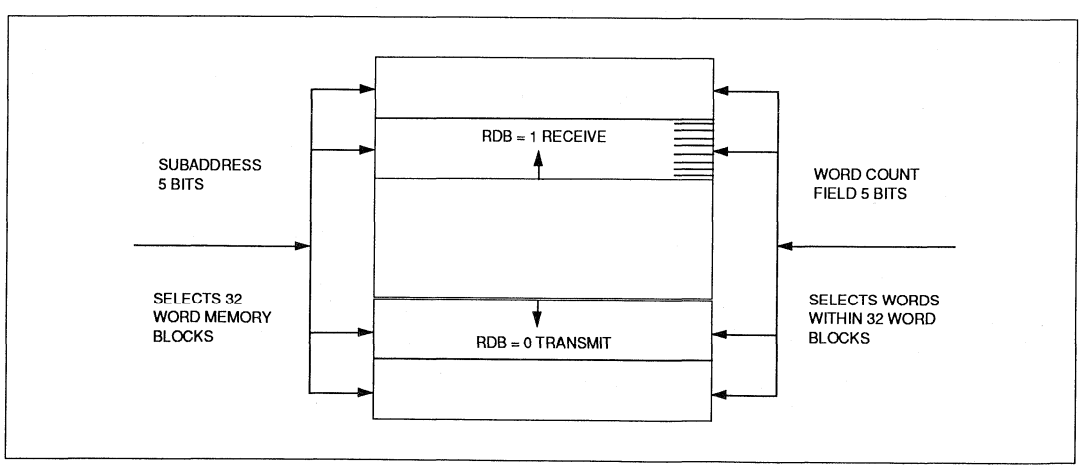


Figure 2.0

TA = - 55°C to 125°C, VDD = +10%, CL = 50pf and ITTL load.

	Symbol	Definition	Time	Units
			T Typical	
PULSE WIDTHS	T-CL	Width CLEB	1	us
	T-CS	Width CSB	1	us
	T-GT	Width GTB	1	us
	T-RD	Width RDB	2	us
	T-SYNC	Width SYNCB	1	us
	T-WE	Width WEB	1	us
	T- RESET	Width RESETB	1.2	us
COMMAND SEQUENCE	T-HR-CL	HREQB to CLEB in Command Sequence	2	us
	T-CL-CS	CLEB to CSB in Command Sequence	2	us
	T-CS-CS	CSB to CSB in Command Sequence	2.5	us
	T-CS-RD	CSB to RDB in Command Sequence	2	us
COMMAND SEQUENCE TO DATA TRANSFER	T-R-COM-DO	Receive: Command CLEB to Data Out CLEB	19*	us
	T-T-COM-DI	Transmit: Command CLEB to Data In CLEB	18*	us
	T-R-RT-COM-DO	Receive: Command to Data Out CLEB for RT- RT transfer	61.5*	us
	T-T-RT-COM-DO	Transmit: Command CLEB to Data In CLEB for RT- RT transfer	18*	us
DATA OUT SEQUENCE	T- R - DO- DO	CLEB to CLEB Data Sequence	20*	us
	T-R-CL-CS	CLEB to CSB in Data Sequence	2	us
	T- R - CS - GT	CSB to GTB for Last Data Out Sequence	3	us
DATA IN SEQUENCE	T-T-DI-DI	CLEB to CLEB in Sequence	20*	us
	T-T-CL-CS	CLEB to CSB in Data In Sequence	2.5	us
	T-RD-CS	RDB to CSB in Data In Sequence	0.5	us
	T-T-CS-GT	CSB to GTB for Last Data In Sequence	3	us
GOOD TRANSACTION	T-GT-HR	GTB TO HREQB at end of sequence	0.5	us

The above times may have a spread of ±20ns.

* These timings are affected by the 1553 bus timing of words.

Table 2: AC Electrical Characteristics

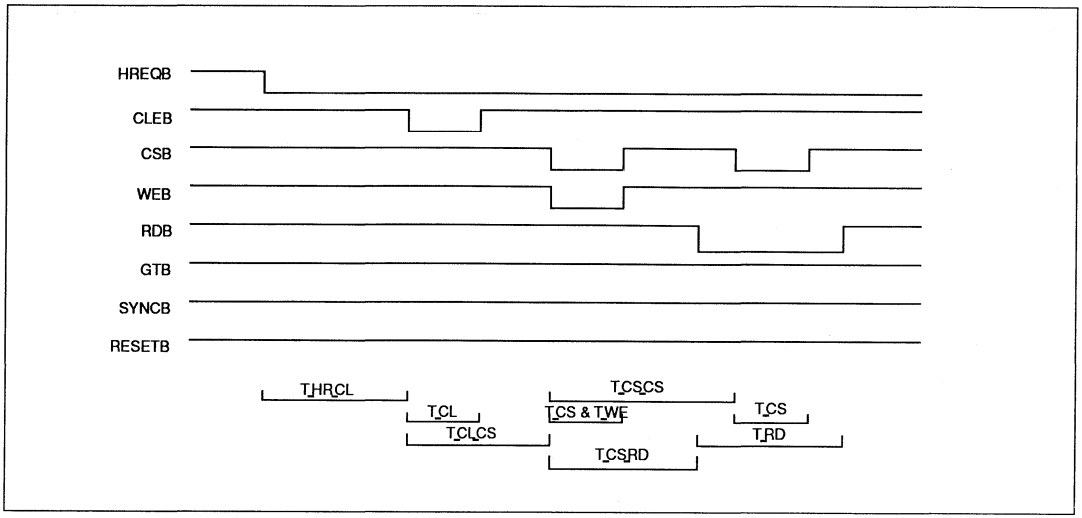


Figure 2.1: Command

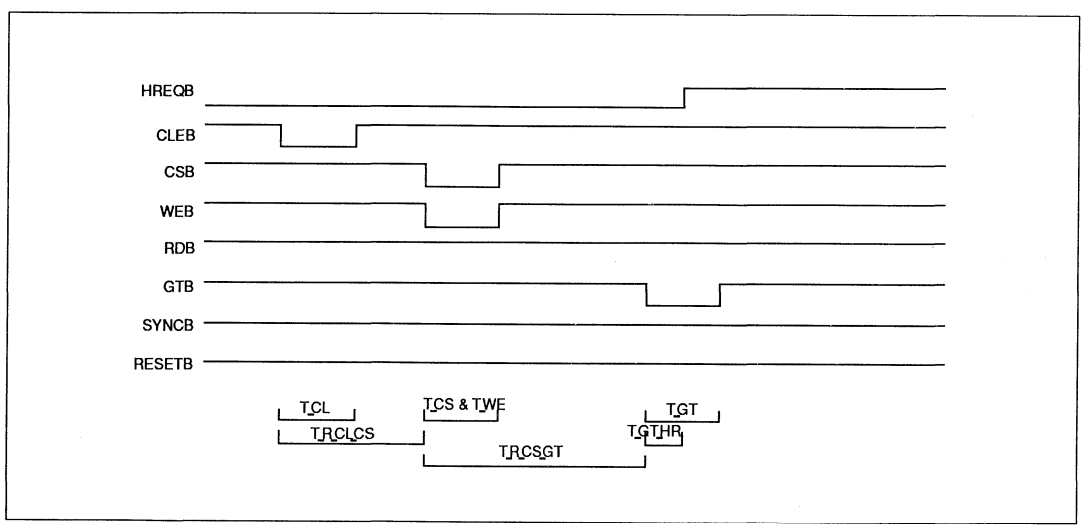


Figure 2.2: Data Out

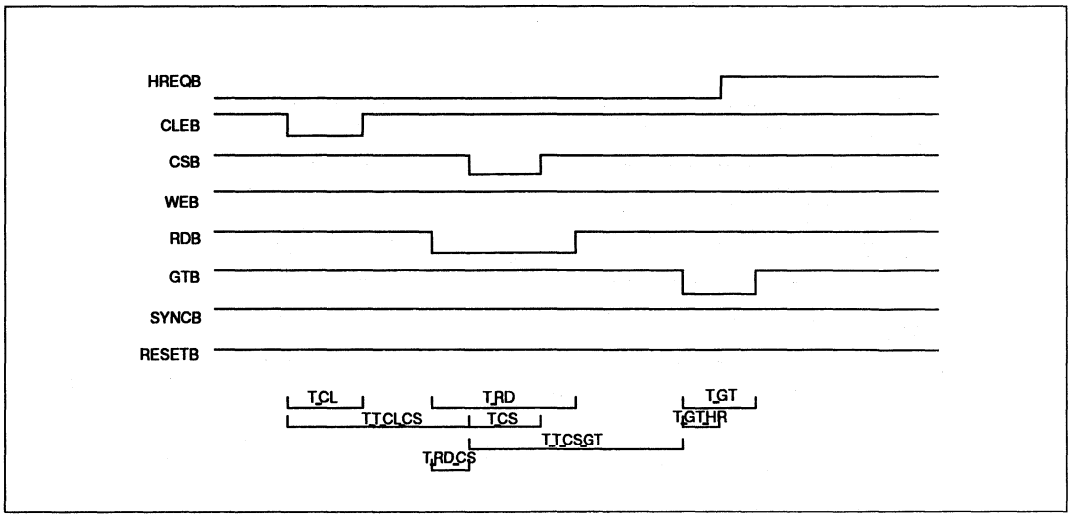


Figure 2.3: Data In

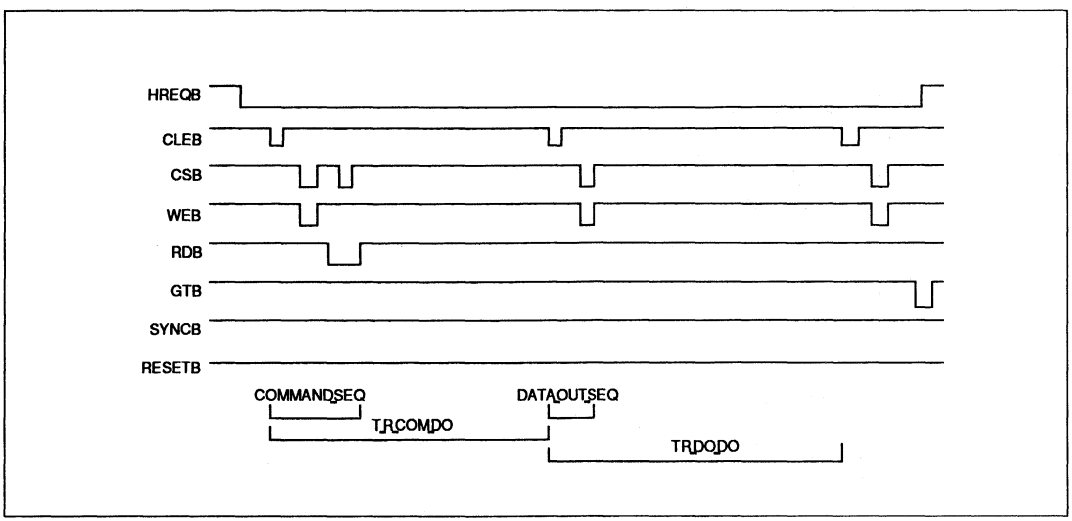


Figure 2.4: Receive Commands (including Broadcast)

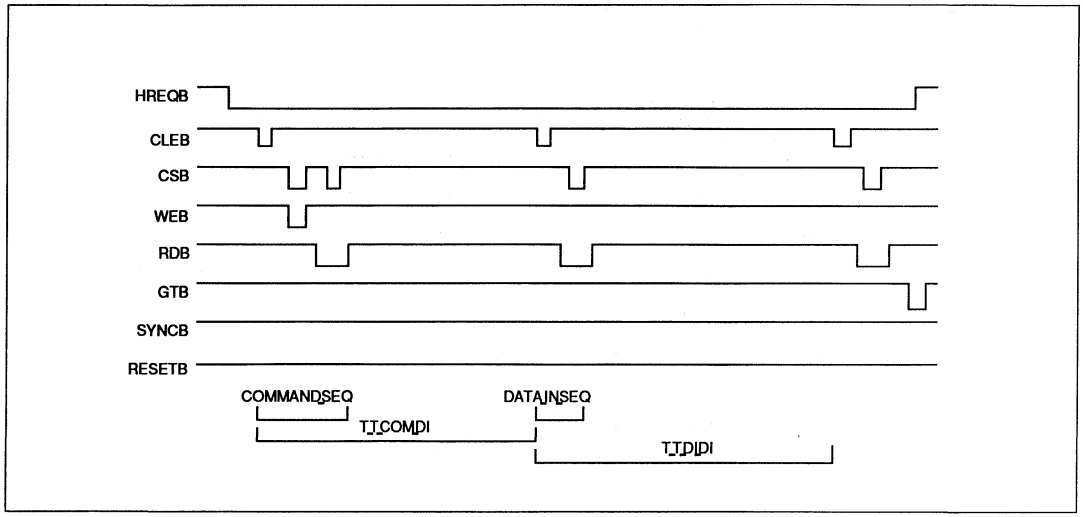


Figure 2.5: Transmit Commands

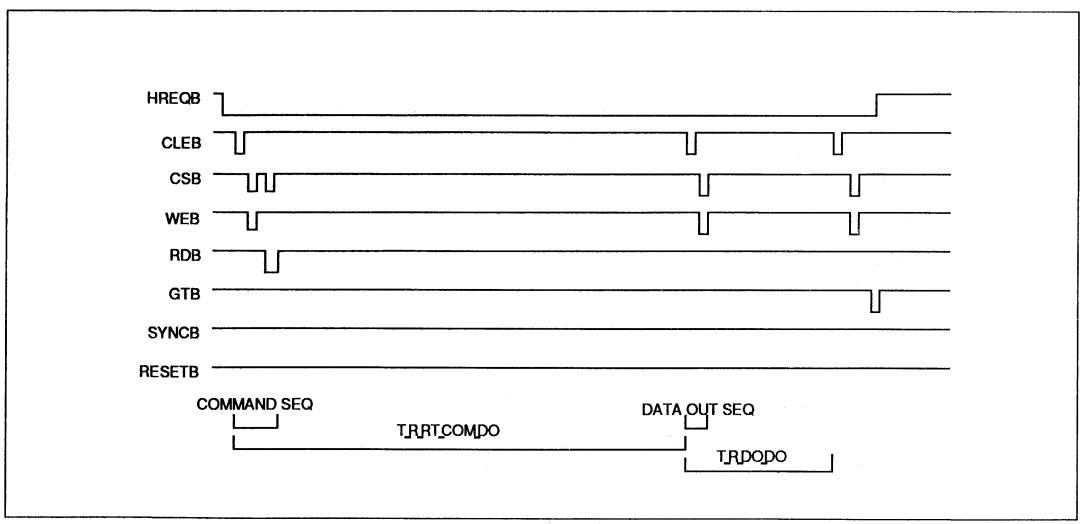


Figure 2.6: Receive Command RT-RT

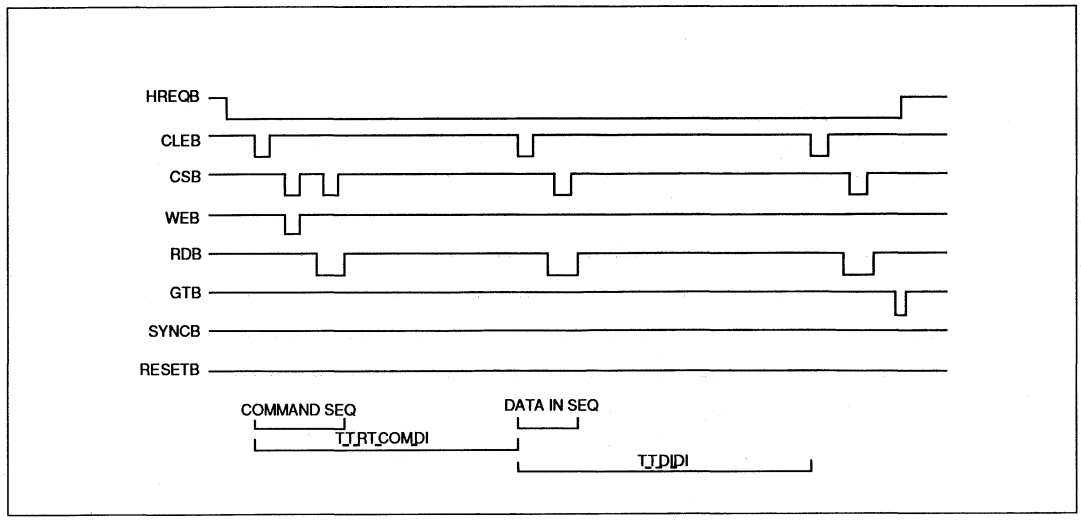


Figure 2.7: Transmit Command RT-RT

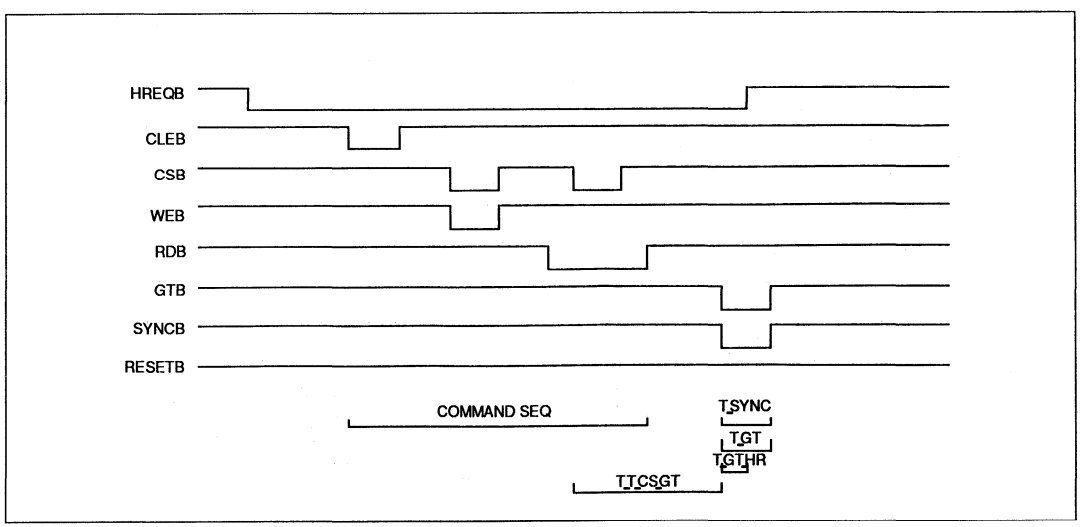


Figure 2.8: Transmit Mode (No Data)

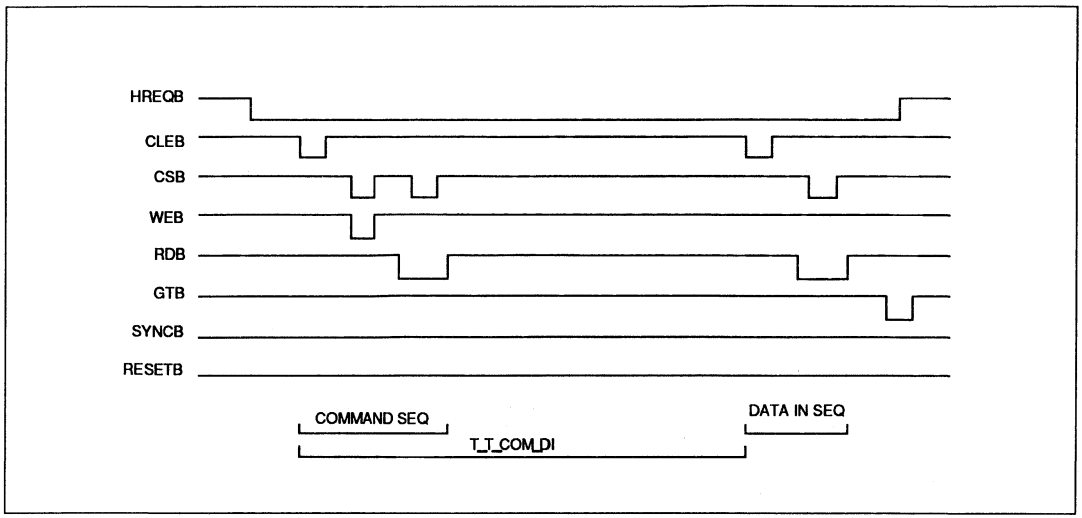


Figure 2.9: Transmit Mode Code + Data

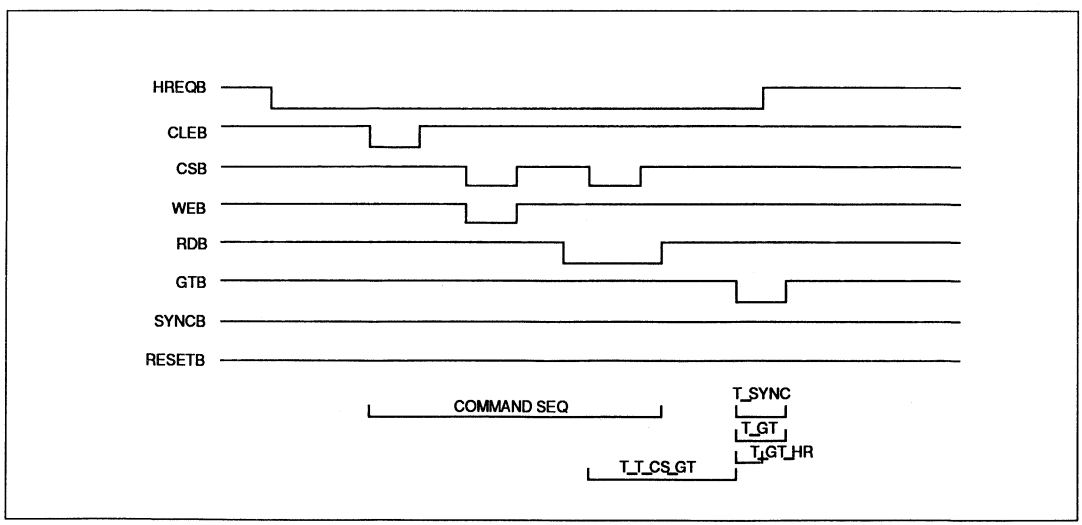


Figure 2.10: Transmit Internal Bit Word

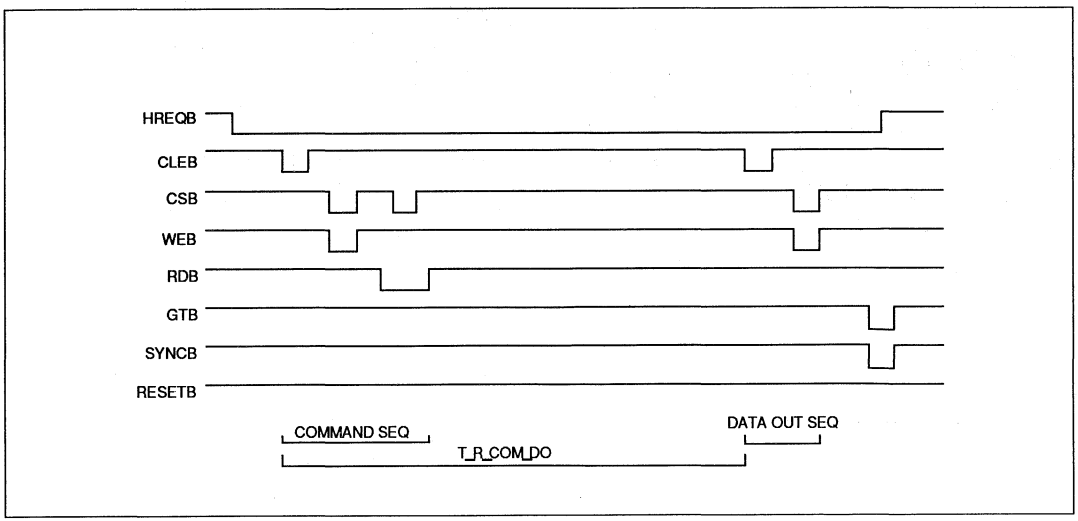


Figure 2.11: Receive Mode Code + Data

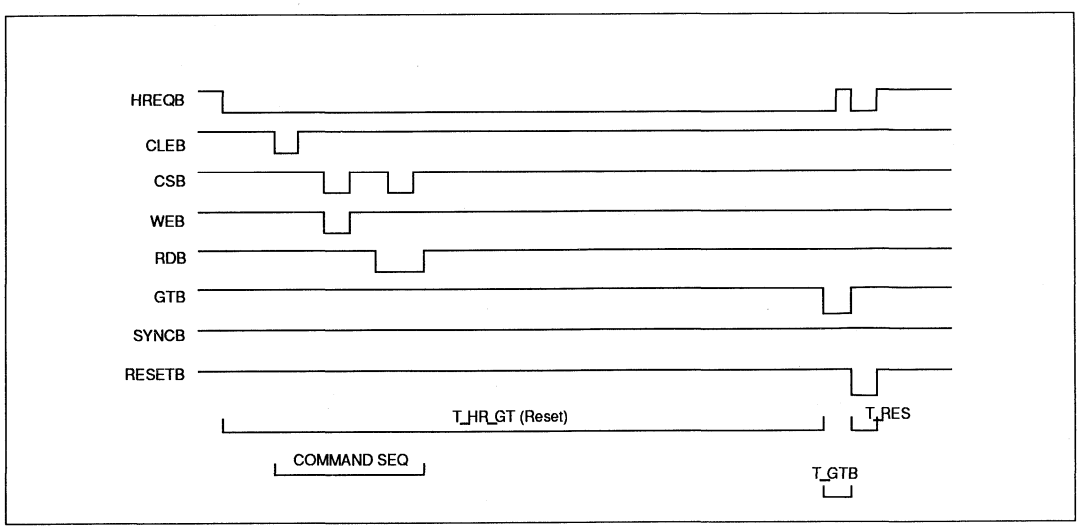


Figure 2.12: Reset

3. HIGHWAY TIMINGS

TA = -55°C to 125°C, VDD = ±10%, CL = 50pf and ITTL load.

Symbol	Definition	Limits			Units
		Min	Typ	Max	
WRITE CYCLE					
T-DRIV	Highway driven from H1Z			500	ns
THW-VAL	Highway data valid		200		ns
THW-HOLD	Highway hold time	500			ns
T- H1Z	Highway to H1Z from driven			na	ns
READ CYCLE					
THR - SET	Highway set up time	500			ns
THR-HOLD	Highway hold time	0			ns

Table 3.1: Electrical Characteristics

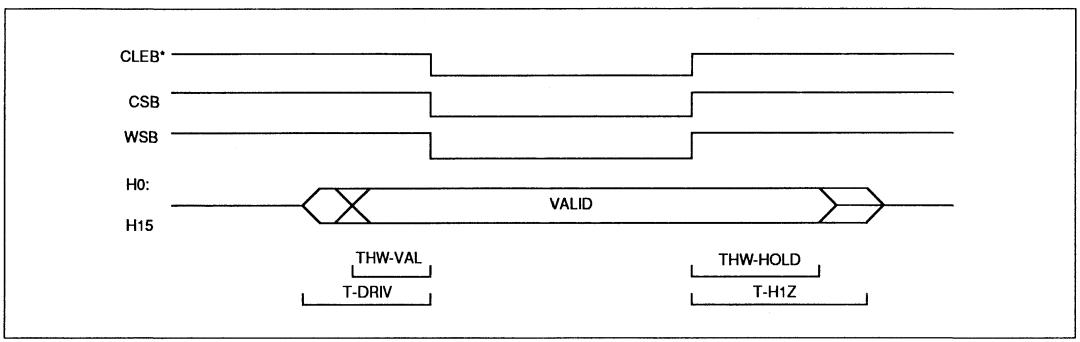


Figure 3.1: Write Cycle

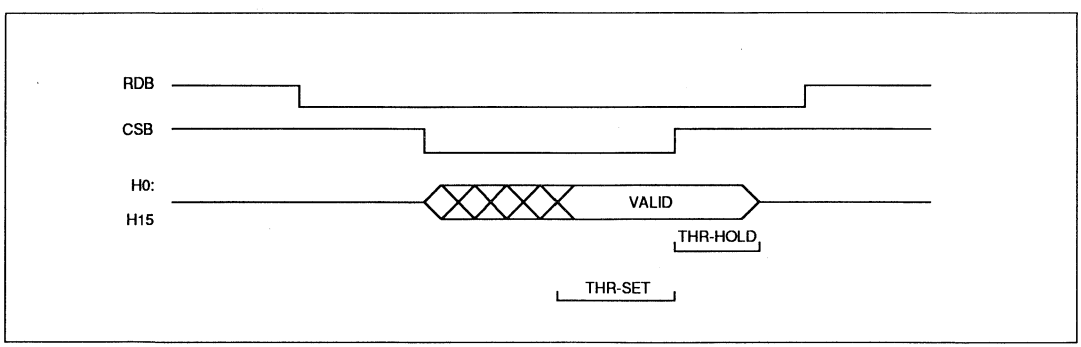


Figure 3.2: Read Cycle

4. RESPONSE TIME

The typical response time of the MA805 chip to messages is between 10 and 10.5µsecs. The measurement is from the mid-point of the parity bit of the last word of the command message (RXDATAO Pin of MA805) and the mid-point of the status response (TXDATAO Pin of MA805).

Delayed Status

An option DELSTATB is provided in the initialisation word. When this Bit is active low the response from the MA805 is delayed by an extra 31.5µsecs. This is for use with those subsystems which need extra time before data can be provided. If RT-RT transfers are to be used as well then the TM1B, TMOB Bits of the initialisation word should be selected accordingly (See Note 3 of the INITWORD section of the Data Sheet).

5. OVERRIDING COMMAND

A command is said to be overriding when a valid command on one bus is terminated before completion, due to reception of a valid command on the other bus. The subsystem signals for the interrupt message are turned off immediately. The second message is then processed. HREQB switches off between the messages with a minimum off period of 1.5µsecs.

If the spacing between the commands is such that GTB starts, then it will be completed and straddle the HREQB rising edge as normal.

Handshake

The signals HREQB, HACKB and HBUSYB provide a handshake between the MA805 and the subsystem. On receipt of a bus message a request is made to the subsystem with HREQB. The subsystem must reply with either HACKB or HBUSYB within 1µsec, otherwise a handshake fail will be recorded. HACKB or HBUSYB must be held active until HREQB goes inactive, failure to do so will result in a handshake failure.

The response to HREQB does not affect the timing of the subsystem signals, (which are timed relative to the HREQB signal going active), but is a time window for a GO/handshake fail decision.

6. INITIATE REGISTER WRITE

Initiate Register Write is a selectable option (IRWB = 0). It transfers the contents of four MA805 registers to the subsystem. The registers are initialisation word, status word, BIT word and Last Command.

The IRW sequence has eight words. Each register word is preceded by a unique control word which can be used as an address (see data sheet).

The timings are fixed and there is no GTB (see Figure 6.1). The IRW sequence has low priority and will be aborted if the MA805 is required for command servicing.

There are two modes of operation:

1) Automatic (IRWB=0), (Figure 6.1 and 6.2).
2) On Request (IRWB pulsed low), (Figure 6.3).

1) Automatic (IRWB=0)

An IRW sequence is output to the subsystem following any 1553 Bus message with a valid command word for the RT.

The subsystem signals for the 1553 messages are as normal. After HREQB goes inactive at the end of the message, the IRW sequence normally starts after a delay of 1.5usecs. For Reset, self-test and internal BIT word mode codes (where there is extra MA805 activity after the subsystem transfer) there are larger delays before the IRW sequence is outputted.

2) On Request (IRWB pulsed low)

The subsystem initiates the IRW sequence from the MA805 internal registers by pulsing IRWB low 0.5usec minimum, provided that the terminal is not servicing a command (see Figure 6.3). If the terminal is busy then hold IRWB=0 until sequence is output.

	Symbol	Definition	Time	Units
			Typ	
PULSED INITIATE REGISTER WRITE	T- IRW- HR	IRW to HREQB going Active Low	2.5	us
	T-IRW-PULSED	IRW Pulse Width	0.5	us
DELAY IRW After Command (IRW=0)	T-IRW1	Normal HREQB inactive period (see T- RW2 to 4 for exceptions)	1.5	us
	T- IRW2	HREQB inactive period after Mode Code Reset	9.5	us
	T-IRW3	HREQB inactive period after Mode Code Internal Bit Word	21.5	us
	T-IRW4	HREQB inactive period after Mode Code Self-test	27.5	us
REGISTER WRITE SEQUENCE	T-HR-CL (IRW)	HREQB to first CLEB in register Write Sequence	2.5	us
	T-CL-CS (IRW)	CLEB to CSB in Register Write Sequence	2	us
	T- CS-CL (IRW)	CSB to CLEB in Register Write Sequence	2	us
	T-CS-HR (IRW)	Last CSB to HREQB in Register Write Sequence	1.5	us

The above times may have a spead of ±20ns.

Table 6.1: Electrical Characteristics

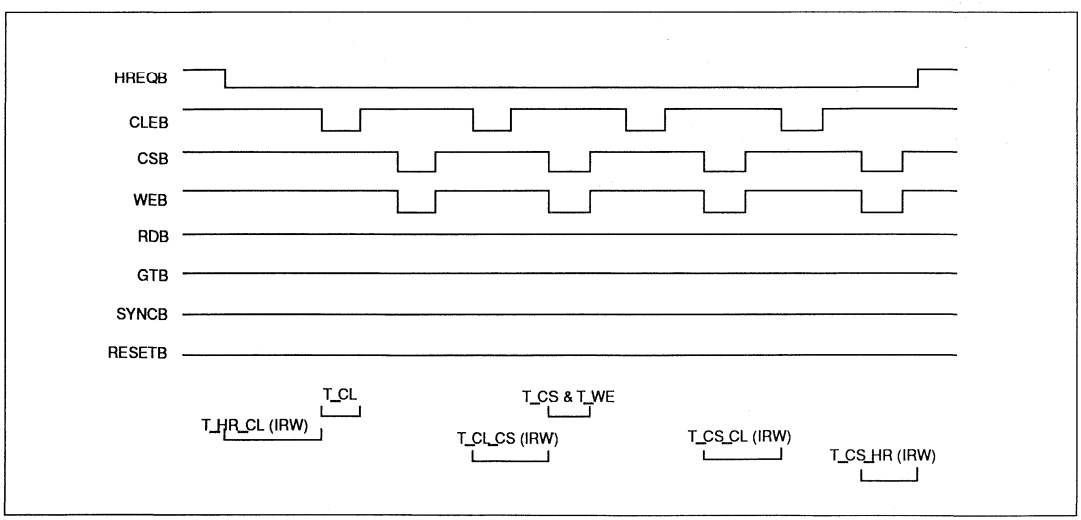


Figure 6.1: Register Write Sequence

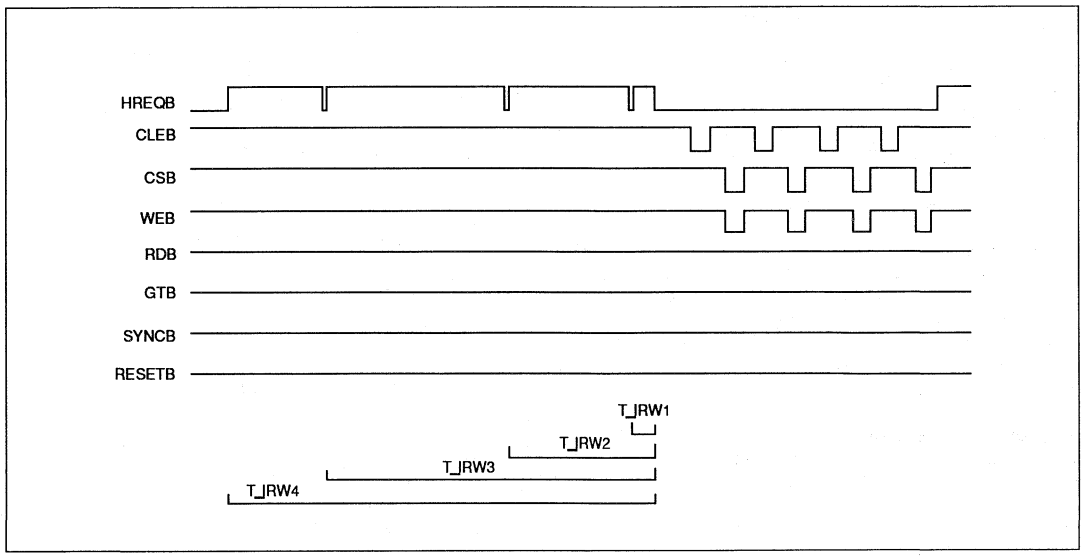


Figure 6.2: Register Write Output Times (IRW = 0)

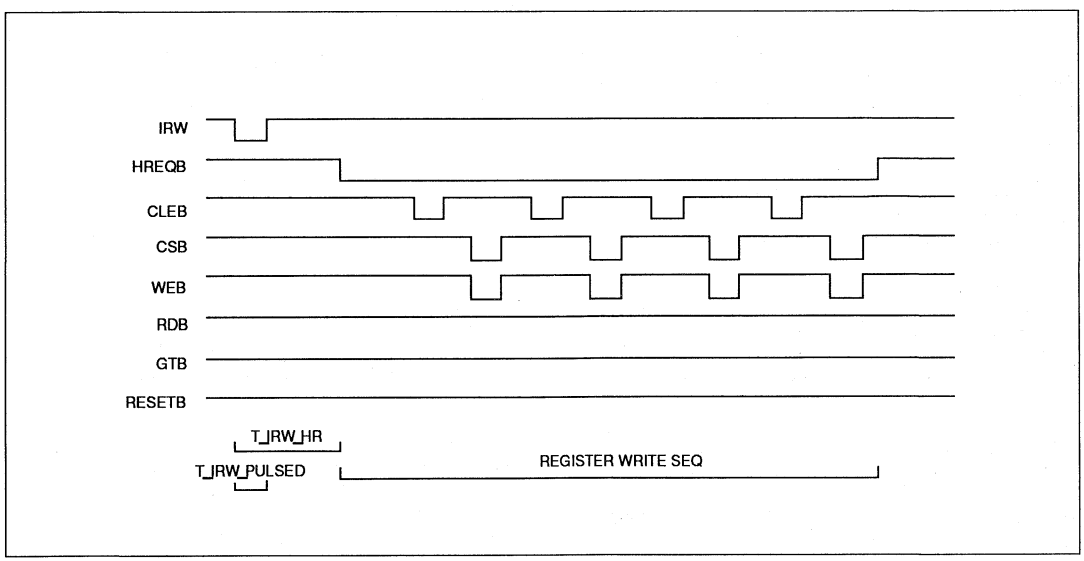


Figure 6.3: Register Write Time (IRW Pulsed Low)

7. Built-in-Test (BIT) Word Register

The MA805 contains a 16 bit register, called the BIT word register, which records message error and terminal status information supplementary to that given by the RT status word. There is an option (ABRB in the initialisation word) to select between this internal BIT word and an external BIT word.

7.1 Internal BIT word (ABRB = 1)

The internal BIT word is structured as shown in Figure 7.1. The BIT word contents will be reset to logic zero by a power up initialisation or subsystem initiated reset or a legal mode command to reset remote terminal, except for the broadcast inhibits which depend on the INITWORD. Additional reset conditions, if any, and the conditions for the setting of each bit are explained below:

BIT Word Reset Exceptions
The contents of the BIT word register shall not be altered by any of the following legal mode commands:

Transmit Status Word
Transmit Last Command
Transmit BIT Word

Transmitter Timeout Flag
This bit shall be set to logic one if a transmitter timeout occurs while the RT is transmitting. In addition, if the RT is issued with a legal Initiate Self Test mode command this bit shall be set if there is a fault in the transmitter timeout mechanism. The timeout mechanism within the transmitter is designed to operate after 680 us of terminal transmission.

Subsystem Handshake Failure
This bit shall be set to logic one if the subsystem does not acknowledge HREQB with either HACKB or HBUSYB within 1usec; or both are asserted; or the response (HACKB, HBUSYB) is removed before HREQB goes inactive.

Loop Test Failure
At all times while the terminal is transmitting the MA805 chip checks the terminal transmission for any sync, Manchester, parity or continuity error. This bit shall be set to logic one if any such error in the transmitted waveform is detected.

Mode T/R Bit Wrong
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified .

This bit shall be set to logic one if a valid mode command is received with a transmit/receive (T/R) bit opposite to that permitted by the Assigned Mode Code table in Appendix A.

Illegal Mode Command
This bit shall be reset to logic zero by the receptionoof any valid command word with the exceptions as specified.

This bit shall be set to logic one if either of the following two conditions arise:

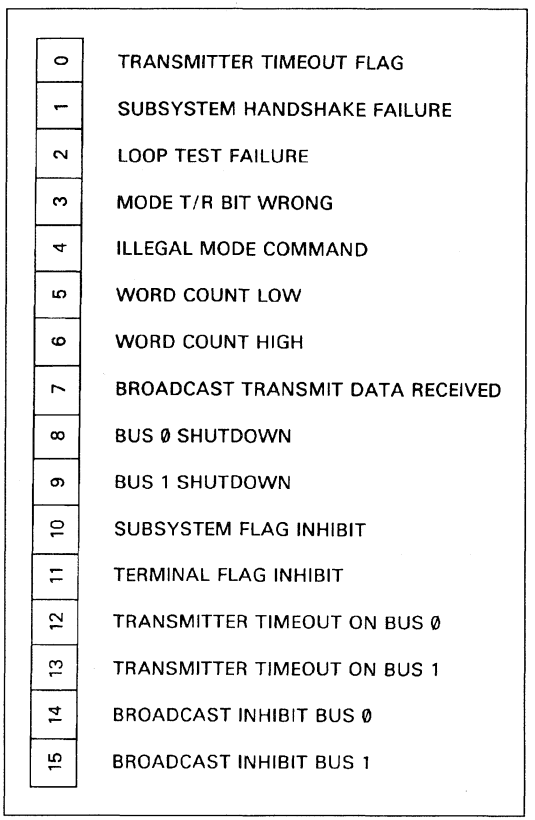


Figure 7.1

i) Reception of a valid mode command with the broadcast address, where this is not permitted.
ii) Reception of a valid mode command with a reserved mode command where this is not allowed by the subsystem.

Word Count Low
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified.

This bit shall be set to logic one if fewer valid data words are received than stipulated by the preceding valid command word.

Broadcast Transmit Data Received
This bit shall be reset to logic zero by the reception of any valid command word with the exceptions as specified.

This bit shall be set to logic one if a valid, non-mode command to transmit data words is received with the broadcast address.

Bus 0 Shutdown
This bit shall be set to logic one if bus 0 has been shutdown by one of the legal transmitter shutdown mode commands.

This bit shall be reset to logic zero if bus 0 is re-opened by one of the legal override transmitter shutdown mode commands.

Bus 1 Shutdown
This bit operates as bus 0 shutdown but relates to bus 1.

Subsystem Flag Inhibit
This bit shall be reset to logic zero if the INHSSFB bit in the STATMOD word is set to 1 except if the current command is transmit BIT word.

This bit shall be set to logic 1 if the INHSSFB bit in the STATMOD word is set to zero, except if the current command is transmit BIT word.

Terminal Flag Inhibit
This bit shall be reset to logic zero if the INHTFB bit in the STATMOD Word is set to 1 except if the current command is transmit BIT word.

This bit shall be set to logic one if the INHTFB bit in the STATMOD word is set to zero, except if the current command is transmit BIT word.

Transmitter Timeout on Bus 0
This bit shall be set to logic one if a transmitter timeout has occurred on bus 0.

Transmitter Timeout on Bus 1
This bit shall be set to logic one if a transmitter timeout has occurred on bus 1.

Broadcast Address recognition inhibited (Bus 0)
This bit shall be reset to logic zero after a reset if BCSTENO in the INITWORD is set to 1.

This bit shall be set to logic one after a reset if BCSTENO in the INITWORD is set to 0.

Broadcast Address recognition inhibited (Bus 1)
This bit shall be reset to logic zero after a reset if BCSTEN1 in the INITWORD is set to 1.

This bit shall be set to logic one after a reset if BCSTEN1 in the INITWORD is set to 0.

7.2 The BIT Word as a Expansion of the Status Word

Expansion of the Message Error Bit
Bits 3, 4, 5, 6 and 7 may be used to analyse the cause of the message error bit being set respectively into:

i) A mode command having being received with an incorrect T/R bit.
ii) A mode command having been received with a reserved mode code or an illegal broadcast address.
iii) Too few valid data words having been received.
iv) A message which was too long having been received.
v) A broadcast command to transmit data words having been received.

Expansion of the Subsystem Flag Bit
Bit 1 of the BIT word may be used to determine whether the Subsystem Flag is set due to an RT/Subsystem handshaking failure or due to the subsystem itself flagging a fault.

Expansion of the Terminal Flag Bit
Bits 0 and 2 of the BIT word may be used to analyse the cause of the Terminal Flag bit being set respectively into:

i) a transmitter timeout error having occurred.
ii) the terminal transmitting erroneous waveforms.

RT Self Test Results
If the RT fails its self test this will be reflected in the Status Word by the setting of the Terminal Flag bit.

The error source may be further analysed by presenting the RT with the following sequence of mode commands:

a) Reset Remote Terminal
b) Initiate Self Test
c) Transmit BIT Word

Bits 13, 12 and 0 of the BIT word may then be interpreted as follows:

Tx Timeout on Bus N	Tx Timeout Flag	
0	0	Self Test aborted due to superseding valid command
0	1	Transmitter timeout mechanism inoperative
1	0	Self Test good
1	1	Transmitter timeout mechanism operating incorrectly

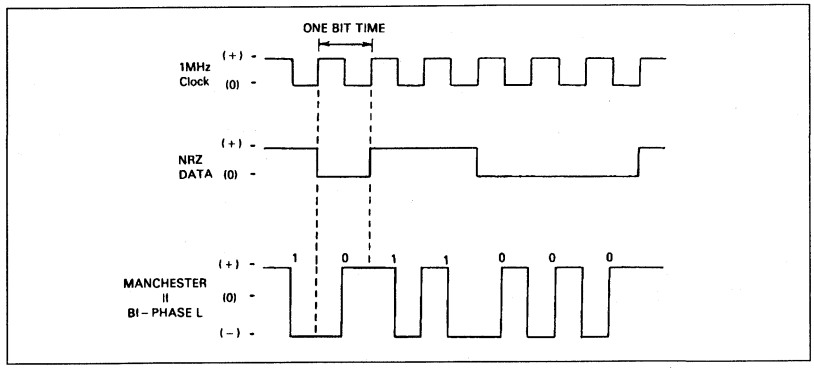
where N is the bus on which the self test command was issued.

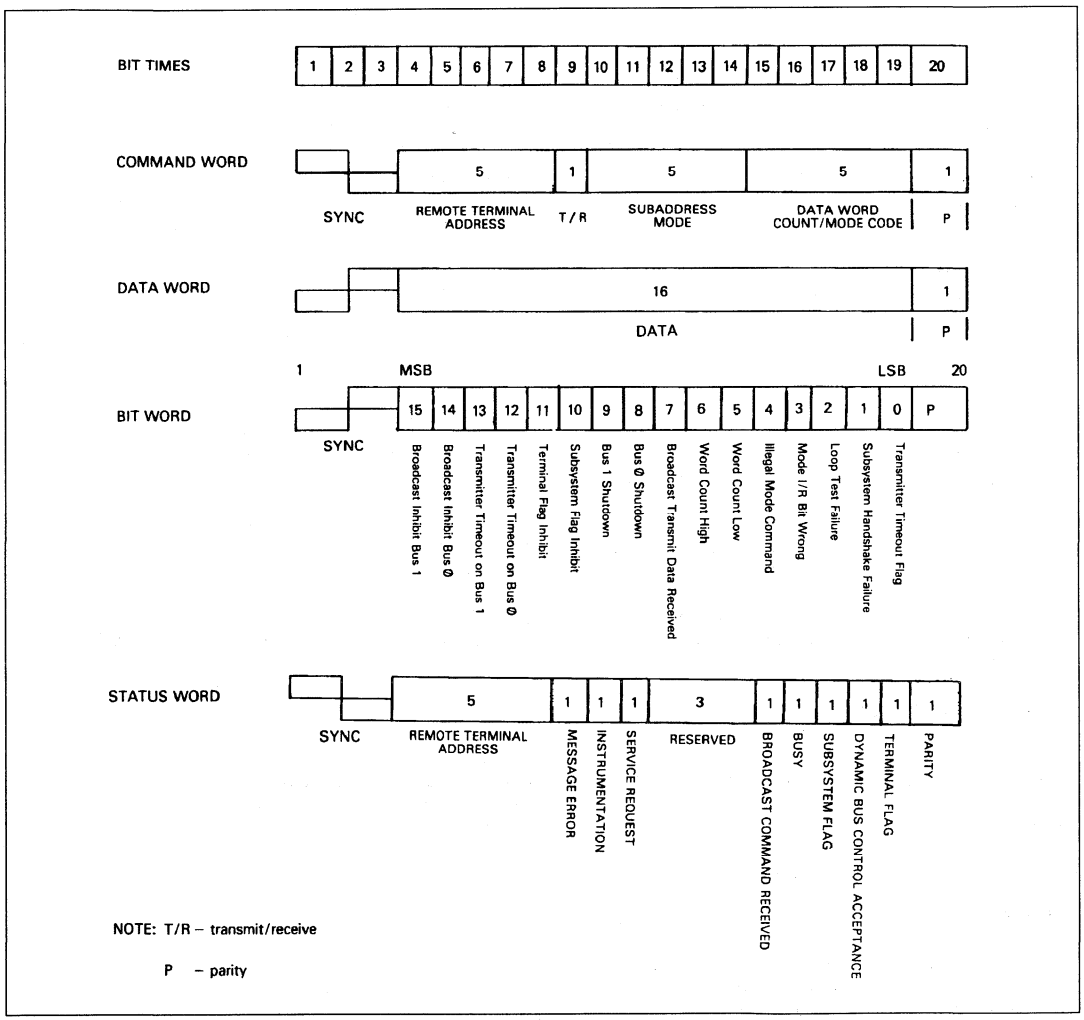
It should be noted that an RT self test forces the transmitter timeout mechanism to operate. The self test circuitry then checks:

a) that the mechanism does operate
and b) that the mechanism operates correctly.

7.3 External BIT Word (ABRB =0)
The BIT word is provided externally by the subsystem and is non-standard. It is an option to provide the subsystem designer with an alternative method of overall system monitoring.

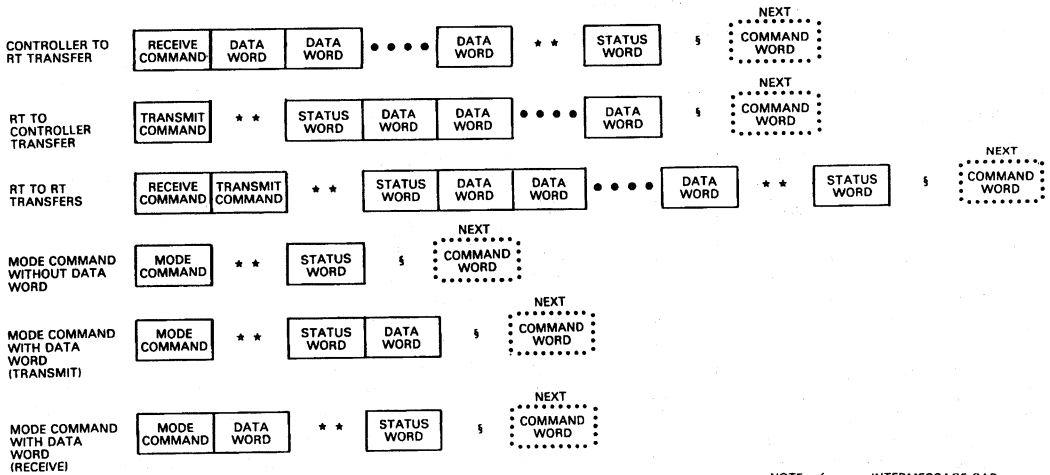
TRANSMISSION FORMATS





Appendix A.1: Data Encoding and Word Formats

TYPICAL MESSAGE FORMATS ASSIGNED MODE CODES



T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	Override Inhibit Terminal Flag Big	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
↓	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	Transmit BIT Word	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
↓	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

NOTE: To be determined (TBD)

Appendix A.2: Typical Message Formats and Assigned Mode Codes

MEMORY MAP

For MA805 using a chip select at address 2000 HEX and read signal (RDB 1 line), Sub address (SA 5 lines), current word count (CWC 5 lines)

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
0	00	00	2000	1	2000	STATUS MODIFIER WORD
0	00	01	2001	1	2001	NOT USED
0	00	02	2002	1	2002	NOT USED
0	00	03	2003	1	2003	NOT USED
0	00	04	2004	1	2004	NOT USED
0	00	05-07	2005	3	2005-07	NOT USED
0	00	08	2008	1	2008	NOT USED
0	00	09-1F	2009	23	201F	NOT USED
0	01	00-1F	2020	32	203F	SUBADDRESS 01 DATA TO BE TRANSMITTED
0	02	00-1F	2040	32	205F	SUBADDRESS 02 DATA TO BE TRANSMITTED
0	03	00-1F	2060	32	207F	SUBADDRESS 03 DATA TO BE TRANSMITTED
0	04	00-1F	2080	32	209F	SUBADDRESS 04 DATA TO BE TRANSMITTED
0	05	00-1F	20A0	32	20BF	SUBADDRESS 05 DATA TO BE TRANSMITTED
0	06	00-1F	20C0	32	20DF	SUBADDRESS 06 DATA TO BE TRANSMITTED
0	07	00-1F	20E0	32	20FF	SUBADDRESS 07 DATA TO BE TRANSMITTED
0	08	00-1F	2100	32	211F	SUBADDRESS 08 DATA TO BE TRANSMITTED
0	09	00-1F	2120	32	213F	SUBADDRESS 09 DATA TO BE TRANSMITTED
0	0A	00-1F	2140	32	215F	SUBADDRESS 10 DATA TO BE TRANSMITTED
0	0B	00-1F	2160	32	217F	SUBADDRESS 11 DATA TO BE TRANSMITTED
0	0C	00-1F	2180	32	219F	SUBADDRESS 12 DATA TO BE TRANSMITTED
0	0D	00-1F	21A0	32	21BF	SUBADDRESS 13 DATA TO BE TRANSMITTED
0	0E	00-1F	21C0	32	21DF	SUBADDRESS 14 DATA TO BE TRANSMITTED
0	0F	00-1F	21E0	32	21FF	SUBADDRESS 15 DATA TO BE TRANSMITTED
0	10	00 1F	2200	32	221F	SUBADDRESS 16 DATA TO BE TRANSMITTED
0	11	00-1F	2220	32	223F	SUBADDRESS 17 DATA TO BE TRANSMITTED
0	12	00-1F	2240	32	225F	SUBADDRESS 18 DATA TO BE TRANSMITTED
0	13	00-1F	2260	32	227F	SUBADDRESS 19 DATA TO BE TRANSMITTED
0	14	00-1F	2280	32	229F	SUBADDRESS 20 DATA TO BE TRANSMITTED
0	15	00-1F	22A0	32	22BF	SUBADDRESS 21 DATA TO BE TRANSMITTED
0	16	00-1F	22C0	32	22DF	SUBADDRESS 22 DATA TO BE TRANSMITTED
0	17	00-1F	22E0	32	22FF	SUBADDRESS 23 DATA TO BE TRANSMITTED
0	18	00-1F	2300	32	231F	SUBADDRESS 24 DATA TO BE TRANSMITTED
0	19	00-1F	2320	32	233F	SUBADDRESS 25 DATA TO BE TRANSMITTED
0	1A	00-1F	2340	32	235F	SUBADDRESS 26 DATA TO BE TRANSMITTED
0	1B	00-1F	2360	32	237F	SUBADDRESS 27 DATA TO BE TRANSMITTED
0	1C	00-1F	2380	32	239F	SUBADDRESS 28 DATA TO BE TRANSMITTED
0	1D	00-1F	23A0	32	23BF	SUBADDRESS 29 DATA TO BE TRANSMITTED
0	1E	00-1F	23C0	32	23DF	SUBADDRESS 30 DATA TO BE TRANSMITTED
0	1F	00	23E0	1	23E0	MODE CODE 00 NO DATA NO S/S NOT USED
0	1F	01	23EI	1	23EI	MODE CODE 01 NO DATA NO S/S NOT USED
0	1F	02	23E2	1	23E2	MODE CODE 02 NO DATA NO S/S NOT USED
0	1F	03	23E3	1	23E3	MODE CODE 03 NO DATA NO S/S NOT USED
0	1F	04	23E4	1	23E4	MODE CODE 04 NO DATA NO S/S NOT USED
0	1F	05	23E5	1	23E5	MODE CODE 05 NO DATA NO S/S NOT USED
0	1F	06	23E6	1	23E6	MODE CODE 06 NO DATA NO S/S NOT USED
0	1F	07	23E7	1	23E7	MODE CODE 07 NO DATA NO S/S NOT USED
0	1F	08	23E8	1	23E8	MODE CODE 08 NO DATA NO S/S NOT USED
0	1F	09	23E9	1	23E9	MODE CODE 09 NO DATA NO S/S NOT USED
0	1F	0A	23EA	1	23EA	MODE CODE 10 NO DATA NO S/S NOT USED

Appendix B.1

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
0	1F	0B	23EB	1	23EB	MODE CODE 11 NO DATA NO S/S NOT USED
0	1F	0C	23EC	1	23EC	MODE CODE 12 NO DATA NO S/S NOT USED
0	1F	0D	23ED	1	23ED	MODE CODE 13 NO DATA NO S/S NOT USED
0	1F	0E	23EE	1	23EE	MODE CODE 14 NO DATA NO S/S NOT USED
0	1F	0F	23EF	1	23EF	MODE CODE 15 NO DATA NO S/S NOT USED
0	1F	10	23F0	1	23F0	MODE CODE 16 DATA FROM SS VECTOR WORD
0	1F	11	23F1	1	23F1	MODE CODE 17 NO DATA NOT USED
0	1F	12	23F2	1	23F2	MODE CODE 18 DATA FROM SS NO S/S NOT USED
0	1F	13	23F3	1	23F3	MODE CODE 19 DATA FROM SS BITWORD
0	1F	14	23F4	1	23F4	MODE CODE 20 NO DATA - NOT USED
0	1F	15	23F5	1	23F5	MODE CODE 21 NO DATA - NOT USED
0	1F	16	23F6	1	23F6	MODE CODE 22 RESERVED MODE DATA
0	1F	17	23F7	1	23F7	MODE CODE 23 RESERVED MODE DATA
0	1F	18	23F8	1	23F8	MODE CODE 24 RESERVED MODE DATA
0	1F	19	23F9	1	23F9	MODE CODE 25 RESERVED MODE DATA
0	1F	1A	23FA	1	23FA	MODE CODE 26 RESERVED MODE DATA
0	1F	1B	23FB	1	23FB	MODE CODE 27 RESERVED MODE DATA
0	1F	1C	23FC	1	23FC	MODE CODE 28 RESERVED MODE DATA
0	1F	1D	23FD	1	23FD	MODE CODE 29 RESERVED MODE DATA
0	1F	1E	23FE	1	23FE	MODE CODE 30 RESERVED MODE DATA
0	1F	1F	23FF	1	23FF	MODE CODE 31 RESERVED MODE DATA
1	00	00	2400	1	2400	COMMAND WORD
1	00	01	2401	1	2401	INIT WORD (IRWB SEQ)
1	00	02	2402	1	2402	STATUS (IRWB SEQ)
1	00	03	2403	1	2403	NOT USED
1	00	04	2404	1	2404	BIT WORD (IRWB SEQ)
1	00	05	2405	1	2405	NOT USED
1	00	06	2406	1	2406	NOT USED
1	00	07	2407	1	2407	NOT USED
1	00	08	2408	1	2408	LAST COMMAND (IRWB SEQ)
1	00	09-1F	2409	23	241 F	NOT USED
1	01	00-1F	2420	32	243F	SUBADDRESS 01 RECEIVED DATA
1	02	00-1F	2440	32	245F	SUBADDRESS 02 RECEIVED DATA
1	03	00-1F	2460	32	247F	SUBADDRESS 03 RECEIVED DATA
1	04	00-1F	2480	32	249F	SUBADDRESS 04 RECEIVED DATA
1	05	00-1F	24A0	32	24BF	SUBADDRESS 05 RECEIVED DATA
1	06	00-1F	24C0	32	24DF	SUBADDRESS 06 RECEIVED DATA
1	07	00-1F	24E0	32	24FF	SUBADDRESS 07 RECEIVED DATA
1	08	00-1F	2500	32	251F	SUBADDRESS 08 RECEIVED DATA
1	09	00-1F	2520	32	253F	SUBADDRESS 09 RECEIVED DATA
1	0A	00-1F	2540	32	255F	SUBADDRESS 10 RECEIVED DATA
1	0B	00-1F	2560	32	257F	SUBADDRESS 11 RECEIVED DATA
1	0C	00-1F	2580	32	259F	SUBADDRESS 12 RECEIVED DATA
1	0D	00-1F	25A0	32	25BF	SUBADDRESS 13 RECEIVED DATA
1	0E	00-1F	25C0	32	25DF	SUBADDRESS 14 RECEIVED DATA
1	0F	00-1F	25E0	32	25FF	SUBADDRESS 15 RECEIVED DATA
1	10	00-1F	2600	32	261F	SUBADDRESS 16 RECEIVED DATA
1	11	00-1F	2620	32	263F	SUBADDRESS 17 RECEIVED DATA

Appendix B.2

RAM ADDR						
RDB	SA	CWC	BADDR	WORDS	EADDR	FUNCTION
1	12	00-1F	2640	32	265F	SUBADDRESS 18 RECEIVED DATA
1	13	00-1F	2660	32	267F	SUBADDRESS 19 RECEIVED DATA
1	14	00-1F	2680	32	269F	SUBADDRESS 20 RECEIVED DATA
1	15	00-1F	26A0	32	26BF	SUBADDRESS 21 RECEIVED DATA
1	16	00-1F	26C0	32	26DF	SUBADDRESS 22 RECEIVED DATA
1	17	00-1F	26E0	32	26FF	SUBADDRESS 23 RECEIVED DATA
1	18	00-1F	2700	32	271F	SUBADDRESS 24 RECEIVED DATA
1	19	00-1F	2720	32	273F	SUBADDRESS 25 RECEIVED DATA
1	1A	00-1F	2740	32	275F	SUBADDRESS 26 RECEIVED DATA
1	1B	00-1F	2760	32	277F	SUBADDRESS 27 RECEIVED DATA
1	1C	00-1F	2780	32	279F	SUBADDRESS 28 RECEIVED DATA
1	1D	00-1F	27A0	32	27BF	SUBADDRESS 29 RECEIVED DATA
1	1E	00-1F	27C0	32	27DF	SUBADDRESS 30 RECEIVED DATA
1	1F	00	27E0	1	27E0	MODE CODE 00 NO DATA
1	1F	01	27E1	1	27E1	MODE CODE 01 NO DATA
1	1F	02	27E2	1	27E2	MODE CODE 02 NO DATA
1	1F	03	27E3	1	27E3	MODE CODE 03 NO DATA
1	1F	04	27E4	1	27E4	MODE CODE 04 NO DATA
1	1F	05	27E5	1	27E5	MODE CODE 05 NO DATA
1	1F	06	27E6	1	27E6	MODE CODE 06 NO DATA
1	1F	07	27E7	1	27E7	MODE CODE 07 NO DATA
1	1F	08	27E8	1	27E8	MODE CODE 08 NO DATA
1	1F	09	27E9	1	27E9	MODE CODE 09 NO DATA
1	1F	0A	27EA	1	27EA	MODE CODE 10 NO DATA
1	1F	0B	27EB	1	27EB	MODE CODE 11 NODATA
1	1F	0C	27EC	1	27EC	MODE CODE 12 NO DATA
1	1F	0D	27ED	1	27ED	MODE CODE 13 NO DATA
1	1F	0E	27EE	1	27EE	MODE CODE 14 NO DATA
1	1F	0F	27EF	1	27EF	MODE CODE 15 NO DATA
1	1F	10	27F0	1	27F0	MODE CODE 16 NO DATA
1	1F	11	27F1	1	27F1	MODE CODE 17 DATA TO SS SYNCHRONISE DATA
1	1F	12	27F2	1	27F2	MODE CODE 18 NO DATA
1	1F	13	27F3	1	27F3	MODE CODE 19 NO DATA
1	1F	14	27F4	1	27F4	MODE CODE 20 DATA TO SS SELECTED TRANSMITTER SHUTDOWN DATA
1	1F	15	27F5	1	27F5	MODE CODE 21 DATA TO SS OVERRIDE SELECTED TRANSMITTER SHUTDOWN DATA
1	1F	16	27F6	1	27F6	MODE CODE 22 RESERVED MODE DATA
1	1F	17	27F7	1	27F7	MODE CODE 23 RESERVED MODE DATA
1	1F	18	27F8	1	27F8	MODE CODE 24 RESERVED MODE DATA
1	1F	19	27F9	1	27F9	MODE CODE 25 RESERVED MODE DATA
1	1F	1A	27FA	1	27FA	MODE CODE 26 RESERVED MODE DATA
1	1F	1B	27FB	1	27FB	MODE CODE 27 RESERVED MODE DATA
1	1F	1C	27FC	1	27FC	MODE CODE 28 RESERVED MODE DATA
1	1F	1D	27FD	1	27FD	MODE CODE 29 RESERVED MODE DATA
1	1F	1E	27FE	1	27FE	MODE CODE 30 RESERVED MODE DATA
1	1F	1F	27FF	1	27FF	MODE CODE 31 RESERVED MODE DATA

NO ASSOCIATED DATAWORD NOT USED

Appendix B.3

DS3043-1.2 December 1991

MA805

MIL-STD-1553B REMOTE TERMINAL

The complex transfer of data between subsystems, particularly in military and avionics systems has been significantly streamlined by the introduction of the Mil-Std-1553B Data Bus This standard is accepted by the US Military; by the UK as DEF STAN 00 - 18 Part 2; and by NATO as STANAG 3838.

The MA805 has been designed to meet full Mil-Std-1553B protocol for a remote terminal interface.

The single silicon gate CMOS device is capable of dual redundant operation without the need for complicated hardware or software support. All message formats, including all mode codes and broadcast commands can he serviced

The MA805 can also be configured to accept nonstandard 1553 protocol for use in industrial and commercial applications Reserved status bits and reserved mode commands can be made accessible by selection of the relevant options during command servicing. Data rates greater and less than the standard 1 MBit/s are possible and the status response can be delayed for certain applications. If no special functions are required, the MA805 powers up to the standard 1553B interface by default.

The MA805 can easily interface to sub-system memory and is flexible enough to ensure compatibility with a wide range of microprocessors. Data is transferred over a 16 bit highway between the MA805 and the subsystem. Error detection is included and the MA805 is capable of responding to error conditions in the correct manner without reference to the subsystem. Timeout counters prevent terminal latch-up problems and a separate inhibit line to the bus transceivers prevents excessive transmission on the bus.

The small size 40-lead DIL and LCC, make the MA805 particularly suited to applications where space is limited, and its low cost allows a cost-effective high integrity data transfer system for military, industrial, and commercial applications.

FEATURES

- Mil Temp Range -55° to +125°C
- Small Package
- Low power high speed CMOS technology
- Dual Bus Capability
- Full 1553B Remote Terminal protocol
- 16 Bit Highway
- SEAFAC Validated
- Suitable for MIL-STD-1760 Stores Applications

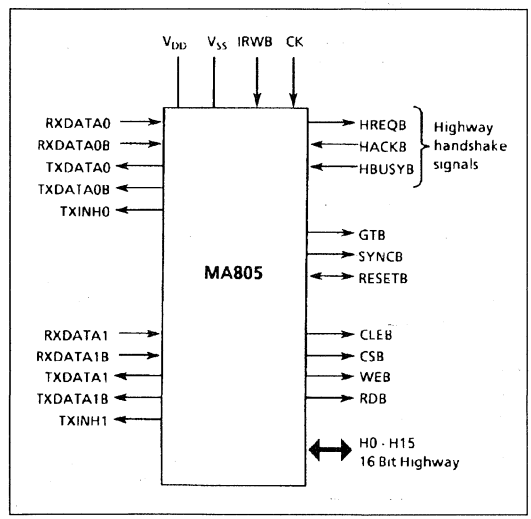


Figure 1: Full Dual Redundant 1553B Interface

1 SIGNAL DESCRIPTION

The B suffix denotes active low signals.

1.1 Supplies

V_{DD} - 5 Volts positive supply
V_{SS} - Ground

1.2 1553B Bus Interface Lines

RXDATA0 - Input. Positive threshold exceeded on bus 0
RXDATA0B - Input. Negative threshold exceeded on bus 0
TXINH0 - Output. Transmit inhibit for bus 0
TXDATA0 - Output. Drive bus 0 positive
TXDATA0B - Output. Drive bus 0 negative
RXDATA1 - Input. Positive threshold exceeded on bus 1
RXDATA1B - Input. Negative threshold exceeded on bus 1
TXINH1 - Output. Transmit inhibit for bus 1
TXDATA1 - Output. Drive bus 1 positive
TXDATA1B - Output. Drive bus 1 negative

1.3 Clock inputs

CK - 10MHz clock (for 1MHz data rate)

1.4 Subsystem interface lines

HREQB - Output. Highway REQuest. Indicates that the MA805 is currently servicing a command and hence requests control of the highway. Also operates during subsystem reset sequence.

HACKB - Input. Highway ACKnowledge. The subsystem responds to HREQB by setting HACKB low if the highway is not in use. Response must occur within 1us of HREQB going active.

HBUSYB - Input. Highway BUSY. Setting this line low causes the MA805 to relinquish control of the highway and set the busy bit in the status word.

RESETB[2] - Input/Output. Normally an output from the MA805. Active on power up and after reception of a RESET RT mode command. Also the subsystem can reset the entire terminal and reload the initialisation word by pulsing this line and HACKB low.

The subsystem should drive this line low from an open drain or open collector device. It is recommended that this signal be fitted with a 15kohm pull-up resistor.

GTB - Output. Good Transaction. Pulses low when a message has been received, passed all the validity and error checks and the appropriate transfers have taken place with the subsystem.

CLEB[1] - Output. Control Latch Enable. Active low when the control word is valid on the highway lines H15 - H0.

CSB[1] - Output. Chip Select. Used in conjunction with the read (RDB) and write (WEB) signals to control transfers between the MA805 and the subsystem.

WEB[1] - Output. Write. Active low when a word on the highway lines H15 - H0 is valid and is being transferred from the MA805 to the subsystem.

RDB[1] - Output. Read. Active low to enable a word to be read from the subsystem.

IRWB - Input. Initiate Register Write. This line allows access to the INITWORD, STATUS, BITWORD and LASTCMD registers of the MA805.

SYNCB - Output. SYNChronise. Pulses low when a synchronise mode command has been serviced with no errors.

H15 to H0[1] - Input/Outputs. Subsystem interface 16 line highway.

Notes:

[1] These three state outputs are high impedance when HACKB is inactive to allow the subsystem to drive these lines to control memory etc when the MA805 is not servicing a command. On chip resistors pull these signals to a high level when not being driven.

[2] The RESETB signal operates in conjunction with HREQB and HACKB. Initialisation data in the INITWORD is loaded into the MA805 typically 1us after HACKB has been driven active low.

2 SUBSYSTEM INTERFACE

The subsystem interface is a 16 line bidirectional highway. All transfers on this highway are initiated by the MA805 When the command servicing is complete the MA805 highway pins are in high impedance state, i.e., the highway can be used by the subsystem. The highway request (HREQB) indicates when the MA805 requires full control of the highway. The subsystem responds with HACKB to indicate the highway is available for use. This must occur within 1us of HREQB. If the subsystem is not prepared to allow the MA805 use of the highway, it indicates this by setting HBUSYB low.

For all the transfers, the MA805 will first write a control word (CONTWORD) which describes the required transfer. The CLEB signal indicates when the control word is valid. CSB, WEB and RDB are also used during transfers as shown in Figures 2, 3 and 4.

3 DEFINITION OF HIGHWAY WORDS

3.1 CONTWORD

CONTWORD is the control word used in the transfer sequences.

Bit	Name	Description	
15	BCST	Command word had the broadcast address	
14	RESMODE	Reserved mode code detected	
13	SYNCVEC	Synchronise/Transmit Vector Word (Note 1)	
12	CMDSTAT	Command/Status Word. (Note 2)	
11	NMD	Non Mode Data	1 = Normal data transfer
			0 = Mode data transfers
10	TR	Transmit/Receive bit of the command word	
9	SA4	(Note 3)	
8	SA3		
7	SA2		
6	SA1		
5	SA0		
4	CWC4		
3	CWC3		
2	CWC2		
1	CWC1		
0	CWC0		

Notes:

1. When bit 13 is high, a mode code to synchronise (with data word) or a mode code to transmit vector word is being serviced.

During the data word transfer, WEB is active when mode code synchronise is being serviced and RDB is active when mode code transmit vector word is being serviced.

2. When bit 12 is high, the command word is to be transferred to the subsystem and the status modifier word will be requested from the subsystem. WEB is active when the command word is being transfecred and RDB is active when the status modifier is required.

3. During data transfers the SA field contains the subaddress of the command word and the CWC field contains the current word count.

During command word, status modifier word and mode data transfers, the SA and CWC field are described below:

WEB	RDB	SA	CWC	
0	1	00	00	Command word
1	0	00	00	Status modifier word
0	1	01-1E	0-1F	Received data
1	0	01-1E	0-1F	Data to be transmitted
0	1	1F	0-1F	Mode data (to SS)
1	0	1F	0-1F	Mode data (from SS)

Command words, data words and data words associated with mode commands can thus be directly located in subsystem memory.

4. If IRWB (pin 39) is used to access the internal registers of the MA805, the following sequence will be output from the MA805:

CONTWORD = 0001 (HEX)
INITWORD
CONTWORD = 0002 (HEX)
STATUS
CONTWORD = 0004 (HEX)
BITWORD
CONTWORD = 0008 (HEX)
LASTCMD

5. If ABRB = 0 in the INITWORD, then the BIT word is read from the subsystem. The following CONTWORD will be output from the MA805 to address the external BIT word CONTWORD = 07F3 (HEX).

3.2 CMDWORD

The received command is transferred to the subsystem as the CMDWORD. The command word transferred to the subsystem is identical to the received command word. This allows the subsystem to verify that the correct terminal address has been loaded.

Bit	Name	Description
15 14 13 12 11	RTAD4 RTAD3 RTAD2 RTAD1 RTAD0	RT Address
10	TR	Transmit/Receive bit
9 8 7 6 5	SA4 SA3 SA2 SA1 SA0	Subaddress/mode
4 3 2 1 0	WC4 WC3 WC2 WC1 WC0	Data Word Count/Mode Code

3.3 STATMOD

Status modifier is read from the subsystem. It gives the subsystem limited control over the status bits and allows use of reserved mode codes.

Bit	Name	Description
15	SETMEB	Sets the message error (ME) bit of the current status register. This will also affect command servicing by preventing data transfers
14	SETSERVB	Sets the service request (SERV) bit of the current status register.
13	SETBUSYB	Sets the subsystem busy (BUSY) bit of the current status register. This will also affect command servicing by preventing data transfers.
12	SETSSFB	Set the subsystem flag (SSF) bit of the current status register.
11	SETTFB	Set the remote terminal flag (TF) bit of the current status register.
10	INHSSFB	Prevent the subsystem flag being set in the transmitted status word.
9	INHTFB	Prevent the remote terminal flag being set in the transmitted status word.
8	SETDBCAB	Set the dynamic bus control accept (DBCA) bit of the status register. This is ignored unless the current command is a mode command for dynamic bus control.
7	SETRES7B	Sets bit 7 of the current status register. Note that this is a reserved status bit.
6	SETRES6B	Sets bit 6 of the current status register. Note that this is a reserved status bit.
5	SETRES5B	Sets bit 5 of the current status register. Note that this is a reserved status bit.
4	SETINSTB	Sets the instrumentation (INST) bit of the current status register. Note that the instrumentation bit should always be zero for MIL STD 1553B. (i.e. SETINSTB = 1)
3	ALLOWB	This bit is only consulted when the received command is a mode command with a reserved mode code. The subsystem is able to decare such a command legal via this bit.
2	not used	
1	not used	
0	not used	

Note:

All the above bits are active low. If bits 15 to 8 only need to be set by the subsystem, the STATMOD word can be held in one octal latch. The highway has pull up resistors which cause undriven lines to adopt the default or not set condition. If the STATMOD latch is omitted, the subsystem cannot influence the status word and the MA805 will set status bits as required by the protocol.

3.4 INITWORD

This word is loaded on power up and includes the terminal address and operating conditions.

Bit	Name	Description
15	RTAD4	Remote terminal address bit 4
14	RTAD3	Remote terminal address bit 3
13	RTAD2	Remote terminal address bit 2
12	RTAD1	Remote terminal address bit 1
11	RTAD0	Remote terminal address bit 0
10	RTADPAR	Remote terminal address parity bit, odd parity is used.
9	BCSTEN1	Enable the broadcast address on bus 1
8	BCSTEN0	Enable the broadcast address on bus 0
7	FLAGOPB	Subsystem and terminal flag setting option. See note 2.
6	DELSTATB	Delay status response by 31.5uS
5	BUSCONB	Reserved for future use.
4	EFEB	External front end. Set to 1 for normal operation.
3	TM1B	Timeout multiplier bit 1. Set to 1 for normal operation.
2	TM0B	Timeout multiplier bit 0. Set to 1 for normal operation.
1	SLOWCKB	Clock control. This bit allows the chip to operate at non 1553 speeds. Set to 1 for normal operation. Set to 0 for slow speed
0	ABRB	Allow BIT read. This bit can be set low to indicate that the BUILT IN TEST word will be provided by the subsystem. The MA805 will access the BIT using CONTWORD = 07F3 (Hex).

Notes:

1. Bits 7 to 0 are active low. If the subsystem only needs to be able to set bits 15 to 8 then the INITWORD can be held in one octal latch. The highway has pull up resistors which cause undriven lines to adopt the default or not set condition.

2. FLAGOPB = 1. If the TF or SSF bit is set, it will remain set until some positive action is taken to clear the setting condition, i.e., Mode command to reset or local resetting. The same applies to TIME1, TIME0, LTF, HSF and TIMEOUT in the BIT word.

FLAGOPB = 0. If the TF or SSF bit is set, it will remain set until one status word has been transmitted with the bit set, except when responding to mode codes TRANSMIT STATUS/ TRANSMIT LAST COMMAND. The TF or SSF will then reset unless the fault condition is still present (i.e., SETTFB or SETSSFB in the STATMOD word are still active).

TIME1, TIME0, LTF, HSF and TIMEOUT in the BIT word will similarly reset after one transmission of the BIT word.

3. A receiving terminal will normally wait for 14uS to ensure that a transmitting terminal has responded within the permitted time. If no response is received within this period, the timeout mechanism prevents the terminal from using any data contained in the late response.

Propagation delays in long buses, (e.g., in ships or large industrial installations) could mean that the response time at the receiving end will exceed 14uS. Two bits in the INITWORD, TM0B and TM1B are used to extend the timeout period as shown below:

TM1B	TM0B	Receiver timeout (uS)
1	1	14 (default)
1	0	31
0	1	47
0	0	64

The times given in the right hand column are for a master clock (CK) rate of 10MHz.

4 SUBSYSTEM CONTROL SIGNALS

The subsystem must acknowledge that the MA805 has control of the highway using the HACKB signal, as described in the following sections.

4.1 MA805 to SS transfers

CSB indicates that the H15-H0 lines are valid. For transfers from the MA805 to the subsystem, the write signal WEB and CSB signal are both active when the H15-H0 lines are valid.

4.2 SS to MA805 transfers

CSB allows the subsystem to drive the H15-H0 lines. For transfers to the MA805 from the subsystem, the read signal RDB can be used as an address line to indicate the data to be read. CSB then enables the data onto the highway and is read by the MA805.

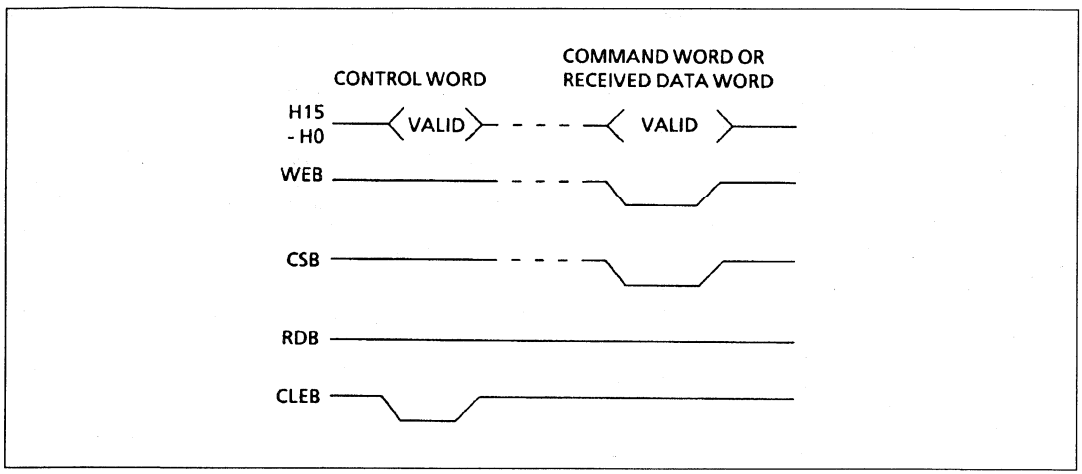


Figure 2: MA805 to Subsystem Transfer

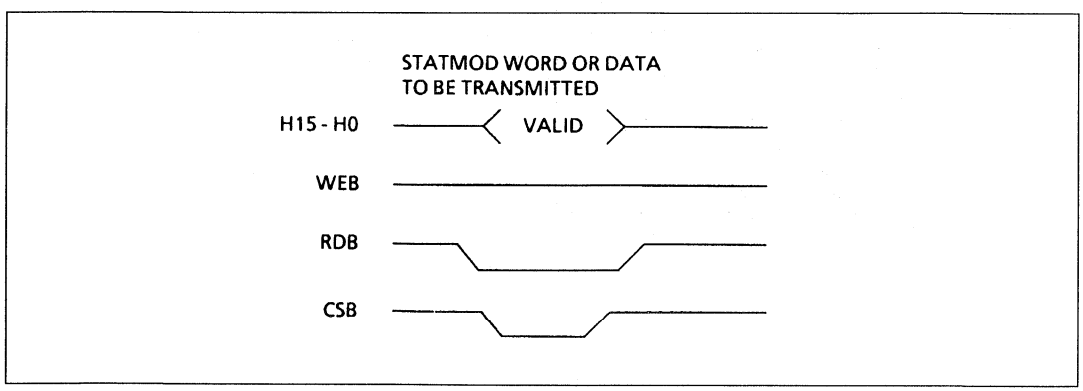
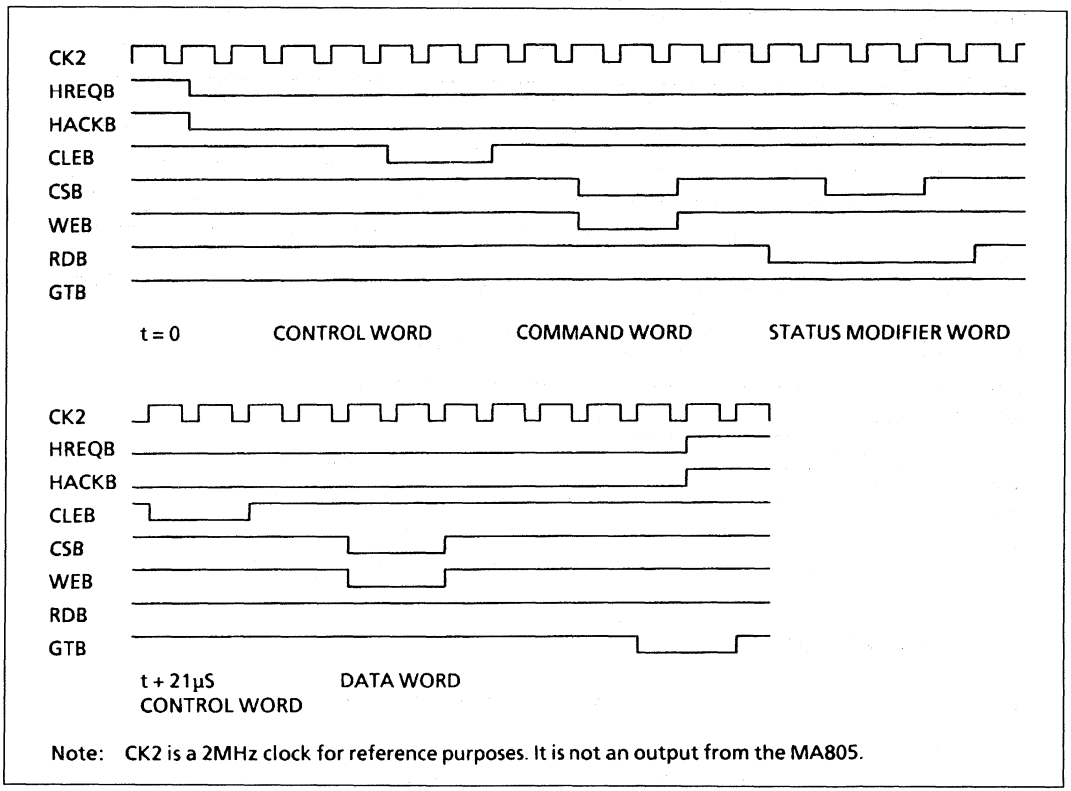


Figure 3: Subsystem to MA805 Transfer



Note: CK2 is a 2MHz clock for reference purposes. It is not an output from the MA805.

Figure 4: Receive Command Transfers (1 data word)

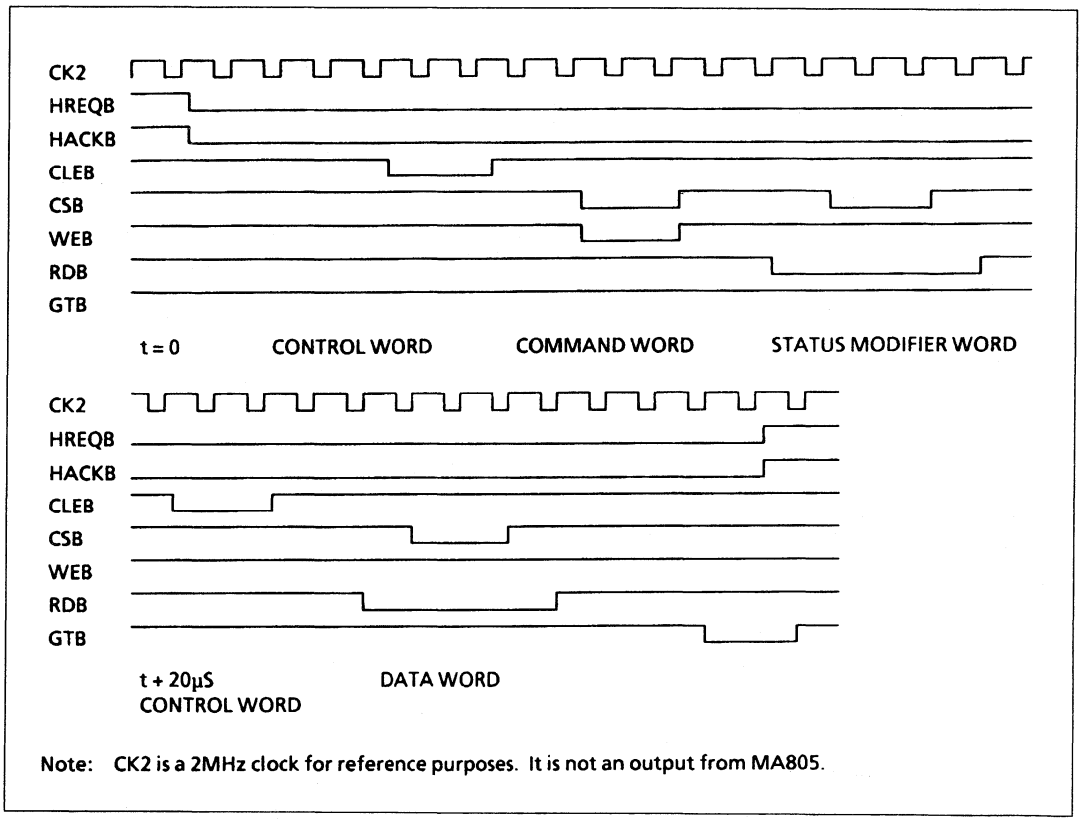


Figure 5: Transmit Command Transfers (1 data word)

5 SUBSYSTEM INTERFACING EXAMPLES

The MA805 has been designed to interface easily with all types of subsystem design, ranging from a simple set of latches to a complex microprocessor system. Two examples of subsystem interface are described:

5.1 Example 1

A simple interface which allows single 16 bit words to be read from and written to the subsystem. On power up, the MA805 resets internally and sends the RESETB and HREQB signals active. This is used to enable the static initialisation word onto the highway to be loaded into the MA805.

In Fig. 6 IC2 enables an 8 bit word onto the highway which is composed of the 5 bit RT address field and a parity bit. The other two bits are BCSTEN0 and BCSTEN1, which, when high, allow the terminal to accept broadcast commands on buses 0 and 1 respectively. Further options can be exercised by the addition of another 74HCT244 to allow the full 16 bit initialisation word to be used.

Data is transferred to the subsystem by means of the WEB (write) signal. In Fig. 6 WEB latches the data word from the 16 bit highway into two octal latches IC3 and IC4.

Data can be read from the subsystem using the RDB (read) signal to enable the output of a buffer, latch or memory. A full 1553B protocol terminal interface to a very basic subsystem is thus possible using a minimum of support logic.

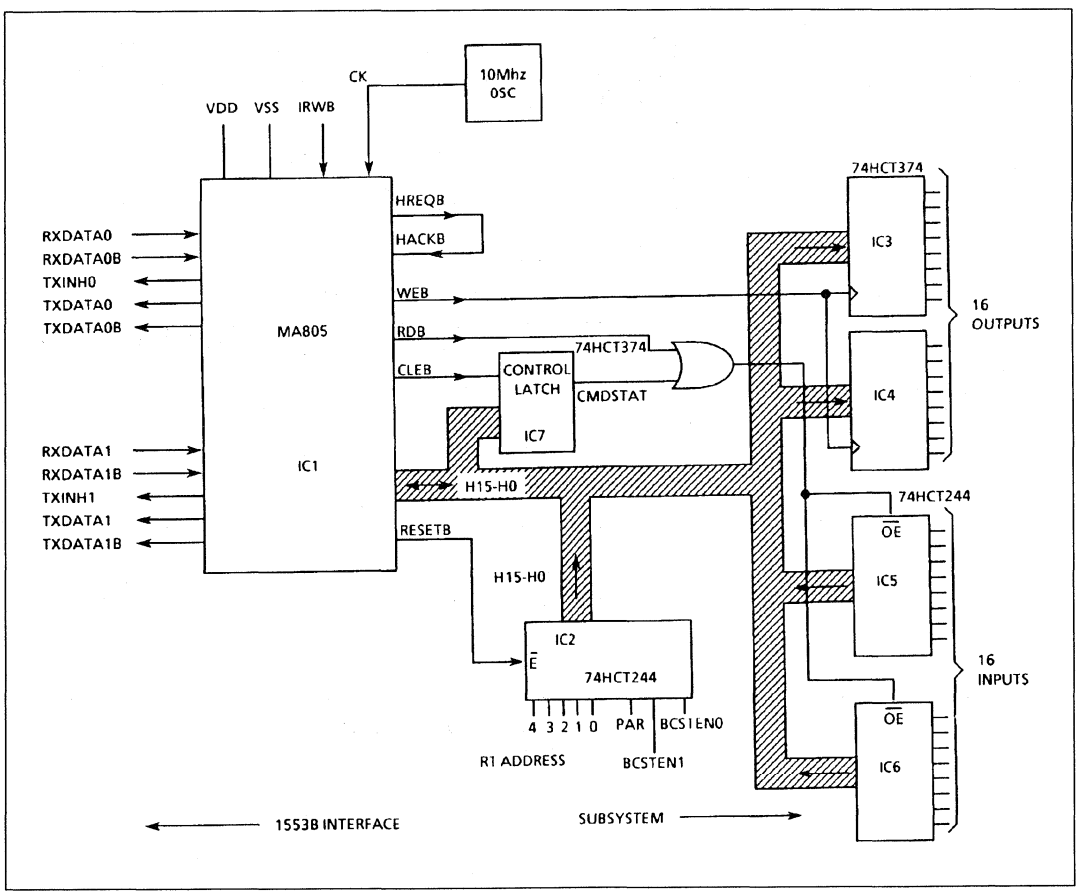


Figure 6: Minimum Interface to a Simple Subsystem

5.2 Example 2

For more complex subsystems capable of transferring up to 32 data words from up to 30 sub-addresses, a control word is available to provide the necessary address information.

Fig. 7 shows an interface to a RAM buffer memory. The control word is loaded into the control latch with the CLEB (Control Latch Enable) signal. In this example, the full 16 bit initialisation word is available to allow all options to be exercised. The control latch is updated before each subsystem transfer to indicate the subaddress and current word count of the next data word.

This provides a ten bit address field to provide a unique location for each word for every sub-address. The RDB signal is also used as a RAM address line, thus allowing data from the 1553B bus to the subsystem to be placed in a separate location to the data from the subsystem to the 1553B bus.

These examples highlight the flexibility of the MA805 which allows it to interface to a wide range of subsystems. Interfaces to double buffered memory, FIFOs, DMA to microprocessor systems are also possible without the need for excessive support logic.

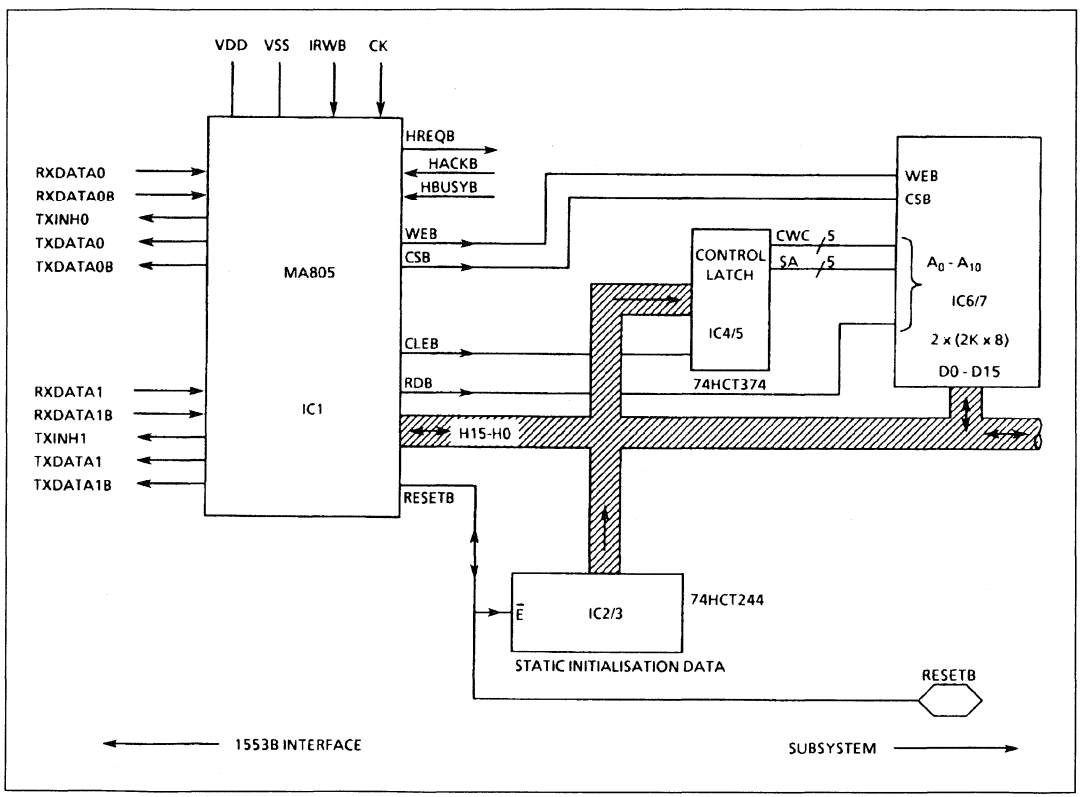


Figure 7: RAM Based Subsystem (all options selectable)

6 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply voltage (relative to V_{SS})	-0.3	8	V
Input voltage (all inputs)	-0.3	V_{DD}+0.3	V
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
V_{DD} Positive supply voltage	4.5	5.0	5.5	V
Operating temperature	-55	-	125	°C
I_{DDS} Standby Current	-	5	10	mA
I_{DDD} Mean operating Current	-	6	12	mA
Clock Frequency (note 1)	-	10	-	MHz
Clock high pulse width (note 1)	-	50	60	ns
Clock low pulse interval (note 1)	-	50	60	ns
Clock rise time	-	-	10	ns
Clock fall time	-	-	10	ns

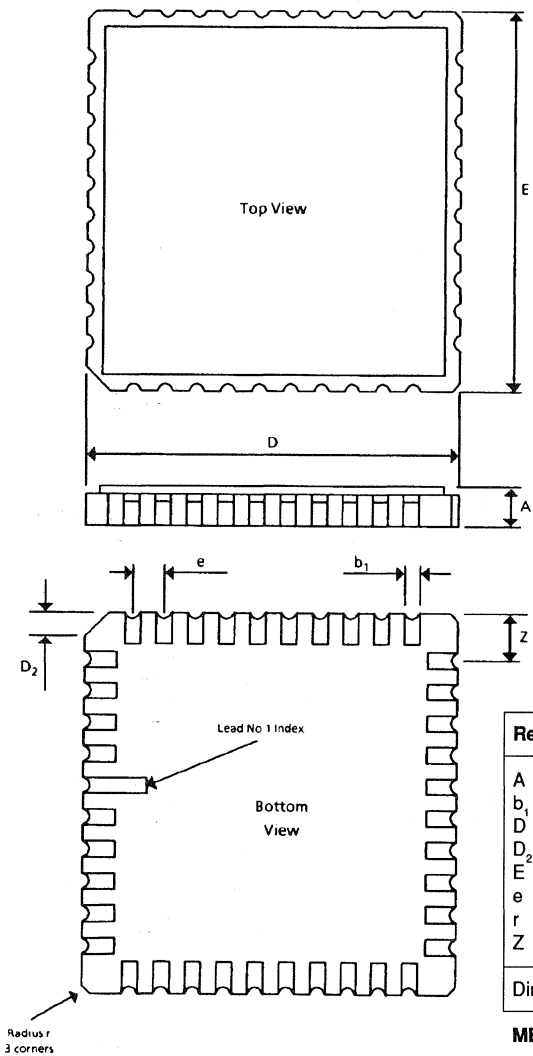
Note 1: For MIL-STD-1553B operation.

8 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
V_{IH}	TTL input high voltage	2.0	-	V
V_{IL}	TTL input low voltage	0	0.8	V
V_{OH}	TTL output high voltage	2.4	-	V
V_{OL}	TTL output low voltage	-	0.4	V
I_{IL}	Input low current	-0.1	-0.45	mA
I_{IH}	Input high current	-	10	uA
I_{OL}	Output low current	-	2.0	mA
I_{OH}	Output high current		-1.0	mA
C_{IN}	Input Capacltance	-	12	pF
V_{IHCK}	Input high voltage clock	V_{DD}-1	-	V
V_{ILCK}	Input low voltage clock	-	0.8	V

V_{DD} = 5V±10%, over full operating temperature range.

9 PACKAGING INFORMATION



Ref	Min	Nom	Max
A	-	-	2.16 (0.085)
b_1	-	0.51 (0.02)	-
D	-	-	12.57 (0.495)
D_2	-	0.711 (0.028)x45°	-
E	-	-	12.57 (0.495)
e	-	1.02 (0.04)	-
r	-	0.19 (0.0075)	-
Z	-	1.524 (0.06) typ	-

Dimensions in mm (inches)

MEDL XG430

Figure 8: 40-pad Leadless Chip Carrier (Package Style L)

Ref	Min	Nom	Max
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	51.31 (2.020)
e	-	2.54 (0.100) typ	-
e_1	-	15.24 (0.600) typ	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)
Z	-	-	1.27 (0.050)

Dimensions in mm (inches)

MEDL XG405

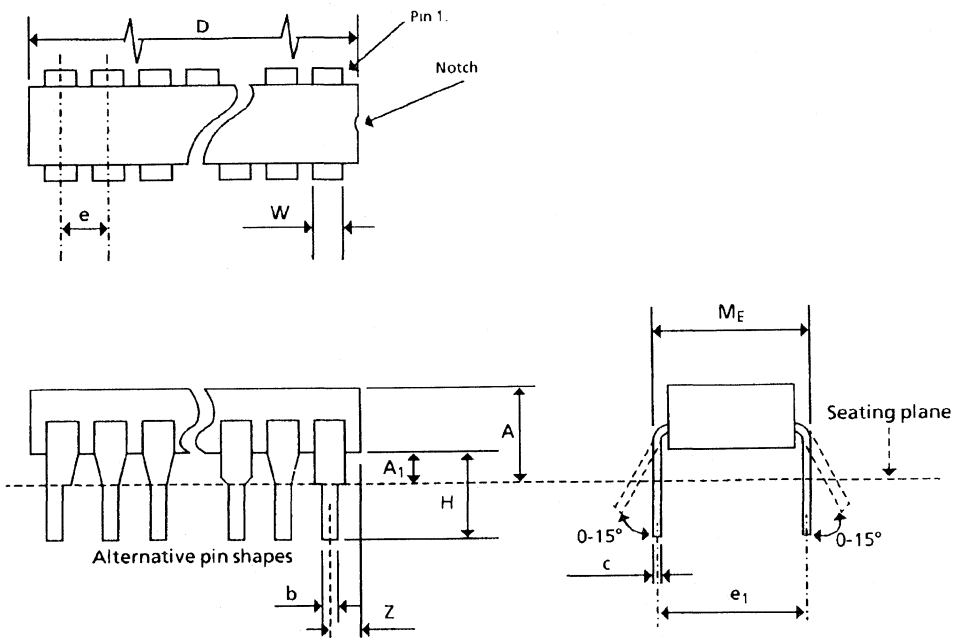


Figure 9: 40-lead Ceramic DIL - Solder Seal (Package Style C)

10 PINOUT INFORMATION

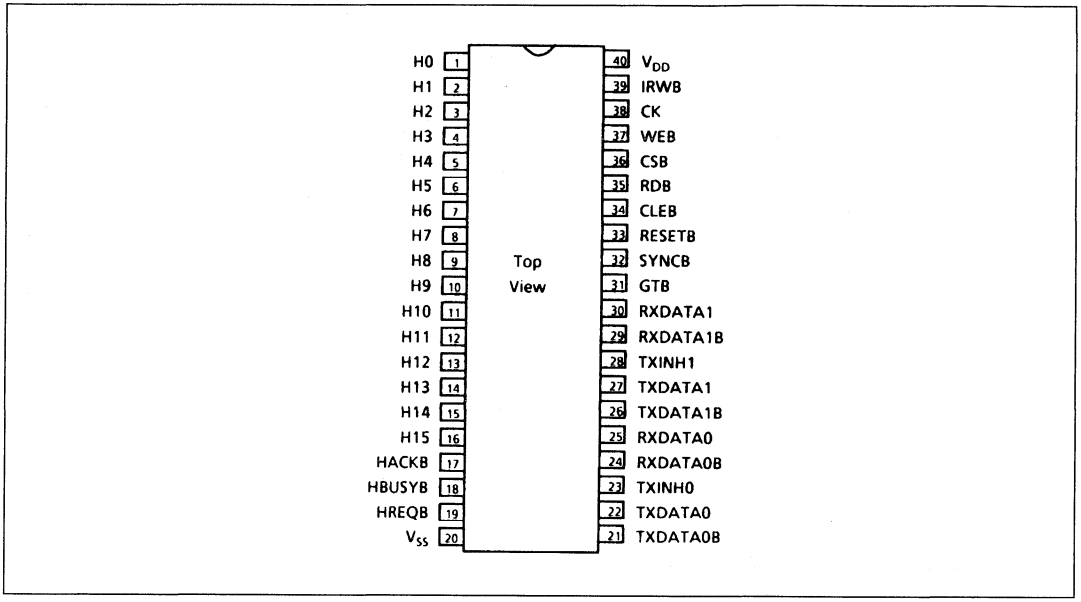


Figure 10: 40-lead Ceramic DIL - Solder Seal (Package Style C)

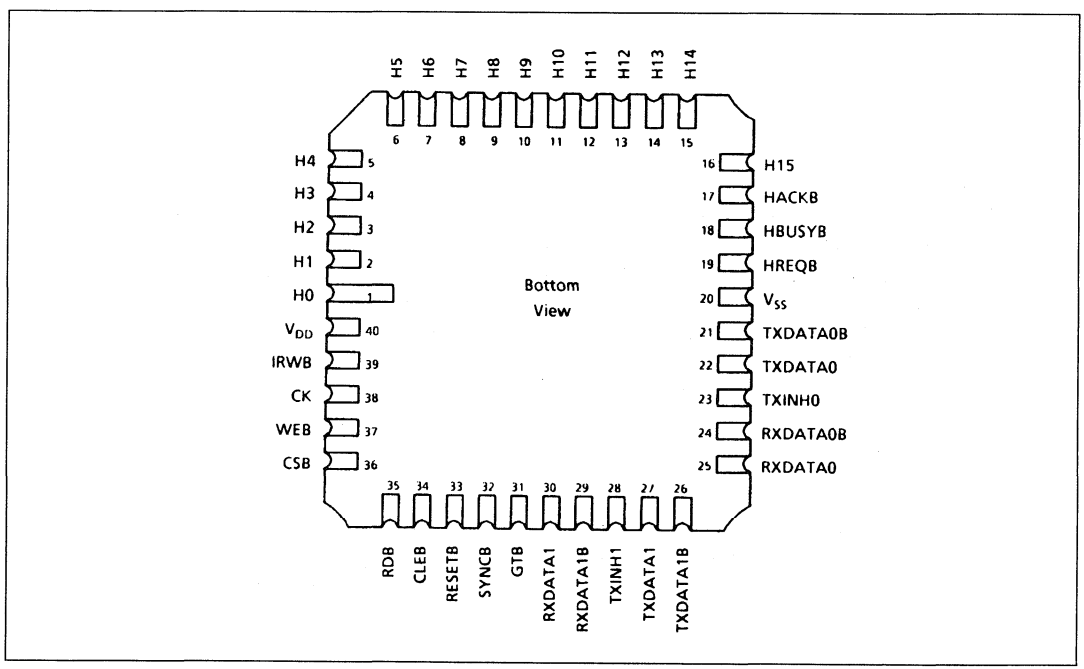
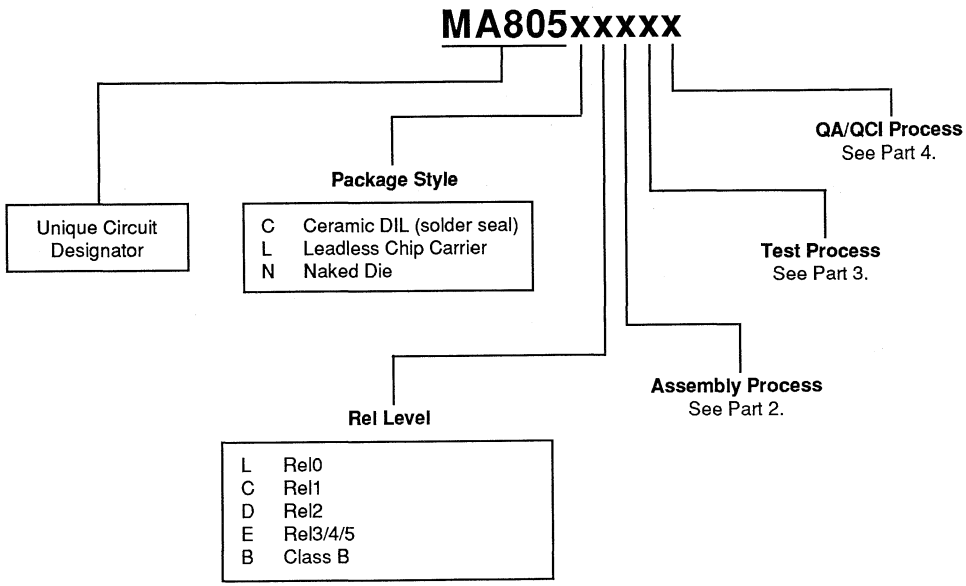


Figure 11: 40-pad Leadless Chip Carrier (Package Style L)

11 ORDERING INFORMATION

For details of quality levels, see 'Quality Assurance Standards Document 1'.

Other package styles and quality levels may be available on request.



Section 5
Sub-System Interfaces

CT2566

MIL-STD-1553 TO MICROPROCESSOR INTERFACE UNIT

GPS CT2566 MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface. It is available packaged in:

1) 78 pin DIL hybrid

2) 82 pin flatpack

3) PGA

The CT2566 provides an interface by using RAM allowing the CPU to transmit or receive 1553 traffic simply by accessing the memory.

All 1553 message transfers are entirely memory or I/O mapped. The CT2566 supports 1553 interface devices such as GPS's CT2512 dual RT or the CT2565 dual BC, RT, and MT.

The CT2566 operates over the full military –55°C to +125°C temperature range.

FEATURES

- Second source to the BUS-66300
- PGA Version available, (second source to the BUS-66312)
- Compatible with MIL-STD-1750 CPUs
- Compatible with MOTOROLA, INTEL, and ZILOG CPUs
- Compatible with GPS CT2565 BC/RT/MT and CT2512 RT
- Minimises CPU overhead
- Signal controls for shared memory implementation
- Transfers complete messages to shared memory
- Provides Memory Mapped 1553 Interface

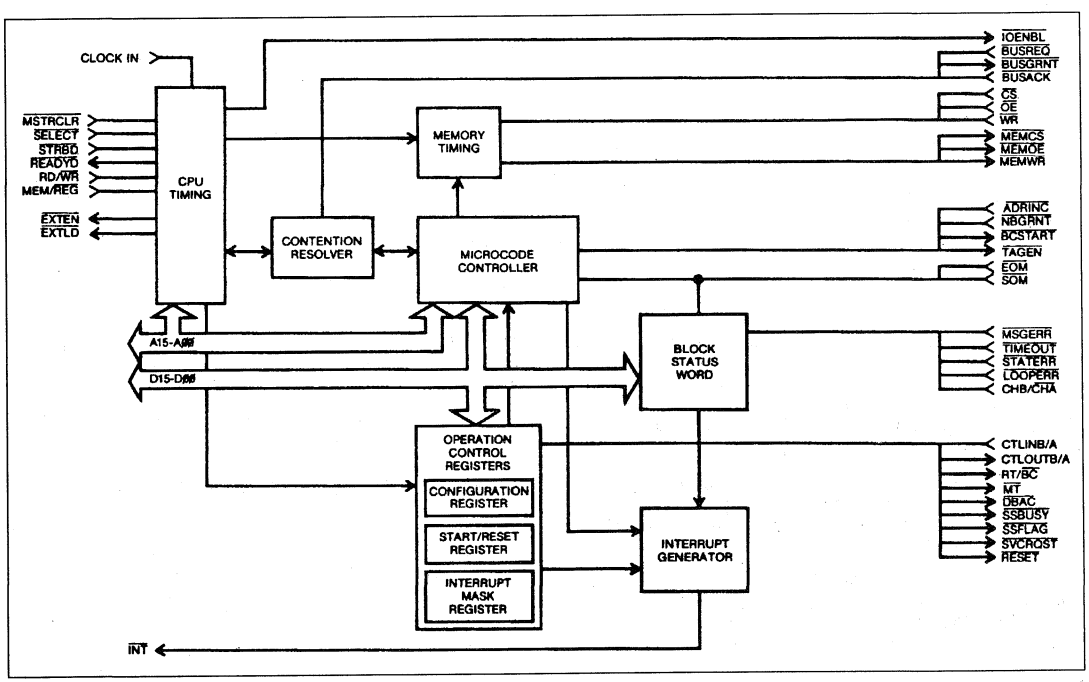


Figure 1: CT2566 Block diagram

SPECIFICATIONS

Specifications at nominal power supply voltages.		
PARAMETER	**UNITS**	**VALUE**
Logic		
I_{IH} (With V_{IH} = 2.7V)	µA	–630
I_{IL} (With V_{IL} = 0.0V)	µA	–700
I_{OH}	mA	4.0 min
I_{OL}	mA	4.0
V_{IH}	V	2.0
V_{IL}	V	0.8
V_{OH}	V	3.7
V_{OL}	V	0.4
Clock	MHz	12
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	10 typ
Temperature Range		
Operating (Case)	°C	–55 to +125
Storage	°C	–65 to +150
Physical Characteristics		
Size		
(78 pin DIP)	in	2.1 × 1.87 × 0.25
	(mm)	(53 × 47.5 × 6.4)
(82 pin flatpack)	in	2.1 × 1.87 × 25
	(mm)	(55.6 × 40.6 × 3.71)
Weight		
(78 pin DIP)	oz (g)	1 (28)
(82 pin flatpack)	oz (g)	1 (28)

Table 1: Specifications

GENERAL

The CT2566 was designed to perform required handshaking to the 1553 interface device, storing or retrieving message(s) from a user supplied RAM and notifying the CPU that a 1553 transaction has occurred. The CPU uses this RAM to read the received data as well as to store messages to be transmitted onto the Bus.

The CT2566 can be used to implement BC, RT, or MT operation and can be either memory mapped or I/O mapped to CPU address space. Registers internal to the CT2566 control its operation.

The CT2566 can access up to four external, user supplied registers and can address up to 64K words of RAM. The RAM selected must be a non-latched static RAM (capable of meeting the timing constraints for the CT2566). A double buffering architecture is provided to prevent incomplete or partially updated information from being transmitted onto the 1553 Data Bus.

The CT2566 requires an external, user supplied clock.

COMPATIBLE MICROPROCESSOR TYPES

The CT2566 may be used with most common microprocessors, including, the Motorola 68000 family, the Intel 8080 family, Zilog Z8000 products, and available MIL-STD-1750 processors.

Interfacing the CT2566 to the 1553 Data Bus requires external circuitry such as GPS's CT2565(BC/RT/MT) and CT1589D transceivers. Figure 2 shows the interconnection for these components.

PIN NO.	NAME	I/O	DESCRIPTION
1	$\overline{\text{SELECT}}$	I	Select. When active, selects CT2566 for operation.
2	RD/$\overline{\text{WR}}$	I	Read/Write. Controls CPU bus data direction.
3	$\overline{\text{READYD}}$	O	Ready Data. When active indicates data has been received from, or is available to the CPU.
4	$\overline{\text{EXTEN}}$	O	External Enable. Output from CT2566 to enable output from external devices. Same timing as $\overline{\text{MEMOE}}$.
5	$\overline{\text{TAGEN}}$	O	Tag Enable. Enables an external time tag counter for transferring the time tag word into memory.
6	$\overline{\text{EOM}}$	I	End of Message. Input from 1553 device indicating end of message.
7	$\overline{\text{SOM}}$	I	Start of Message. Input from 1553 device indicating start of message in RTU mode.
8	$\overline{\text{STATERR}}$	I	Status Error. Input from 1553 device when status word has either a bit set or unexpected RT address (in BC mode only).
9	$\overline{\text{ADRINC}}$	I	Address Increment. Sent from 1553 device to increment address counter following word transfer.
10	MEM/$\overline{\text{REG}}$	I	Memory/Register. Input from CPU to select memory or register data transfer.
11	CLOCK IN	I	Clock input; 50% duty cycle, 12MHz, max.
12	$\overline{\text{LOOPERR}}$	I	Loop Error. Input from 1553 device if short loop BIT fails.
13	$\overline{\text{BUSREQ}}$	I	Bus Request. When active, indicates 1553 device requires use of the address/ data bus.
14	$\overline{\text{BUSGRNT}}$	O	Bus Grant. Handshake output to 1553 device in response to BUS REQUEST indicating address/data bus available to 1553 device.
15	Not Used	-	-
16	$\overline{\text{MEMCS}}$	O	Memory Chip Select. Low from CT2566 to enable external RAM. Used with 4K × 4 RAM type device to read RAM or used in conjunction with $\overline{\text{MEMWR}}$ to write data into RAM.
17	$\overline{\text{OE}}$	I	Output Enable. Input from 1553 device used to enable memory on the parallel bus.
18	N/C	-	Not Used.
19	$\overline{\text{NBGRNT}}$	I	Low pulse from 1553 device preceding start of received new protocol sequence. Used with superseding command to reset DMA in progress.
20	+ 5 Volt	I	Logic power supply.
21	D15	I/O	Data Bus Bit 15 (MSB).
22	D13	I/O	Data Bus Bit 13.
23	D11	I/O	Data Bus Bit 11.
24	D09	I/O	Data Bus Bit 9.
25	D07	I/O	Data Bus Bit 7.
26	D05	I/O	Data Bus Bit 5.
27	D03	I/O	Data Bus Bit 3.
28	D01	I/O	Data Bus Bit 1.
29	$\overline{\text{SSFLAG}}$	O	Subsystem Flag. Output to 1553 device to set RT subsystem flag status bit.
30	$\overline{\text{SSBUSY}}$	O	Subsystem Busy. Output to 1553 device to set RT subsystem busy flag.
31	RTU/$\overline{\text{BC}}$	O	Output to 1553 device used in conjunction with MT to set operating mode.
32	A14	O	Address Bit 14.
33	A12	O	Address Bit 12.
34	A10	O	Address Bit 10.
35	A08	O	Address Bit 8.
36	A06	O	Address Bit 6.
37	A04	O	Address Bit 4.
38	A02	I/O	Address Bit 2.

Table 2: CT2566 Pin Functions (78 Pin Dip)

PIN NO.	NAME	I/O	DESCRIPTION
39	A00	I/O	Address Bit 0 (LSB).
40	GND	-	Signal Return.
41	$\overline{\text{STRBD}}$	I	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to indicate a data transfer cycle to/ from CPU.
42	$\overline{\text{IOEN}}$	O	Input/Output Enable. Output from CT2566 to enable external buffers/latches connecting the hybrid to the address/data bus.
43	$\overline{\text{EXTLD}}$	O	External Load. Used to load data into external device via the CT2566 data bus. Same timing as MEMWR.
44	CHB/$\overline{\text{CHA}}$		Input from 1553 in RT mode used to indicate received 1553 message came in either Channel A or B.
45	$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
46	$\overline{\text{BCSTART}}$	O	Bus Controller Start. Outputs to 1553 in initiate BC cycle.
47	$\overline{\text{RESET}}$	O	Reset. Output to external device from CT2566 consisting of the OR condition of CPU reset and CPU Master Clear.
48	MSGERR	I	Message Error. Input from 1553 device when an error occurs in message sequence.
49	CTLIN B/$\overline{\text{A}}$	I	Input to change active memory map area (0 = area A).
50	CTLOUT B/$\overline{\text{A}}$	O	Output from CT2566 selecting which area is to be active (0 = area A).
51	$\overline{\text{TIMEOUT}}$	I	Input from 1553 device indicating no response time-out.
52	$\overline{\text{MSTRCLR}}$	I	Master Clear. Power-on reset from CPU. Resets DMA in progress and internal registers to logic "O".
53	$\overline{\text{BUSACK}}$	I	Bus Acknowledge. Input from 1553 device acknowledge receipt of $\overline{\text{BUSGRNT}}$.
54	$\overline{\text{WR}}$	I	Write. Input from 1553 device for writing data into memory.
55	$\overline{\text{CS}}$	I	Chip Select. Input from 153 device that is routed to $\overline{\text{MEMCS}}$.
56	$\overline{\text{MEMOE}}$	O	Memory Output Enable. Output from CT2566 to enable memory output data.
57	MEMWR	O	Memory Write. Output pulse from CT2566 to write data bus data into memory.
58	Not Used	-	-
59	$\overline{\text{MT}}$	O	Bus Monitor. Used in conjunction with RTU/$\overline{\text{BC}}$ to set operating mode.
60	D14	I/O	Data Bus Bit 14.
61	D12	I/O	Data Bus Bit 12.
62	D10	I/O	Data Bus Bit 10.
63	D08	I/O	Data Bus Bit 8.
64	D06	I/O	Data Bus Bit 6.
65	D04	I/O	Data Bus Bit 4.
66	D02	I/O	Data Bus Bit 2.
67	D00	I/O	Data Bus Bit 0 (LSB).
68	$\overline{\text{SVCREQ}}$	O	Service Request. Used to set service request bit in RT Block Status Word.
69	$\overline{\text{DBAC}}$	O	Dynamic Bus Acceptance. Used to set status bit in RT Block Status Word.
70	A15	O	Address Bit 15 (MSB).
71	A13	O	Address Bit 13.
72	A11	O	Address Bit 11.
73	A09	O	Address Bit 9.
74	A07	O	Address Bit 7.
75	A05	O	Address Bit 5.
76	A03	O	Address Bit 3.
77	A01	I/O	Address Bit 1.
78	GND	-	Chassis Ground.

Table 2: CT2566 Pin Functions (78 Pin Dip) (Continued)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	N/C	42	N/C
2	$\overline{\text{SELECT}}$	43	GROUND
3	$\overline{\text{STRBD}}$	44	CHASSIS GROUND
4	RD/$\overline{\text{WR}}$	45	A00 (LSB)
5	$\overline{\text{IOENBL}}$	46	A01
6	$\overline{\text{READYD}}$	47	A02
7	$\overline{\text{EXTLD}}$	48	A03
8	$\overline{\text{EXTEN}}$	49	A04
9	CHB/$\overline{\text{CHA}}$	50	A05
10	$\overline{\text{TAGEN}}$	51	A06
11	$\overline{\text{INT}}$	52	A07
12	$\overline{\text{EOM}}$	53	A08
13	$\overline{\text{BCSTART}}$	54	A09
14	$\overline{\text{SOM}}$	55	A10
15	$\overline{\text{RESET}}$	56	A11
16	$\overline{\text{STATERR}}$	57	A12
17	$\overline{\text{MSGERR}}$	58	A13
18	$\overline{\text{ADRINC}}$	59	A14
19	CTLIN B/$\overline{\text{A}}$	60	A15
20	MEM/$\overline{\text{REG}}$	61	RTU/$\overline{\text{BC}}$
21	CTLOUT B/$\overline{\text{A}}$	62	$\overline{\text{DBAC}}$
22	CLOCK IN	63	$\overline{\text{SSBUSY}}$
23	$\overline{\text{TIMEOUT}}$	64	$\overline{\text{SVCREQ}}$
24	$\overline{\text{LOOPERR}}$	65	$\overline{\text{SSFLAG}}$
25	$\overline{\text{MSTRCLR}}$	66	D00
26	$\overline{\text{BUSYREQ}}$	67	D01
27	$\overline{\text{BUSACK}}$	68	D02
28	$\overline{\text{BUSGRNT}}$	69	D03
29	$\overline{\text{WR}}$	70	D04
30	N/C	71	D05
31	$\overline{\text{CS}}$	72	D06
32	$\overline{\text{MEMCS}}$	73	D07
33	$\overline{\text{MEMOE}}$	74	D08
34	$\overline{\text{OE}}$	75	D09
35	$\overline{\text{MEMWR}}$	76	D10
36	Not Used	77	D11
37	N/C	78	D12
38	$\overline{\text{NBGRNT}}$	79	D13
39	$\overline{\text{MT}}$	80	D14
40	+5V	81	D15
41	N/C	82	N/C

Table 3: CT2566FP Pin Functions (82 Pin Flatpack)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	NC	F01	$\overline{\text{SSBUSY}}$
A02	A09	F02	$\overline{\text{DBAC}}$
A03	A08	F03	RTU/$\overline{\text{BC}}$
A04	A06	F11	CLOCKOUT
A05	A05	F12	VCC
A06	A03	F13	CLOCKIN
A07	A02	G01	$\overline{\text{SSFLAG}}$
A08	GND	G02	VCC
A09	$\overline{\text{NBGRNT}}$	G03	$\overline{\text{SVCRQST}}$
A10	$\overline{\text{OE}}$	G11	GND
A11	$\overline{\text{MEMCS}}$	G12	CTLOUTB/$\overline{\text{A}}$
A12	NC	G13	VCC
A13	$\overline{\text{CS}}$	H01	D00
B01	NC	H02	D01
B02	GND	H03	GND
B03	NC	H11	$\overline{\text{ADRINC}}$
B04	A07	H12	CTLINB/$\overline{\text{A}}$
B05	GND	H13	MEM/$\overline{\text{REG}}$
B06	VCC	J01	D02
B07	A00	J02	D03
B08	$\overline{\text{ADRDIR}}$	J12	$\overline{\text{STATERR}}$
B09	$\overline{\text{MEMWR}}$	J13	$\overline{\text{MSGERR}}$
B10	$\overline{\text{MEMOE}}$	K01	D04
B11	NC	K02	D05
B12	GND	K12	$\overline{\text{SOM}}$
B13	$\overline{\text{BUSGRNT}}$	K13	$\overline{\text{RESET}}$
C01	A11	L01	VCC
C02	A10	L02	D07
C06	A04	L06	D13
C07	A01	L07	$\overline{\text{DDIR}}$
C08	$\overline{\text{MT}}$	L08	$\overline{\text{IOENBL}}$
C12	$\overline{\text{WR}}$	L12	$\overline{\text{EOM}}$
C13	$\overline{\text{BUSACK}}$	L13	$\overline{\text{BCSTART}}$
D01	A13	M01	D06
D02	A12	M02	GND
D12	$\overline{\text{BUSREQ}}$	M03	D08
D13	$\overline{\text{MSTRCLR}}$	M04	D10
E01	A15	M05	D12
E02	A14	M06	D14
E12	$\overline{\text{LOOPERR}}$	M07	VCC
E13	$\overline{\text{TIMEOUT}}$	M08	RD/$\overline{\text{WR}}$

Table 4: CT2566PGA Pin Functions (Pin Grid Array)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
M09	GND	N05	GND
M10	$\overline{\text{EXTEN}}$	N06	D15
M11	$\overline{\text{INT}}$	N07	$\overline{\text{SELECT}}$
M12	GND	N08	$\overline{\text{STRBED}}$
M13	VCC	N09	$\overline{\text{READYD}}$
N01	NC	N10	$\overline{\text{EXTLD}}$
N02	NC	N11	CHB/$\overline{\text{CHA}}$
N03	D09	N12	$\overline{\text{TAGEN}}$
N04	D11	N13	NC

Table 4: CT2566PGA Pin Functions (Pin Grid Array) (Continued)

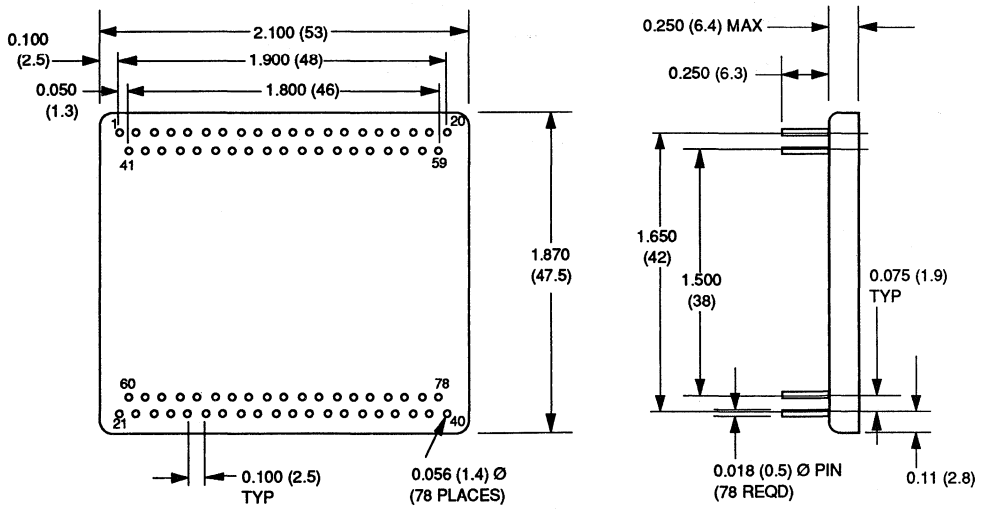


Figure 2: Mechanical Outline (78 Pin DIP)

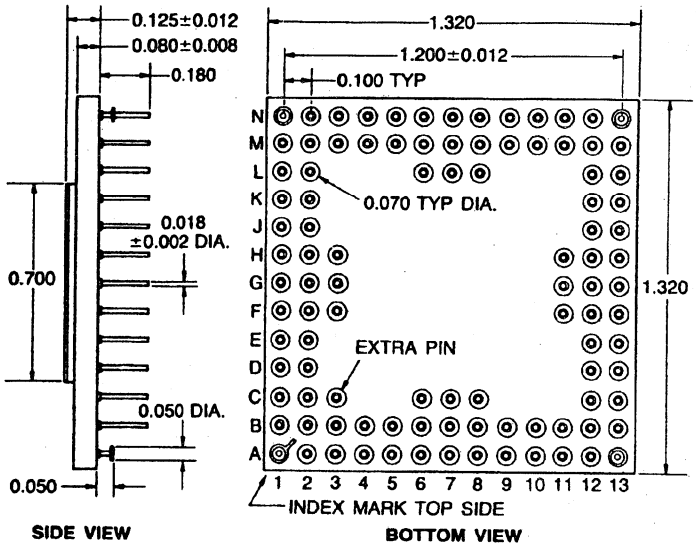


Figure 3: Mechanical Outline (CT2566PGA)

Section 6
Encoder/Decoders

DS3226-1.2 January 1992

MA15530

CMOS MANCHESTER ENCODER - DECODER

The MA15530 is a high performance CMOS integrated circuit used to implement MIL-STD-1553 and similar Manchester II encoded, time division multiplexed, serial data protocols. The device is divided into two independent sections, encoder and decoder, with a common master reset. The function of the encoder section is to produce the sync pulse and parity bit, and encode the data bits. The decoder section recognises the sync pulse, decodes the data bits and checks for parity.

The MA15530 is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over the full temperature and supply voltage ranges. The device interfaces with CMOS, TTL and N-channel support circuitry and operates from a standard 5 volt supply. The circuit can also be used in many party line digital data communications applications.

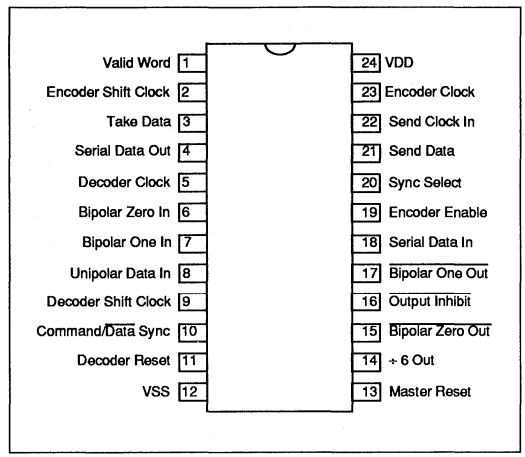


Figure 1: Pin Assignment

FEATURES

- MIL-STD-1553 Compatible
- 1.25 megabit/sec. Maximum Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode/Decode
- Separate Encoder and Decoder Sections
- Low Operating Power
- Military Temperature Range -55°C to 125°C
- Direct Replacement for Harris HD15530

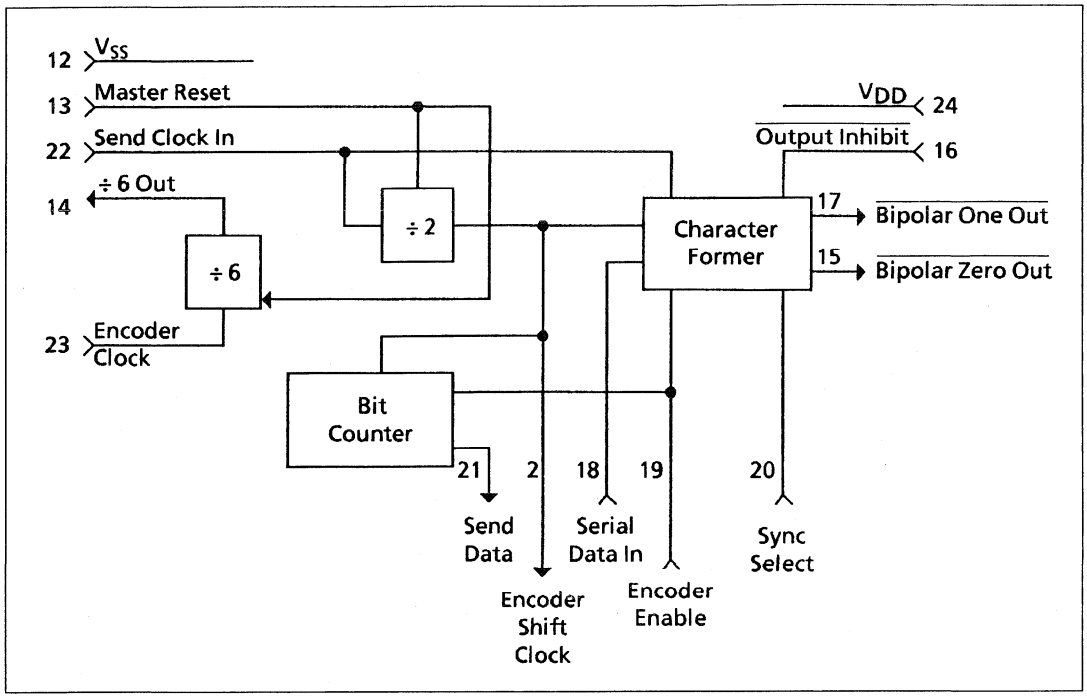


Figure 2: Encoder Block Diagram

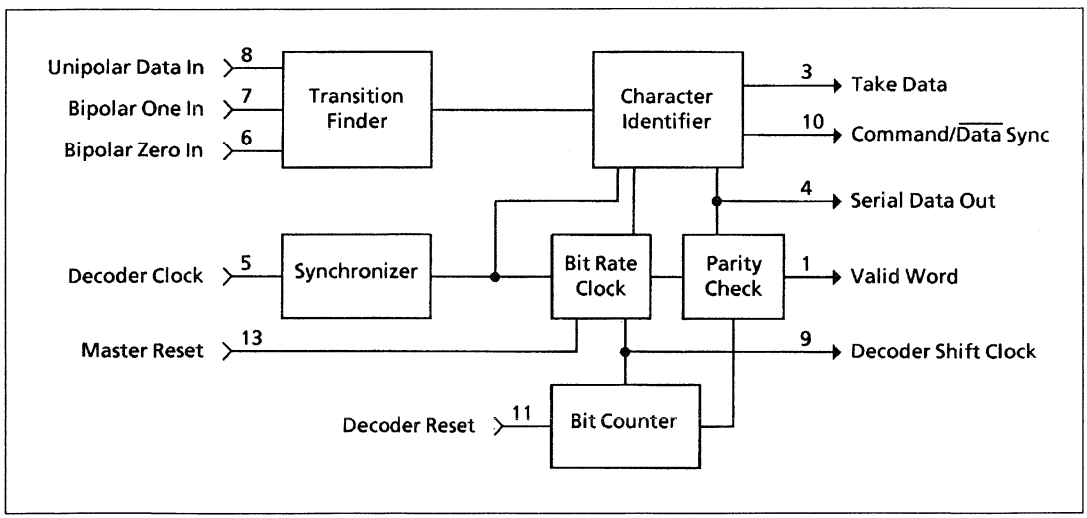


Figure 3: Decoder Block Diagram

PIN DESIGNATIONS

Pin	Input	Output	Enc	Dec	Function	Comment
1		√		√	Valid word	A 'high' signals the receipt of a valid word
2		√	√		Encoder Shift Clock	Shifts data into the encoder on a'low' to 'high' transition
3		√		√	Take Data	'High' during data reception after the sync pulse is identified
4		√		√	Serial Data Out	NRZ output of received data
5	√			√	Decoder Clock	Clock for the transition finder and synchronizer which generates the clock for the rest of the decoder
6	√			√	Bipolar Zero In	Should be 'high' when the bus is in a negative state. Must be tied 'high' when the unipolar input is used
7	√			√	Bipolar One In	Should be 'high' when the bus is in a positive state. Must be tied 'low' when the unipolar input is used
8	√			√	Unipolar Data In	Input for unipolar data to the transition finder. Must be tied 'low' when not in use
9		√		√	Decoder Shift Clock	Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data
10		√		√	Command/$\overline{\text{Data}}$ Sync	This output indicates the type of sychronizing character received as follows: If a data synchronizing character was received, this pin is low while the data is decoded. If a command synchronizing character was received, this pin is high during data decoding
11	√			√	Decoder Reset	A 'high' during a DECODER SHIFT CLOCK rising edge resets the bit counter
12	–	–	√	√	V_{SS}	Ground
13	√		√	√	Master Reset	A 'high' clears the counter in both directions
14		√	√		÷ 6 Out	Provides the ENCODER CLOCK divided by 6
15		√	√		$\overline{\text{Bipolar Zero Out}}$	Provide an active 'low' output to the zero or negative sense of a bipolar line driver
16	√		√		$\overline{\text{Output Inhibit}}$	A 'low' inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive, 'high', states
17		√	√		$\overline{\text{Bipolar One Out}}$	Provides an active 'low' output to the one or positive sense of a bipolar line driver
18	√		√		Serial Data In	Receives serial data at the rate of the ENCODER SHIFT CLOCK
19	√		√		Encoder Enable	A 'high' starts the encode cycle provided that the previous cycle is complete
20	√		√		Sync Select	A 'high' selects the command sync and a 'low' selects the data sync
21		√	√		Send Data	Provides an active 'high' to enable the external serial data source
22	√		√		Send Clock In	Clock input at 2 times the data rate
23	√		√		Encoder Clock	Input to the divide by 6 circuit
24	–	–	√	√	V_{DD}	Positive supply

Figure 4: Pin Designations

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	3	7	V
V_I	Input Voltage	V_{SS}-0.3	V_{DD} +0.3	V
T_A	Operating temperature	–55	125	°C
T_S	Storage temperature	–65	150	°C

Figure 5: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	70%V_{DD}	-	-	V	
V_{IL}	Logic "0" Input Voltage	-	-	30%V_{DD}	V	
V_{IHC}	Logic "1" Input Voltage (clock)	V_{DD}-0.5	-	-	V	
V_{ILC}	Logic "0" Input Voltage (clock)	-	-	V_{SS}+0.5	V	
I_{IL}	Input Leakage Current	-1.0	-	+1.0	µA	$0V \le V_{IN} \le V_{DD}$
V_{OH}	Logic "1" Output Voltage	2.4	-	-	V	I_{OH}=-3mA
V_{OL}	Logic "0" Output Voltage	-	-	0.4	V	I_{OL}=1.8mA
I_{DDSB}	Standby Supply Current	-	0.5	2.0	mA	Outputs Open $V_{IN}=V_{DD}$=5.5V
I_{DDOP}	Operating Supply Current	-	8.0	10.0	mA	V_{DD}=5.5V, f=1MHz
C_{IN}	Input Capacitance	-	5.0	7.0	pF	
C_{OUT}	Output Capacitance	-	8.0	10.0	pF	

1. V_{DD} = 5V ±10%, over full operating temperature range.

Figure 6: DC Characteristics

AC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
f_{EC}	Encoder clock frequency	0	15	MHz
f_{ESC}	Send clock frequency	0	2.5	MHz
t_{ECR}	Encoder clock rise time	-	8	ns
t_{ECF}	Encoder clock fall time	-	8	ns
f_{ED}	Data rate	0	1.25	MHz
t_{MR}	Master reset pulse width	150	-	ns
t_{E1}	Shift clock delay	-	125	ns
t_{E2}	Serial data setup time	75	-	ns
t_{E3}	Serial data hold time	75	-	ns
t_{E4}	Enable setup time	90	-	ns
t_{E5}	Enable pulse width	100	-	ns
t_{E6}	Sync setup time	55	-	ns
t_{E7}	Sync pulse width	150	-	ns
t_{E8}	Send data delay	0	50	ns
t_{E9}	Bipolar output delay	-	130	ns

1. V_{DD} = 5V ±10%, over full operating temperature range.
2. C_L = 50pF

Figure 7: Encoder Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{DC}	Decoder clock frequency	0	-	15	MHz
f_{DCR}	Decoder clock rise time	-	-	8	ns
t_{DCF}	Decoder clock fall time	-	-	8	ns
f_{DD}	Data rate	0	-	1.25	MHz
t_{DR}	Decoder reset pulse width	150	-	-	ns
t_{DRS}	Decoder reset setup time	75	-	-	ns
t_{MR}	Master reset pulse width	150	-	-	ns
t_{D1}	Bipolar data pulse width	t_{DC} + 10	-	-	ns
t_{D2}	Sync transition span	-	$18t_{DC}$	-	ns
t_{D3}	One-Zero overlap	-	-	t_{DC} -10	ns
t_{D4}	Short data transition span	-	$6t_{DC}$	-	ns
t_{D5}	Long data transition span	-	$12t_{DC}$	-	ns
t_{D6}	Sync delay (on)	-20	-	110	ns
t_{D7}	Take data delay (on)	0	-	110	ns
t_{D8}	Serial data out delay	-	-	80	ns
t_{D9}	Sync delay (off)	0	-	110	ns
t_{D10}	Take data delay (off)	0	-	110	ns
t_{D11}	Valid word delay	0	-	110	ns

1. V_{DD} = 5V ±10%, over full operating temperature range.
2. C_L = 50pF
3. t_{DC} = Decoder clock period = $1/f_{DC}$

Figure 8: Decoder Electrical Characteristics

ENCODER OPERATION

The encoder requires a single clock with a frequency of twice the desired rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilised to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK (3) - (4). After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word (5). At any time a low in $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

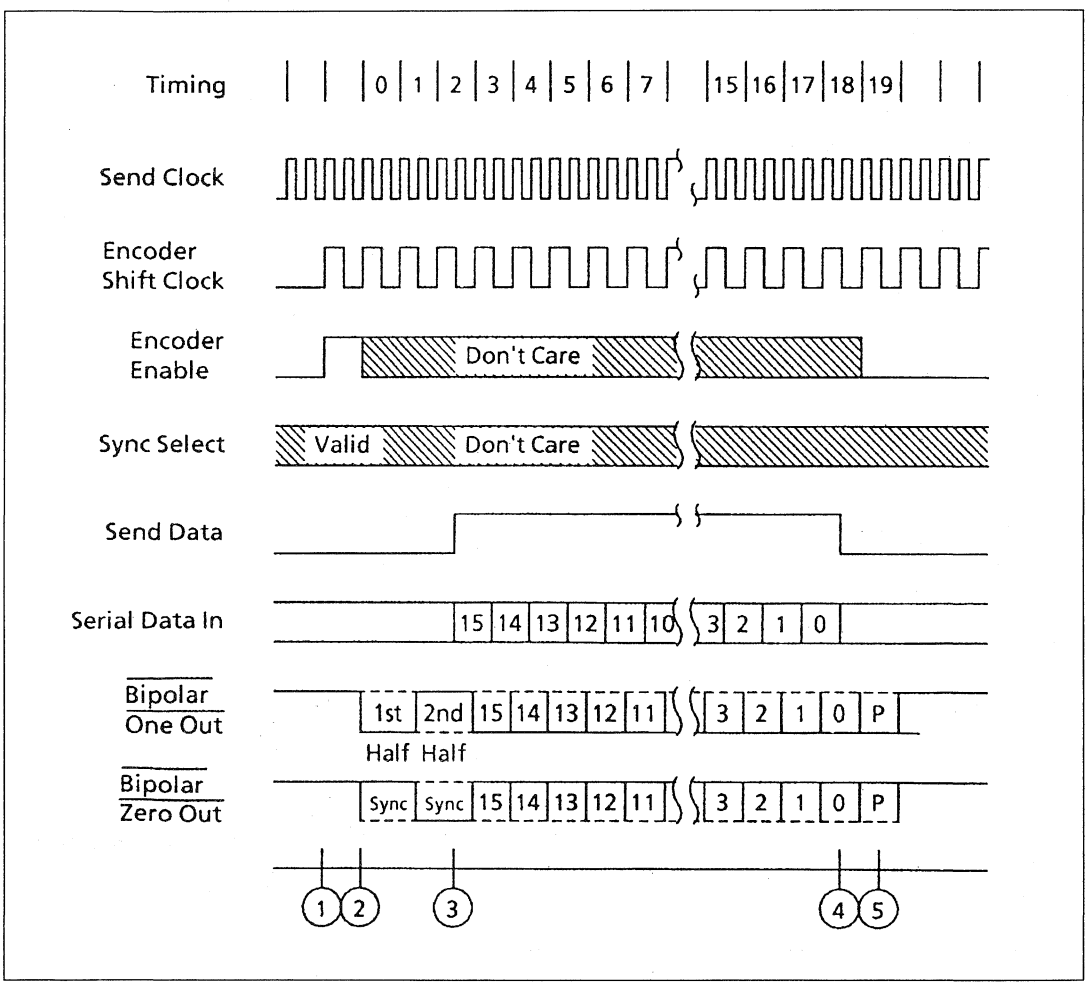


Figure 9: Encoder Operation

DECODER OPERATION

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3) which the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock (2) - (3).

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

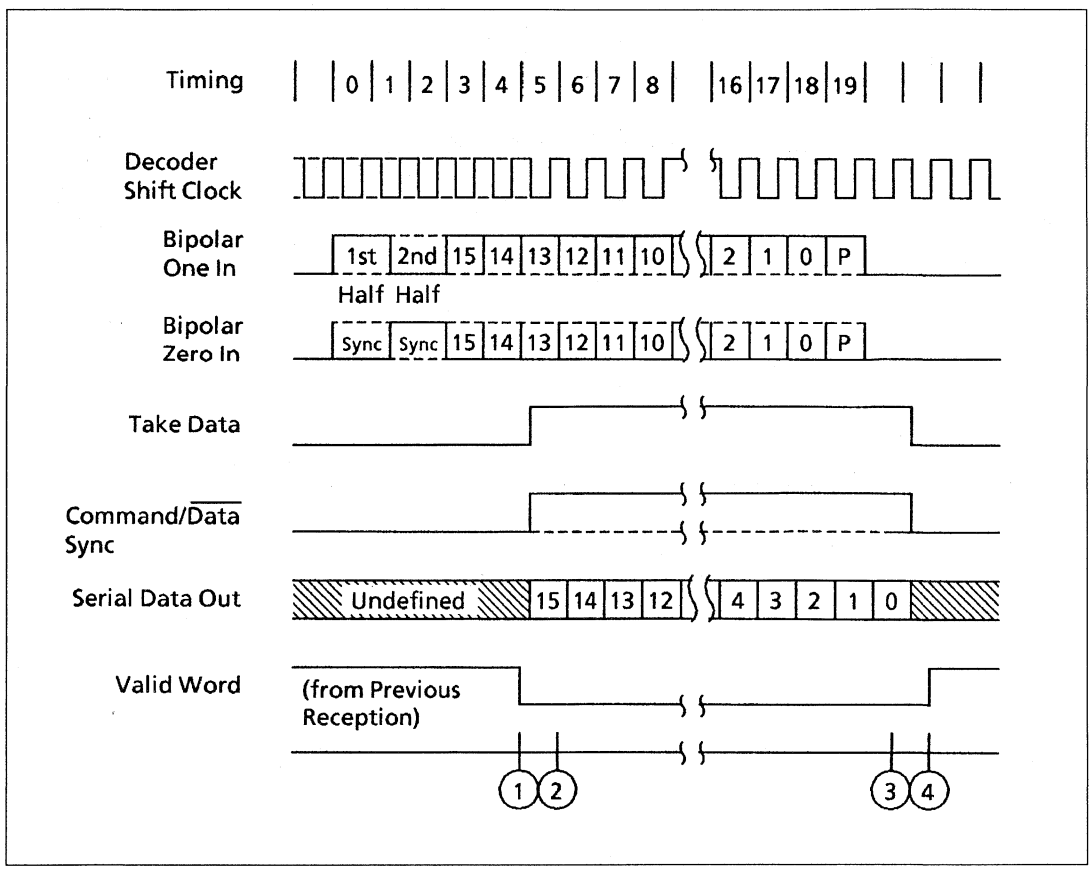


Figure 10: Decoder Operation

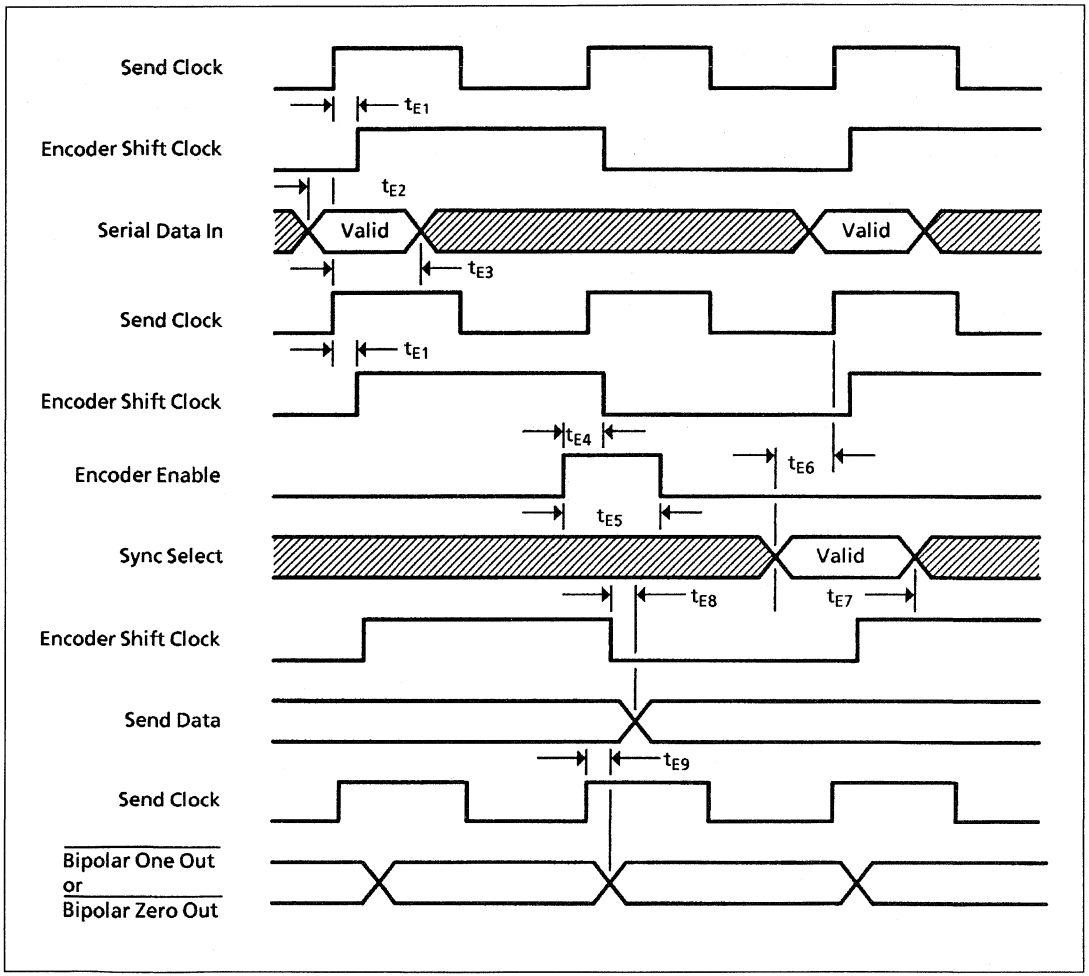
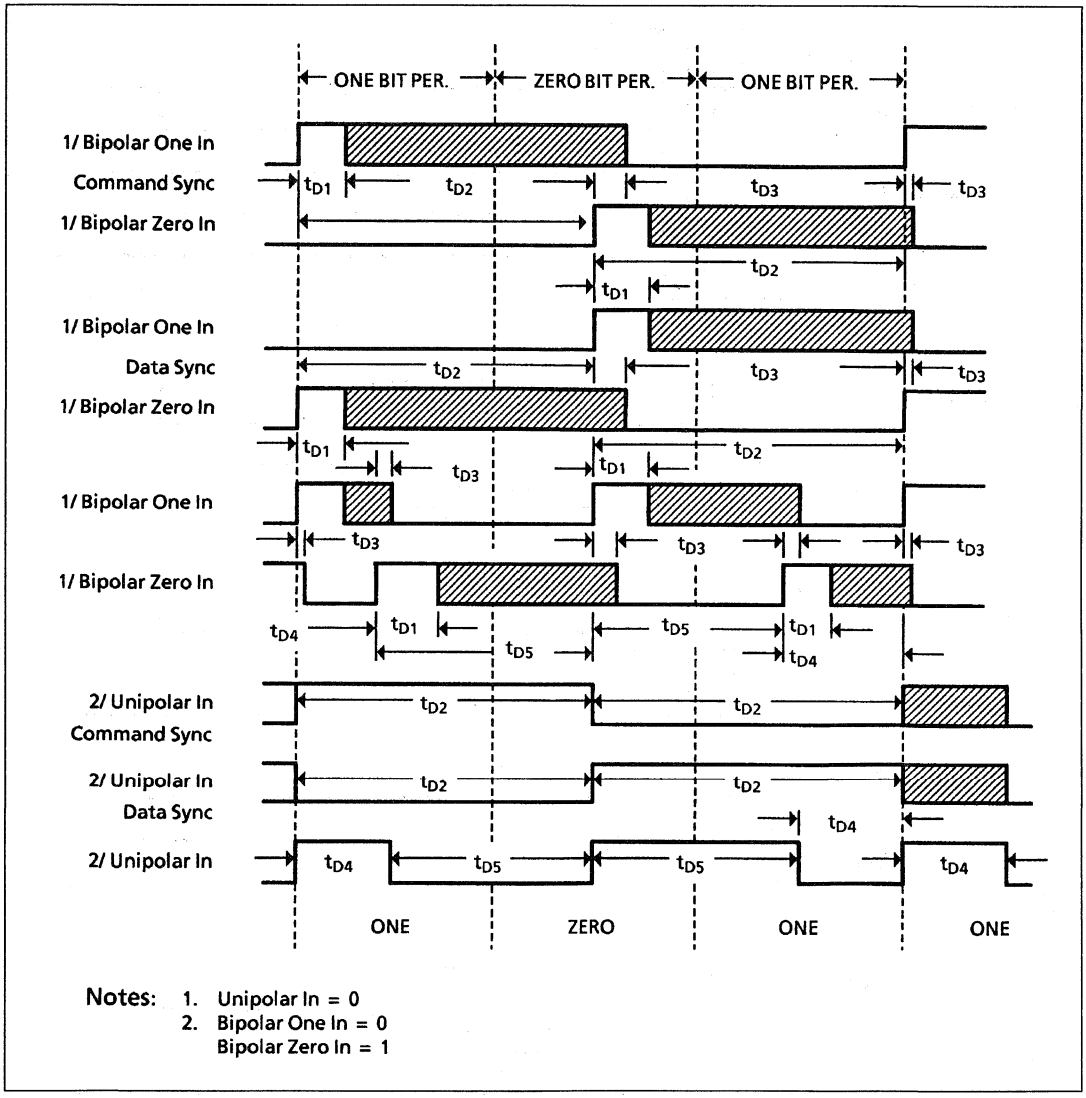


Figure 11: Encoder Timing Diagram



Notes:
1. Unipolar In = 0
2. Bipolar One In = 0
   Bipolar Zero In = 1

Figure 12: Decoder Timing Diagram

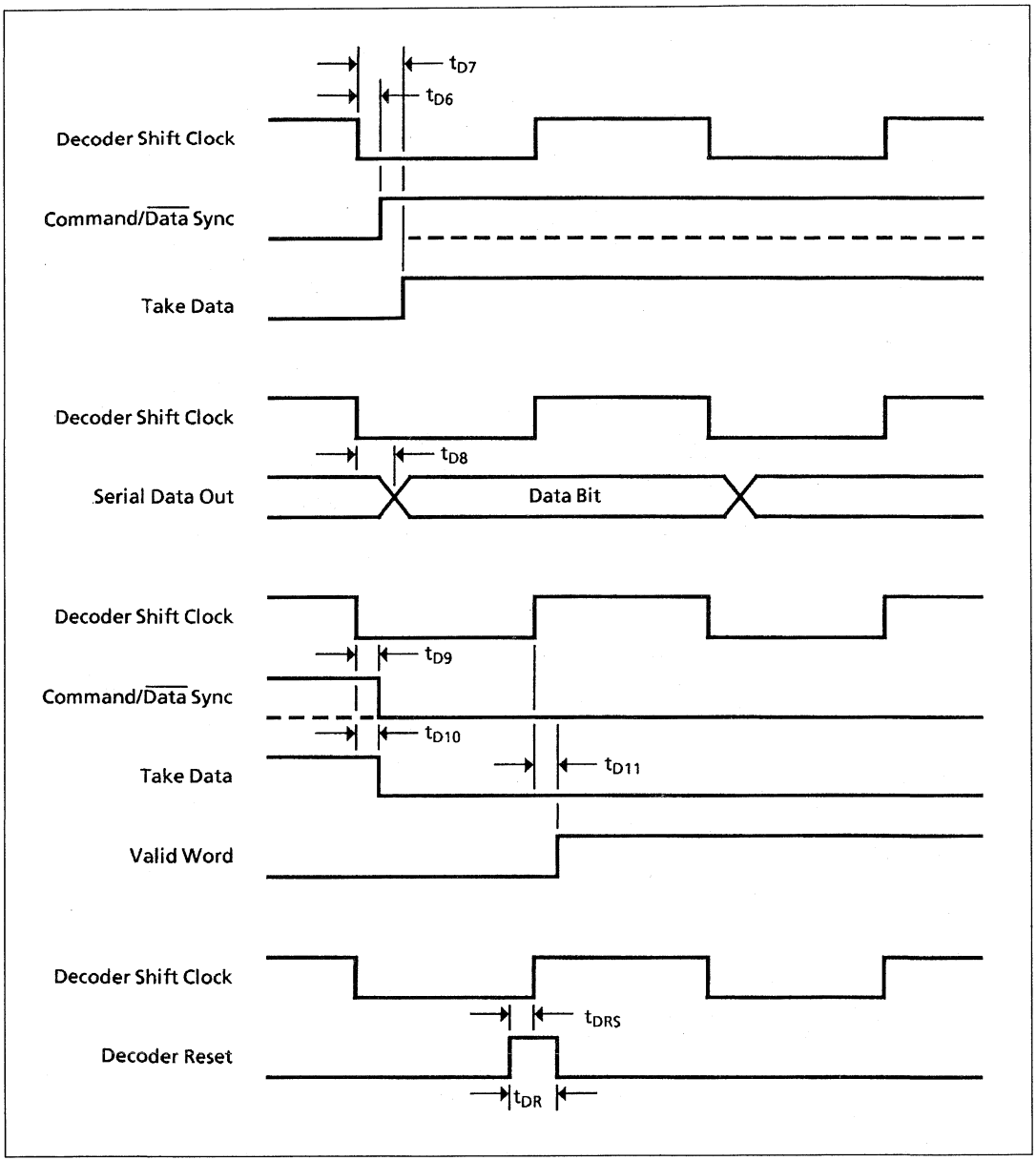


Figure 13: Decoder Timing Details

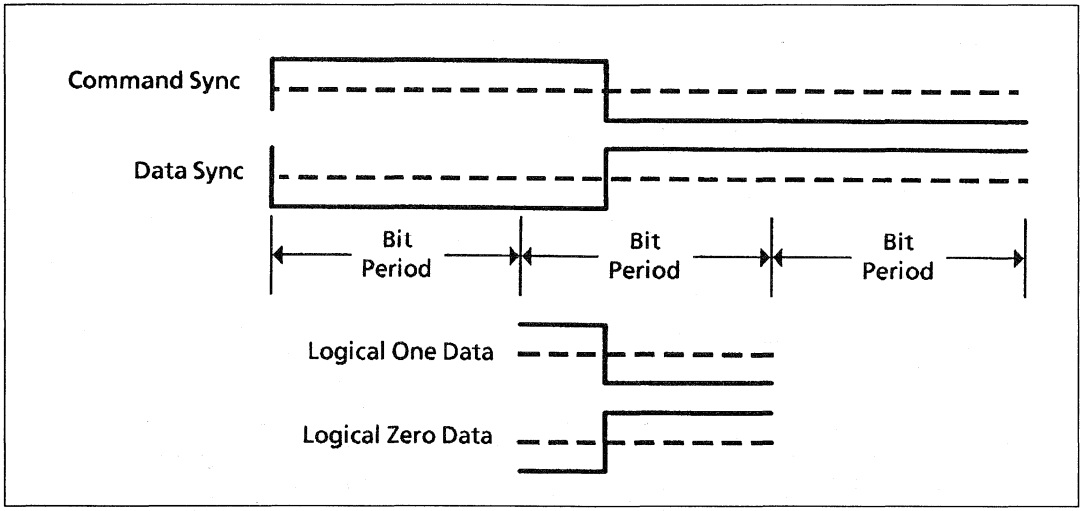


Figure 14: Character Formats

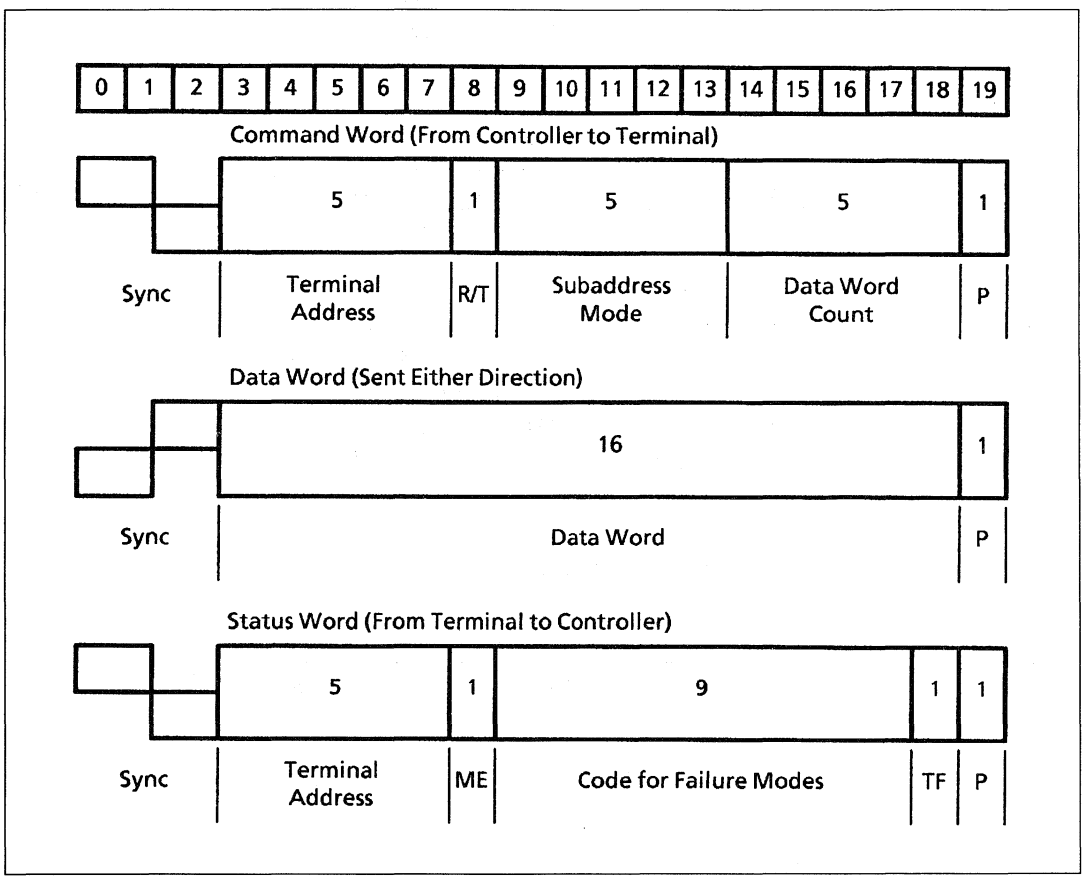
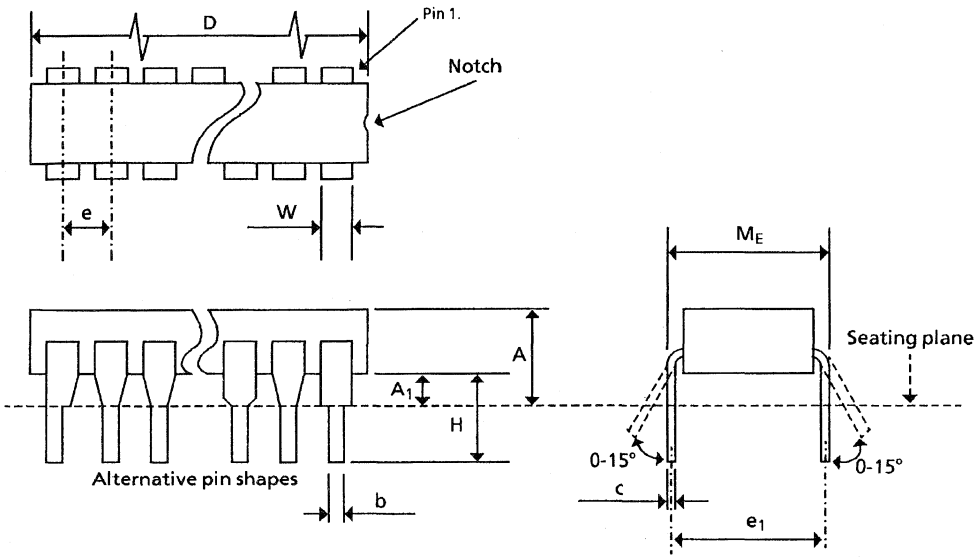


Figure 15: Word Formats

OUTLINES AND PIN ASSIGNMENTS



Ref.	Min.	Nom.	Max.
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.38 (0.015)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54 (0.100) typ	-
e_1	-	15.24 (0.600) typ	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

MEDL XG403

Figure 16: 24-Lead Ceramic DIL (Solder Seal) - Package Style C

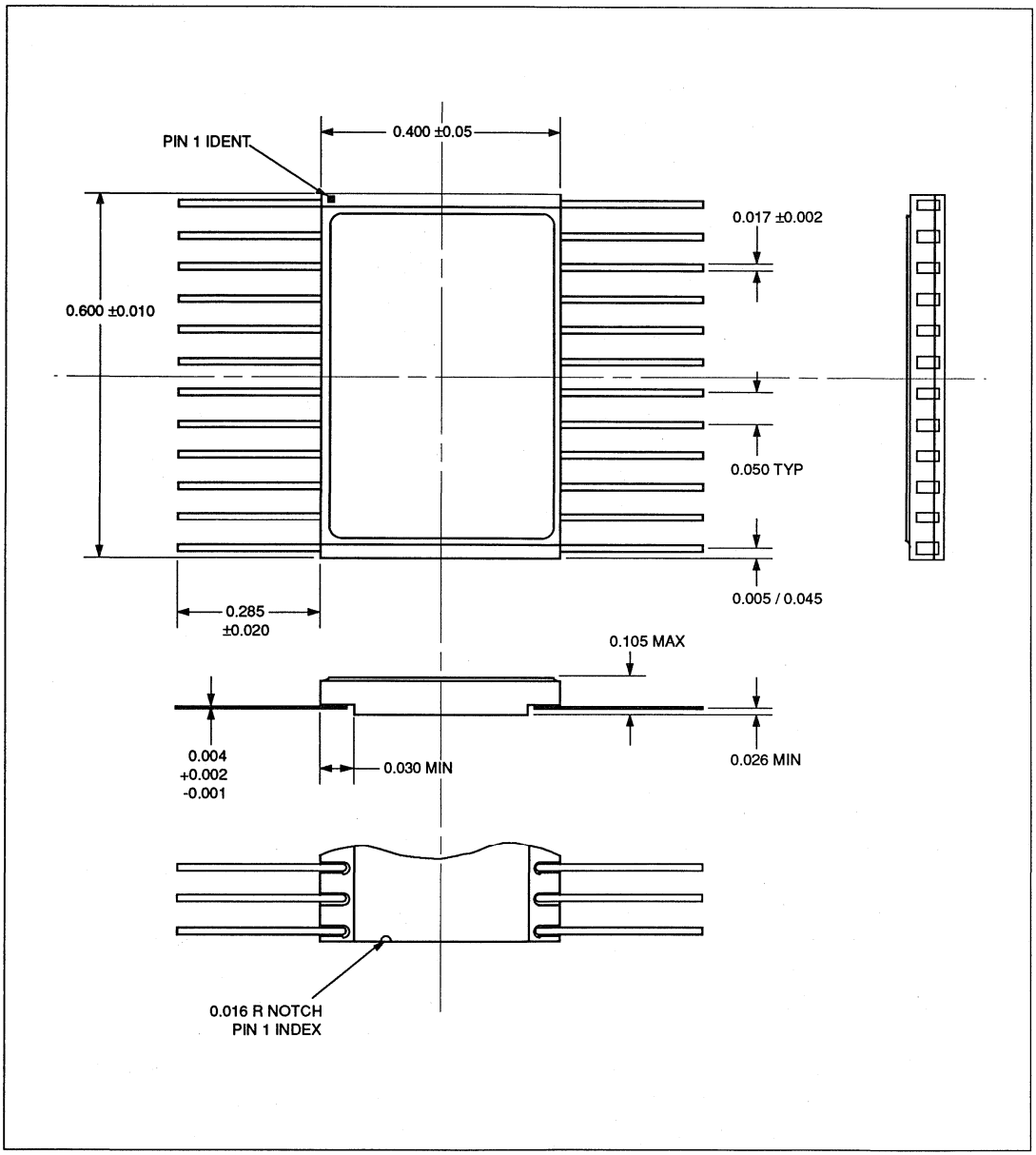


Figure 17: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F

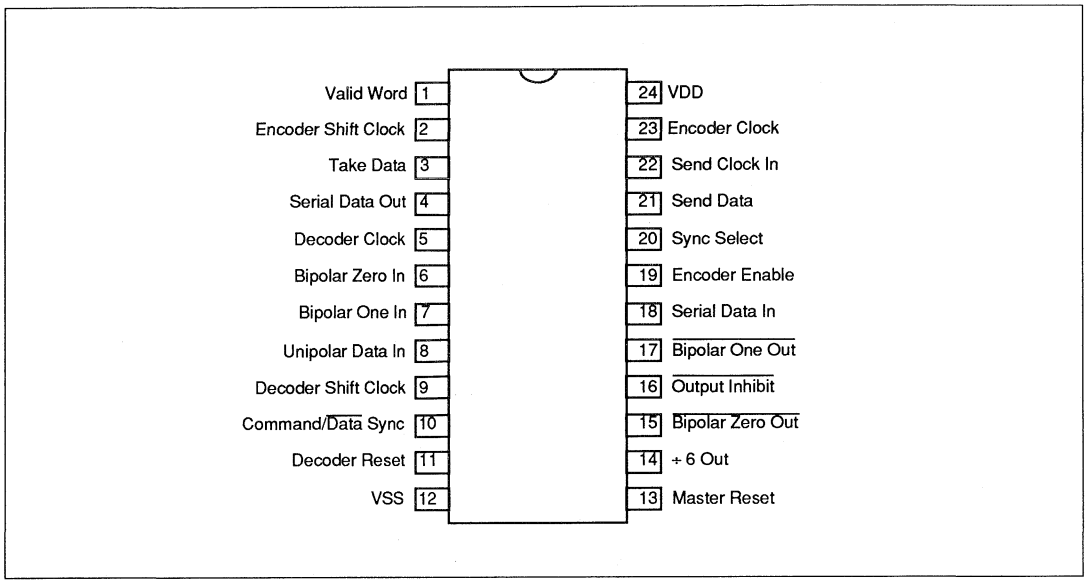


Figure 18: Pin Out - Plug-In

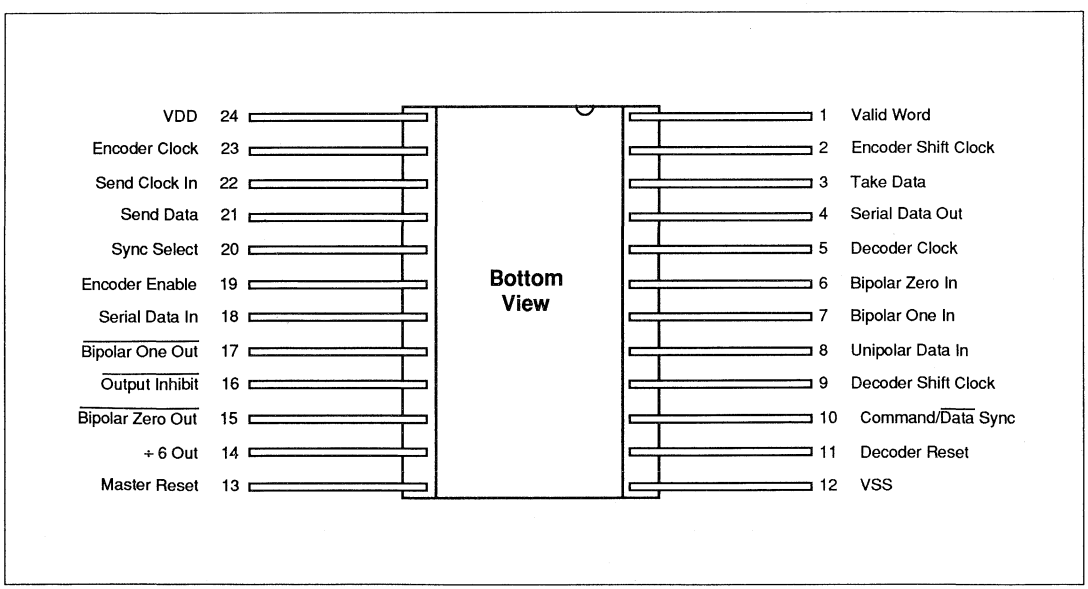
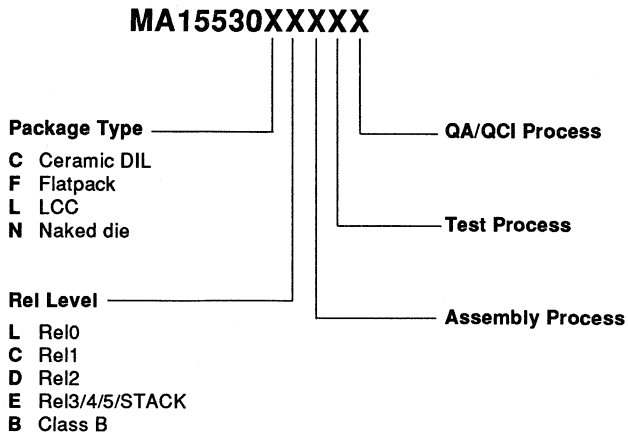


Figure 19: Pin Out - Flatpack

ORDERING INFORMATION



DS3200-1.1 November 1991

CT1555-3/CT1820

DATA TERMINAL BIT PROCESSOR FOR MIL-STD-1553 A & B

GENERAL DESCRIPTION

The CT1555-3/CT1820 Bit Processor Unit (BPU) is an advanced Hybrid Microcircuit that provides the interface between a MIL-STD-1553 Transceiver such as CT3231M or CT3232M, and the subsystem internal parallel data bus. The unit can be employed as the mux bus interface for Remote Subsystems or Master Terminal Bus Controllers, thus providing a common interface for all systems communicating over the bus.

The unit places no restrictions on Command, Response or polling operations as it transfers all Command, Status and Data words from the bus to parallel output lines, together with error information, bus status and handshaking signals. It also contains 5 Bit Address Recognition, Broadcast and Mode Code Decode, Terminal Fail Safe Signal and Self Test.

In the transmit mode, it accepts parallel data from the user and transmits Command, Status and Data words, under subsystem control, to the data bus. Positive handshaking signals provide logic control synchronisation between the unit and the subsystem for direct data flow.

The hybrid is completely compatible with all the electrical and functional spec requirements of MIL-STD-1553 A & B.

FEATURES

- Performs Encoder, Decoder, Logic and Control functions of a Data Bus Terminal to MIL-STD-1553 specifications, including Address, Mode Code and Broadcast Decoding and Terminal Fail Safe
- Flexibility - all control lines accessible
- Parallel tri-state subsystem I/O bus compatible with both 16 bit and 8 bit systems
- Dual rank I/O registers for versatile subsystem timing
- Operates from +5VDC @ 40mA typical (25mA CT1820)
- Self-contained oscillator and clock driver
- Look-ahead serial receive data output
- Self-test, on-line wraparound, plust off-line capability
- Interfaces directly with CT3231M or CT3232M Driver/ Receiver

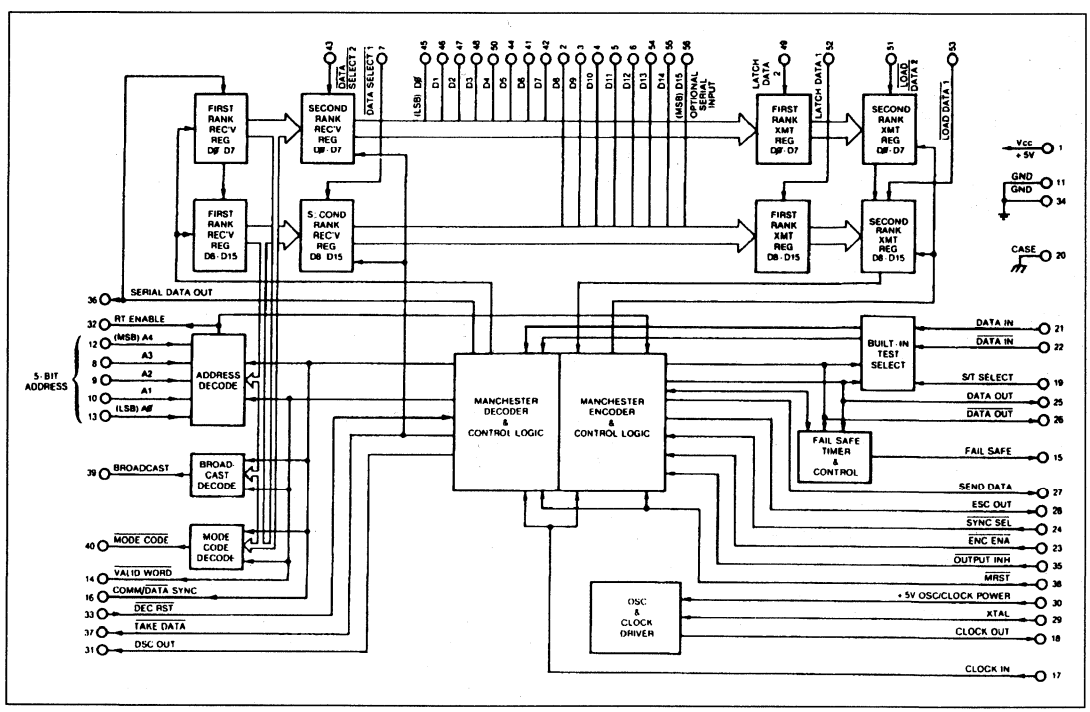


Figure 1: Functional Diagram

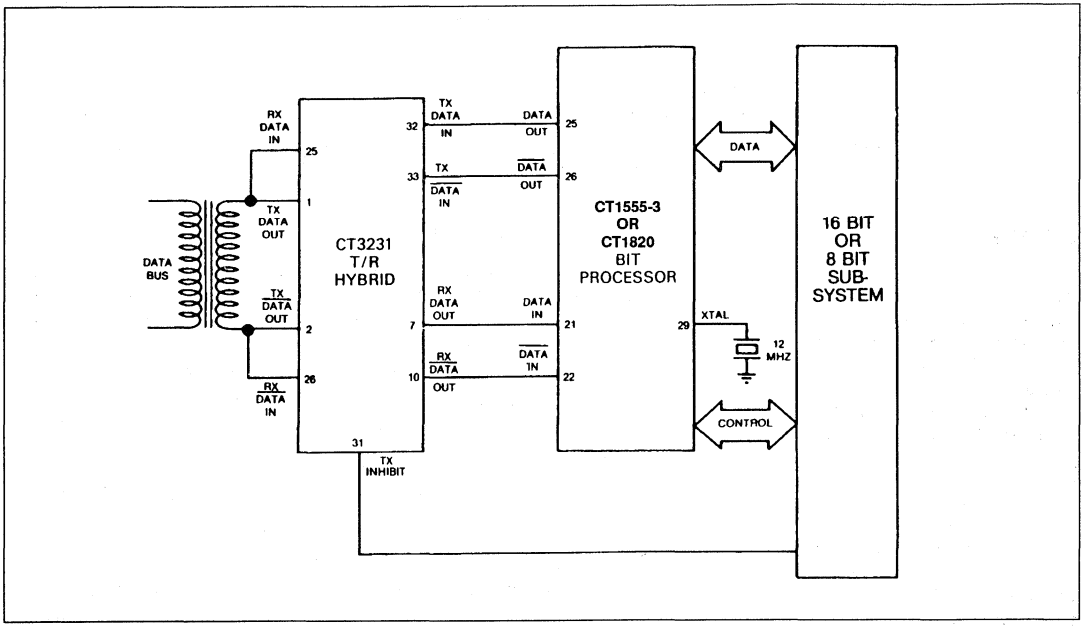


Figure 2: Typical MIL-STD-1553 Data Terminal

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Logic Input Voltage	-0.3 to +5.5V
Logic Input Current	-20 to +4mA
Clock Output Current (PIN 18)	15 mA
Clock In (PIN 17)	-0.3 to V_{CC} +0.3V
Storage Temperature Range	-65 to +150°C
Operating Case Temperature Range	-55 to +125°C

ELECTRICAL CHARACTERISTICS, V_{CC} = 5.0V ±5%

Symbol	Parameter / Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	2.0			V
V_{IL}	Logic "0" Input Voltage			0.7	V
V_{OH}	Logic "1" Output Voltage	See Pin assignments and Loading			
V_{OL}	Logic "0" Output Voltage	See Pin assignments and Loading			
V_{IHC}	Logic "1" Input Voltage (CLOCK)	V_{CC}-0.5			V
V_{ILC}	Logic "0" Input Voltage (CLOCK)			GND+0.5	V
V_{OHC}	Logic "1" Output Voltage (CLOCK)	V_{CC}-0.3			V
V_{OLC}	Logic "0" Output Voltage (CLOCK)			GND+0.3	V
I_{OC}	Logic Supply Current		40		mA
I_{OSC}	Oscillator / Clock Supply Current		8	13	mA

PIN ASSIGNMENTS AND LOADING

In the following table, the symbols are defined as follows:
I_{IH} = maximum input HIGH current with V_{IN} = 2.5 volts
I_{IL} = maximum input LOW current with V_{IN} = 0.4 volts
I_{OH} = maximum output HIGH current for V_{OUT} = 2.5 volts minimum
I_{OL} = maximum output LOW current for V_{OUT} = 0.4 volts maximum

* indicates use of an internal pull-up resistor

		CT1555-3				CT1820				CT1820-2	
Pin No.	Name	I_{IH} (µA)	I_{IL} (µA)	I_{OH} (µA)	I_{OL} (mA)	I_{IH} (µA)	I_{IL} (µA)	I_{OH} (µA)	I_{OL} (mA)	I_{OL} (mA)	Description
1	V_{CC}										+5V Power Input
2	D8	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
3	D9	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕ ↕
4	D10										
5	D11										
6	D12	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
7	$\overline{\text{DATA SELECT 1}}$	20	-0.4								A LOW on this input applies the contents of the SECOND RANK REC'V REG to the D8-D15 I/O pins
8	A3*	-1500	-3.2								Part of 5 Bit ADDRESS INPUT
9	A2*										↕ ↕
10	A1*	-1500	3.2			20	-0.4				Part of 5 Bit ADDRESS INPUT
11	GROUND										Logic and power return
12	A4*	-1500	-3.2			20	-0.4				MSB of 5 Bit ADDRESS INPUT
13	A0*	-1500	-3.2			20	-0.4				LSB of 5 Bit ADDRESS INPUT
14	$\overline{\text{VALID WORD}}$			-400	2.4			-400	4.0	4.0	A LOW on this output indicates receipt of a valid word
15	FAIL SAFE			-400	2.4			-400	4.0	4.0	A HIGH on this output indicates termination of a transmitted message that exceeds 768µs.
16	COMM / $\overline{\text{DATA}}$ SYNC			- 380	2.4			-400	4.0	4.0	A HIGH on this output indicates COMMAND (or STATUS) word reception. A LOW indicates DATA word reception.
17	CLOCK IN	±30	±0.003			100	0.1				Input for 12MHz clock (20pf load). See text for clock requirements.
18	CLOCK OUT			-1000	1.0			-1000	1.0	1.0	Output of OSCILLATOR AND CLOCK DRIVER (see text for description).
19	S / T SELECT	40	-0.8			20	-0.4				A HIGH on this input sets the unit in the self test mode.
20	CASE										CASE CONNECTION
21	DATA IN	20	-0.4			20	-0.4				A HIGH on this input represents a positive state on the bus.
22	$\overline{\text{DATA IN}}$	20	-0.4			20	-0.4				A HIGH on this input represents a negative state on the bus. (Pins 21 and 22 must both be high when the bus is inactive.)
23	$\overline{\text{ENC ENA}}$	20	-0.4			20	-0.4				A LOW on this input initiates a transmit cycle.
24	$\overline{\text{SYNC SEL}}$	20	-0.4			20	-0.4				Actuates COMMAND (or STATUS) sync for an input LOW and DATA sync for an input HIGH.
25	DATA OUT			360	2.4			-400	4.0	4.0	A HIGH on this output produces a positive state on the bus.
26	$\overline{\text{DATA OUT}}$			360	2.4			-400	4.0	4.0	A HIGH on this output produces a negative state on the bus.
27	SEND DATA			380	2.4			-400	4.0	4.0	A HIGH on this output indicates data shifting during the transmit cycle.
28	ESC OUT			1000	1.2			-1000	1.2	1.2	LOW to HIGH transitions on this output during HIGH SEND DATA cause the transmit cycle data shifting to occur.
29	XTAL										A 12MHz (parallel resonant) crystal is connected between this pin and ground.
30	+5V OSC / CLOCK POWER										+5V power for OSCILLATOR AND CLOCK DRIVER.
31	DSC OUT			-1000	1.2			-1000	1.2	1.2	LOW to HIGH transitions on this output during LOW $\overline{\text{TAKE DATA}}$ cause receive cycle data shifting to occur.
32	RT ENABLE			-400	2.4			-400	4.0	4.0	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing the terminal's address. It also resets the FAIL SAFE.

Pin No.	Name	CT1555-3 I_{IH} (µA)	CT1555-3 I_{IL} (µA)	CT1555-3 I_{OH} (µA)	CT1555-3 I_{OL} (mA)	CT1820 I_{IH} (µA)	CT1820 I_{IL} (µA)	CT1820 I_{OH} (µA)	CT1820 I_{OL} (mA)	CT1820-2 I_{OL} (mA)	Description
33	$\overline{\text{DEC RST}}$	20	-0.4			20	-0.4				A LOW on this input (for 1µs minimum) resets the decoder to a condition ready for a new word, resets the COMM / $\overline{\text{DATA}}$ SYNC output LOW, and resets the $\overline{\text{VALID}}$ $\overline{\text{WORD}}$ output HIGH.
34	GROUND										Logic and power return.
35	$\overline{\text{OUTPUT INH}}$	20	-0.4			20	-0.4				A LOW on this input holds output pins 25 and 26 LOW.
36	SERIAL DATA OUT			-400	1.6			-400	4.0	4.0	The received serial data in NRZ format is available at this pin during LOW $\overline{\text{TAKE DATA}}$.
37	$\overline{\text{TAKE DATA}}$			-360	2.4			-400	4.0	4.0	A LOW on this output indicates data shifting during the receive cycle. A LOW to HIGH transition on this pin always transfers the current contents of the FIRST RANK REC'V REG to the SECOND RANK REC'V REG.
38	$\overline{\text{MRST}}$	60	-1.2			20	-0.4				A LOW on this input (for 1µs minimum) interrupts and clears the transmit cycle, resets the FAIL SAFE, and also performs the same functions as $\overline{\text{DEC RST}}$.
39	BROADCAST*			-300	1.6			-400	4.0	4.0	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES in the address field.
40	$\overline{\text{MODE CODE}}$*			-600	2.4			-600	6.0	6.0	A LOW on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES or all ZEROS in the sub-address field.
41	D6	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
42	D7	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
43	$\overline{\text{DATA SELECT 2}}$	20	-0.4			20	-0.4				A LOW on this input applies the contents of the SECOND RANK REC'V REG to the D0 -D7 I/O pins.
44	D5	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
45	D0							↕	↕		LSB of 16 Bit TRI-STATE I/O
46	D1										Part of 16 Bit TRI-STATE I/O
47	D2										Part of 16 Bit TRI-STATE I/O
48	D3	40	-0.4	-1000	2.4			-1000	6.0		Part of 16 Bit TRI-STATE I/O
49	LATCH DATA 2	20	-0.4								A HIGH on this input allows the I/O data on D0-D7 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
50	D4	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
51	$\overline{\text{LOAD DATA 2}}$	60	-1.2								A LOW on this input loads the D0-D7 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
52	LATCH DATA 1	20	-0.4			20	-0.4				A HIGH on this input allows the I/O data on D8-D15 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
53	$\overline{\text{LOAD DATA 1}}$	60	-1.2			20	-0.4				A LOW on this input loads the D8-D15 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
54	D13	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
55	D14	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
56	D15	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	MSB of 16 Bit TRI-STATE I/O and OPTIONAL SERIAL INPUT.

TRANSMIT CYCLE OPERATION

ENCODER SHIFT CLOCK (ESC) (see Figure 3) operates at the data rate (1MHz). A low at ENCODER ENABLE (ENC ENA) during a falling edge of ESC ① starts the Transmit cycle, which lasts for twenty ESC clock periods. The SYNC SELECT (SYNC SEL) input is valid at the next low-to-high transition of ESC ②. A high at SYNC SEL will produce a data sync, or a low will produce a command sync for that word.

Parallel data must be stable at the second rank transmit register before SEND DATA goes high ③. Since ENC ENA is not synchronous with ESC, the minimum time to ③ is 3µsec from ENC ENA leading edge.

The first-rank transmit register may be operated transparently (LATCH DATA always high), or may be used to hold data ready for transmission, independent of the activity on the 16-line subsystem I/O bus. As long as LATCH DATA is held high, data present on the subsystem I/O bus appears at the output of the first rank transmit register. Stable data may be latched and held at the first rank register output by bringing LATCH DATA low. Data to be transmitted may be latched any time before the low-to high transition of SEND DATA (SEND DATA, when appled to the LOAD DATA inputs, locks out the data inputs to the second rank transmit register.) For multiple word transmissions, the next word may be inputted and latched any time after ③, but before the next low to-high transition of SEND DATA.

SEND DATA remains high for 16 ESC periods, during which the parallel transmit data is clocked to the MANCHESTER ENCODER ③ to ④. After the sync and Manchester coded data are transmitted through the DATA OUT and DATA OUT outputs, the ENCODER adds on the parity bit for that word ⑤.

If the transmitted word is to be the last word of the transmission, ENC ENA must go high by ⑤ to prevent initiation of another transmit cycle.

At any time, a low applied to OUTPUT INHIBIT will force both DATA OUT and DATA OUT to a low state without affecting any other operations.

The entire transmit cycle may be interrupted and cleared by applying a minimum of 1µsec negative pulse to the MASTER RESET (MRST) input.

For 8-BIT I/O subsystems, D0 is tied to D8, D1 to D9, etc., through D7 tied to D15, and data is inputted in 8-BIT bytes by using LATCH DATA 1 and LATCH DATA 2 and / or LOAD DATA 1 and LOAD DATA 2 independently.

For serial data applications, D15 input serves as the serial transmit input. With LOAD DATA 1 held low and LATCH DATA 1 held high, D15 input is applied to the ENCODER's serial data input. Inputted data must be at the ESC rate with the MSB starting at the low-to-high transition of SEND DATA.

If a message length ever exceeds 768µsec, the 768µsec TIME OUT (FAIL SAFE) flag goes high, and DATA OUT and DATA OUT are both forced to a low state. This condition will remain until a valid command word (containing the terminal's address) is received or until MRST goes low.

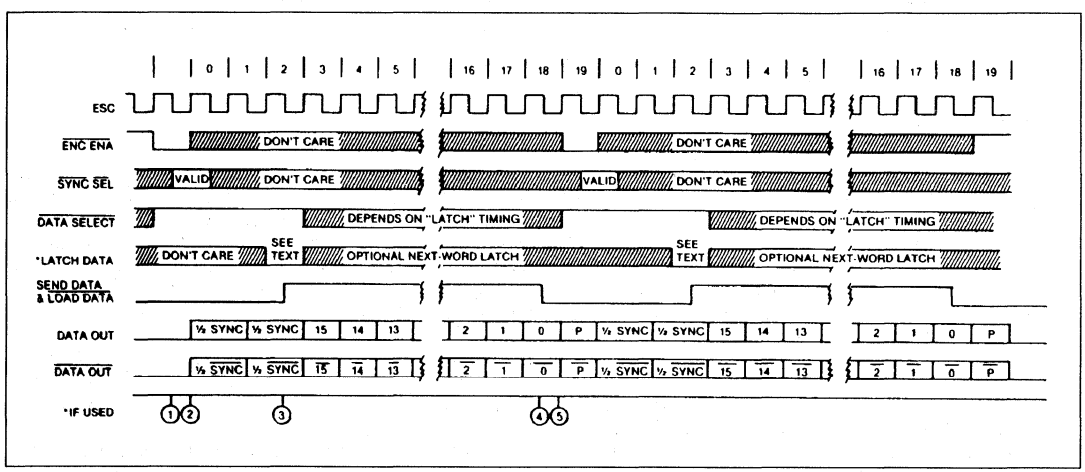
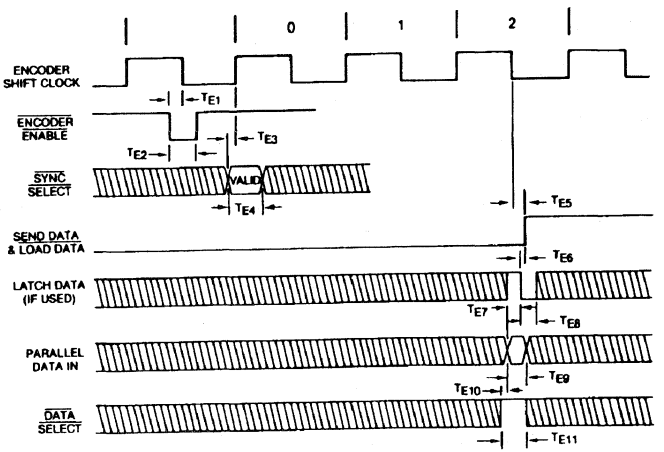


Figure 3: Transmit Cycle Timing



Symbol	Description	Min	Max	Units
T_{E1}	ENCODER ENABLE SET-UP TIME	100		ns
T_{E2}	ENCODER ENABLE PULSE WIDTH	180		ns
T_{E3}	SYNC SELECT SET-UP TIME	190		ns
T_{E4}	SYNC SELECT 'VALID' PULSE WIDTH	150		ns
T_{F5}	SEND DATA DELAY		70	ns
T_{E6}	LATCH DATA HOLD TIME	25		ns
T_{E7}	LATCH DATA SET UP TIME	50		ns
T_{E8}	LATCH DATA PULSE WIDTH LOW	50		ns
T_{E9}	PARALLEL DATA 'VALID' WIDTH	75		ns
T_{E10}	DATA SELECT DISABLE TIME	25		ns
T_{E11}	DATA SELECT PULSE WIDTH HIGH	100		ns

Figure 4: Encoder Timing Detail

RECEIVE CYCLE OPERATION

DECODER SHIFT CLOCK (DSC) (see Figure 5) operates at the data rate (1MHz). When the DECODER recognises a valid sync and two valid Manchester data bits ①, a receive cycle is initiated. The new sync is indicated at the COMMAND/DATA SYNC (C/D SYNC) output and the TAKE DATA output goes low ②. The C/D sync output will remain in its valid state until a new sync is detected on a subsequent word or until DECODER RESET (DEC RST) or MRST goes low. A low at DEC RST or MRST causes C/D SYNC to go low.

TAKE DATA remains low for 16 DSC periods during which time the 16 serial data bits appear at the SERIAL DATA OUTPUT (SDO). This data is simultaneously loaded into the first-rank receive register. The low-to-high transition of TAKE DATA ③ makes the new data available at the output of the second-rank receive register. This data remains available until the next low-to-high transitions of TAKE DATA. It is not reset or cleared by any other signals. This data is applied to the D0 to D15 I/O bus by setting DATA SELECT lines low.

After all data has been loaded into the receive registers, the data is checked for odd parity. A low on VALID WORD (VW) output ④, indicates successful reception of a word without any Manchester or parity errors. For consecutive word receptions, VW will go high again in 3 to 3.5µs. In the absence of succeeding valid syncs, VW will return high in 20µs. A DEC RST (low) at any time will reset VW high.

All decoded commands, including RT ENABLE (address recognition), BROADCAST and MODE CODE are enabled internally by VW and remain valid only as long as VW is low.

For 8-BIT I/O subsystems (D0 tied to D8, through D7 tied to D15), data may be extracted in 8 BIT bytes by selectively activating DATA SELECT 1 and DATA SEL.ECT 2.

For serial data systems, SERIAL DATA OUTPUT is available at the DSC rate from ② to ③.

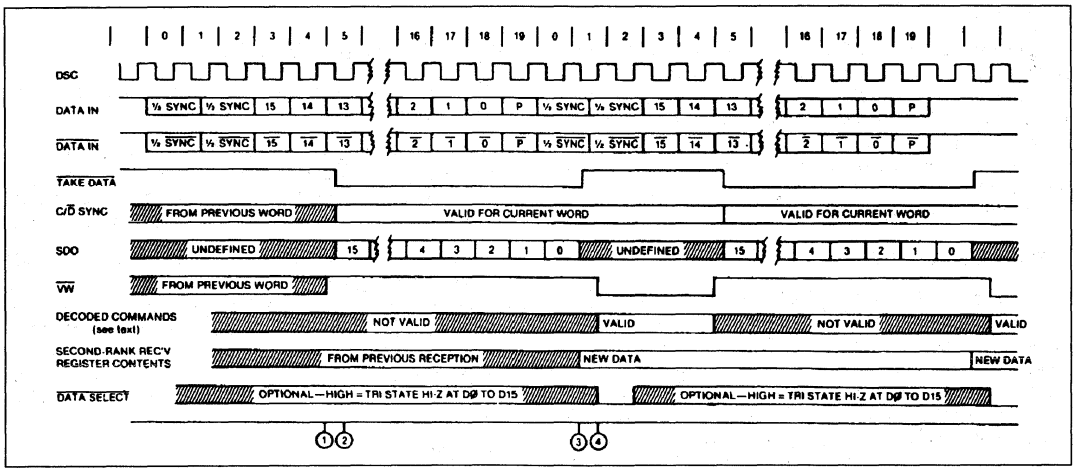
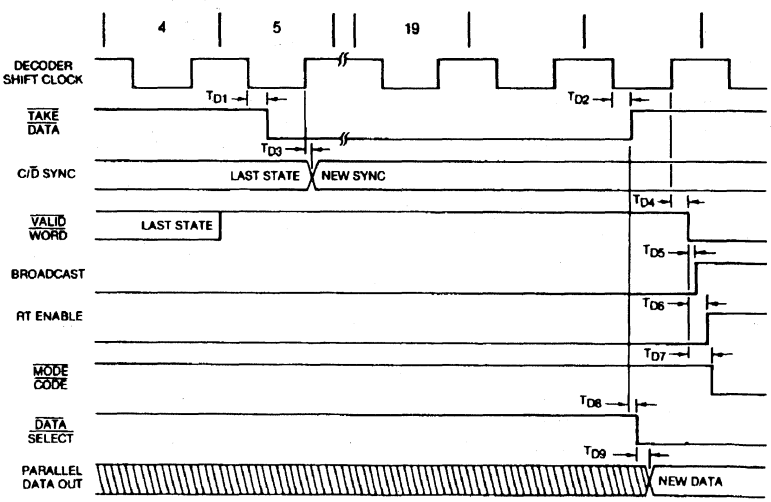


Figure 5: Receive Cycle Timing



Symbol	Description	Min	Max	Units
T_{D1}	TAKE DATA RELAY ON		125	ns
T_{D2}	TAKE DATA DELAY OFF		125	ns
T_{D3}	SYNC DELAY		50	ns
T_{D4}	VALID WORD DELAY		125	ns
T_{D5}	BROADCAST DELAY		70	ns
T_{D6}	RT ENABLE DELAY		100	ns
T_{D7}	MODE CODE DELAY		100	ns
T_{D8}	DATA SELECT INPUT DELAY	0 (Note 1)		ns
T_{D9}	PARALLEL DATA OUTPUT DELAY		50 (Note 2)	ns

Notes: 1. DATA SELECT may be applied at any time that the 16 line I/O is otherwise free.
The parallel DATA OUT, however, is not 'NEWDATA' until 50ns after TAKE DATA goes high.
2. 180ns max for CT1555-3

Figure 6: Decoder Timing Detail

SELF TEST FUNCTION

A high on the S/T SELECT input sets the hybrid in the SELF TEST mode. In this mode, the DATA and $\overline{\text{DATA}}$ output lines are connected to the Decoder inputs so that the unit may operate in the "wraparound" mode without actually going through the data bus transceiver. Note that the DATA and $\overline{\text{DATA}}$ output lines are active in this mode and the S/T SELECT command must also be used to inhibit the data bus transmitter to prevent arbitrary transmission on the data bus.

TERMINAL FAIL SAFE

In order to satisfy the Terminal Fail Safe requirements of MIL-STD-1553B, the DATA and $\overline{\text{DATA}}$ output lines are continuously monitored for length of message. A transmitted message in excess of 768µs sets the FAIL SAFE output high and terminates the transmission by setting both DATA and $\overline{\text{DATA}}$ output lines low. As a redundant safety factor, the FAILSAFE output may be applied to the INHIBIT input of the data bus transmitter (if so equipped). Further transmissions are prevented until the FAIL SAFE flag is reset either by reception of a valid command word containing the terminal address or by a negative pulse on the $\overline{\text{MRST}}$ input. Note: Transmissions containing gaps of 3µs or less are considered continuous, even if the gap is caused by a $\overline{\text{MRST}}$ pulse.

TERMINAL ADDRESS LINES

The five-bit terminal address is set by hard wiring the 5-BIT ADDRESS lines. The hybrid contains internal pull-up resistors so that logic "1" lines may be left open circuited. Logic "0" lines must be grounded.

In operation, RT ENABLE goes high when a valid command word containing the hard-wired address is received. See "RECEIVE CYCLE OPERATION" for timing.

OSCILLATOR AND CLOCK DRIVER

The hybrid may be operated with either the internal clock or an external clock source.

For internal clock operation, a 12MHz parallel-resonant fundamental-mode crystal must be connected from XTAL to ground. Power (+5V) must be applied to +5V OSC/CLOCK POWER and CLOCK OUT must be connected to CLOCK IN.

For external clock operation, no power is applied to +5V OSC/CLOCK POWER and the external clock is applied to CLOCK IN (CLOCK OUT not connected). The external clock must be capable of driving a 20 picofarad load to within 0.5 volts of V_{CC} and within 0.5 volts of ground with rise and fall times of less than 10 nanoseconds. Standard TTL levels are not satisfactory. For a normal 1MHz data rate, the clock frequency must be 12MHz.

FALSE RT ENABLE

Terminals that continuously monitor their own transmissions are subject to "END-AROUND" operation due to a false RT ENABLE. The terminal can erroneously interpret its own status word as a new command word. If no measures are taken to prevent or re-set RT ENABLE, it will remain high for 20µs or until the DECODER recognises a new valid sync (whichever time is shorter).

RT ENABLE may be inhibited by interrupting the RECEIVE CYCLE during a status word transmission. Inverted SEND DATA applied to DEC RST will prevent reception of the status word.

If continuous monitoring is required, RT ENABLE may be reset immediately after it goes high by a 1µs (minimum) low at DEC RST. The status word will then be available at the second-rank receive register.

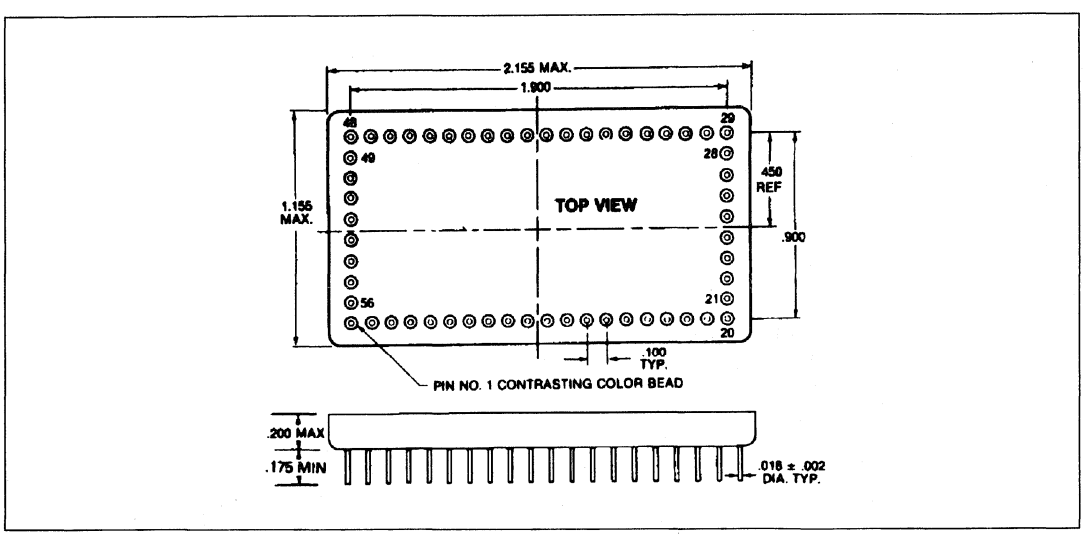


Figure 7: Package Outline

Section 7
Card Products

CT2600

MIL-STD-1773 IBM PC/AT INTERFACE CARD

FEATURES

- Transmits over 2000ft. in point to point configuration
- IBM PC/AT compatible
- Provides electrical isolation for critical interface
- Emulates MCTC MIL-STD-1553B
- Compatible with SMA connectors

GENERAL DESCRIPTION

The CT2600 implements a MIL-STD-1773 fibre optic data bus remote terminal or bus controller which is directly compatible with the IBM PC/AT. The fibre optic interface operates within the first optical transmission window at a peak emission wavelength of 820nm. The MIL-STD-1553B protocol is controlled by the CT1612 and CT1611 hybrids.

INTRODUCTION

The fibre optic driver (CT1750) and receiver (CT1760) are modified existing components. These devices connect to the MIL-STD-1553B Protocol Hybrid (CT1612). The same interface that existed between the CT1612 and the wire transceiver is duplicated, which maintains the low bit/word error rates associated with the existing interface. The protocol hybrid operates in the Bus Controller and Remote Terminal Modes. This function is software controllable via the subsystem interface. All mode codes and error handling capabilities are retained.

The interface between the protocol hybrid and the IBM PC/AT signal set is controlled by the Microprocessor Interface Hybrid (CT611) which is connected to a 4K by 16 bit Dual Port RAM. Block arbitration is utilized to insure that consistent sample sets are maintained from the subsystem side, as well as the 1553 side. All modes of operation, as well as error handling, are contolled by software commands from the IBM interface.

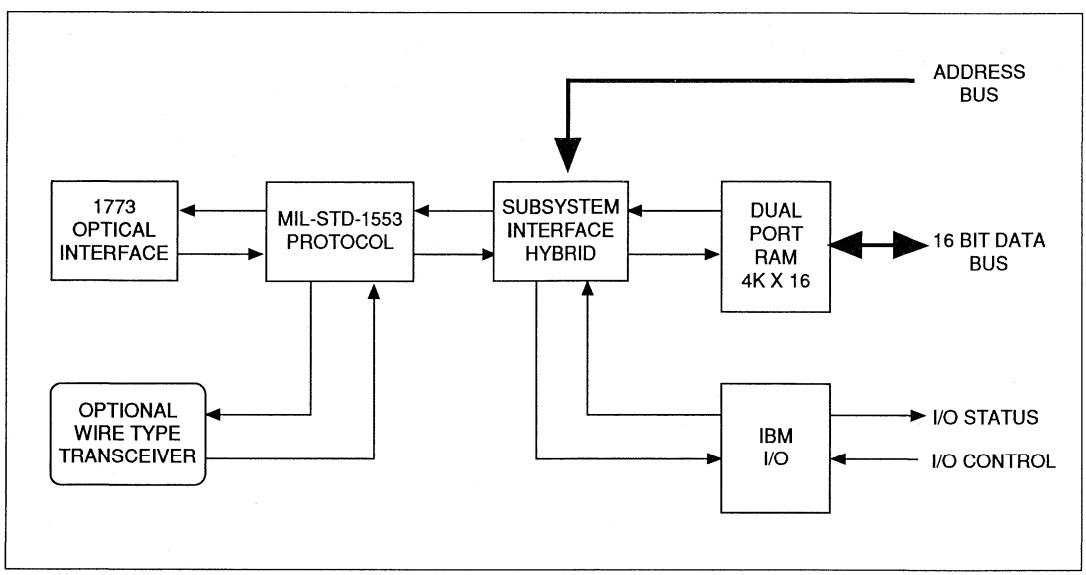


Figure 1: CT2600 Block Diagram

FIBER OPTIC INTERFACE

The fiber optic interface utilized in the implementation of MIL-STD-1773 consists of a hybrid transmitter and receiver. These devices operate in the first optical window with a peak emission wavelength of 820nm. The transmitter directly translates a TTL data signal to optical pulses have a rise and fall time of less than 12 nS at a nominal output power lever of 200 uW. The receiver is capable of accepting data at rates of up to 10 MHz and has a sensitivity of 1 uW.

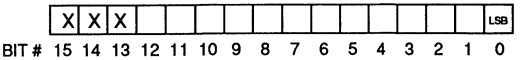
An optical data bus system may be implemented in any of the configurations suggested by MIL-STD-1773. All bus configurations are possible since the CT2600 utilizes separate transmit and receiver optical ports. Detailed specifications of the optical interface and contained in the CT1750/1760 data sheet.

PC/AT - CT2600 INTERFACE

The CT2600 functions as an I/O peripheral on the IBM PC bus. The CT2600 is controlled through simple I/O commands. The PC address locations for these operations are listed in the table below. The word formats needed to program the 1553 interface on the CT2600 are identical to the formats for the CT1611. Detailed operational characteristics may be found in the CT1611 data sheet.

ADDRESS	FUNCTION	READ/WRITE
300_H	Address Word	Write only
302_H	Command Word	Read/Write
304_H	Data Word	Read/Write
306_H	Status Word	Read only
308_H	RT Address Word	Write only

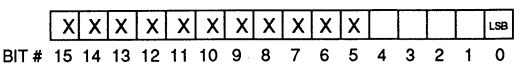
ADDRESS WORD (300_H)



REG BIT	FUNCTION
0-12	Address bits for Data and Command Words

Notes:
1. For Command Word addresses, only bits 0-5 will determine which register will be accessed. Bits 6-12 should be "0".
2. For Data Word addresses, only bits 5-11 will be used to access the dual port RAM. Bits 0-4 are set by an on board counter which resets to 00_H on every address load. This means that an address can be loaded, and then data can be sequentially accessed without re-entering the address. (Bit 12="0")
3. Bit 12 is the hardware reset bit. When this bit = 1, a hardware reset of the 1553 protocol chip will be executed when the address load cycle is complete.

STATUS WORD (306_H)



REG BIT	FUNCTION
0	Interupt #0
1	Interupt #1
2	Interupt #2
3	Interupt #3
4	Command error

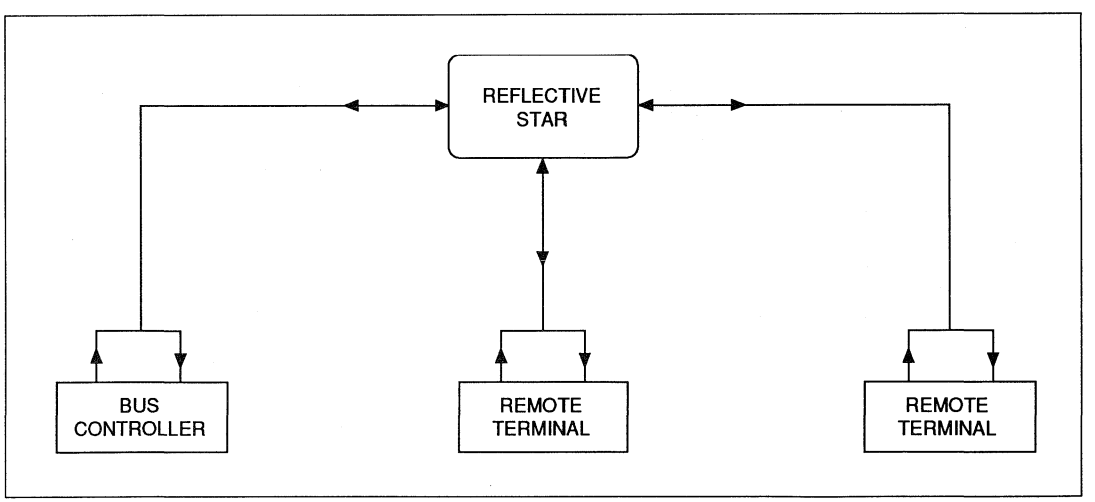
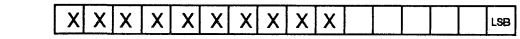


Figure 2: Typical 1773 Configuration: Reflective Star Coupled Bus

RT ADDRESS WORD (308_H)



REG BIT	FUNCTION
0-4	RT address bits
5	RT address parity bit (odd parity only)

OPERATION

Operation of the CT2600 board is made simple through the use of the included subroutines. Read and write operations are simple call routines in the main program. The software routines are written in assembly language and can be called from Quick-Basic (Ver. 4.0 thru 4.5). Also included are several sample main programs written in Basic to operate the board in a Bus Controller mode and a Remote Terminal mode.

Because the CT2600 board contains the CT1611 Subsystem Interface Hybrid, all of the commands and operations of the 1553B bus are controlled through the registers in the hybrid. Enclosed are the basic register descriptions and their addresses. Detailed operation notes not found in this document can be obtained from the CT1611 USERS GUIDE.

Upon power-up, the board automatically assumes a Remote Terminal (RT) configuration with the busy flag set. To change this configuration we must update the registers of the CT2600. This is done by first loading in the RT address into the RT address latch. This must be done even if we are going to operate in the Bus Controller (BC) mode because the Protocol Hybrid constantly checks for a RT address parity error. Since we don't know the state of the RT address latch, we must update it to prevent a RT address parity error. This is shown in the following example:

```
IX2% = &H1              'Load RT address #1
CALL WRRTADR(IX2%)      'Address loaded
                        'No address needs to be loaded
                        'prior to this operation.
```

To access the different registers of the on board CT1611, we must first load the register address into the address latch. This operation is illustrated below:

```
IADDR% = &H0A           'Address &H0A = Operation register
CALL WRADDR(IADDR%)
```

After loading in the address, we can load in the command word into the operation register. The word &H01 in the operation register will place the board in the Bus Controller mode with polling disabled. (See Operation Word table attached)

```
1X1% = &H01
CALL WRCMD(IX1%)        'Write a &H01 in the Operation register
```

We then set up the transaction register for a normal BC to RT transfer with error bits masked. (See Transaction table)

```
IADDR% = &H0C
CALL WRADDR(IADDR%)     'Address &H0C = Transaction register
IX1% = &HFF80
CALL WRCMD(IX1%)        'Write word into Transaction register
```

Now we load in the command word and data words to be transmitted. We will transmit 3 data words to RT terminal #4, sub-address #1.

```
IADDR% = &H0            'Address for Command word register.
CALL WRADDR(IADDR%)
IX1% = &H2023           'Command word for transmit 3 words to
CALL WRCMD(IX1%)        'RT #4 for sub-address #1.

IADDR% = &H420          'Transmit RAM address location for
CALL WRADDR(IADDR%)     'sub-address #1.
IX1% = 1
CALL WRDATA(IX1%)       'Word #1 = 1
IX1% = 4
CALL WRDATA(IX1%)       'Word #2 = 4
IX1% = 7
CALL WRDATA(IX1%)       'Word #3 = 7
```

Now that we are set up, we can trigger the transaction.

```
IX1% = 0
IADDR% = &H2A           'Address for trigger.
CALL WRADDR(IADDR%)
CALL WRCMD(IX1%)        'Message sent.
```

Once the initial set up has been done, we can just loop on the trigger command to send messages quickly. We can periodically update the data to be sent also. Another important point to note is that when we are loading in data, we only need to load the address of the data once. We then can write up to 32 words sequentially. There is a built in address counter which will automatically increment the address with every read or write to RAM. An address load command will reset this counter. This counter applies only to the reading and writing of data. Command word operations do not need this counter.

Sample programs are provided along with the the source code so that anyone can write custom applications for the CT2600.

SUMMARY OF I/O COMMANDS FOR CT1611 1553B INTERFACE (ALL CODES IN HEX)

<table>
<tr><th colspan="2">BUS CONTROLLER I/O</th><th>ADDRESS CODE</th><th>DESCRIPTIONS</th></tr>
<tr><td>(Read or Write)</td><td>Command Word #1</td><td>XX00</td><td>All transfers.</td></tr>
<tr><td>(Read or Write)</td><td>Command Word #2</td><td>XX02</td><td>1. Second command word for RT to RT transfers.
2. Also associated mode data for mode codes such as sync with data.
3. Also used for RTU vector word.</td></tr>
<tr><td>(Read or Write)</td><td>Transaction Word</td><td>XX0C</td><td>Defines type of transfer and Bus selection. Examples
<table>
<tr><th colspan="2">Function</th><th>Data</th></tr>
<tr><td>Normal transfer</td><td>Bus 0
Bus 1</td><td>0000
0008</td></tr>
<tr><td>RT to RT</td><td>Bus 0
Bus 1</td><td>0001
0009</td></tr>
<tr><td>Mode (no data)</td><td>Bus 0
Bus 1</td><td>0003
000B</td></tr>
<tr><td>Mode (returned data)
i.e. vector word,
last cmd, etc.</td><td>Bus 0
Bus 1</td><td>0005
000D</td></tr>
<tr><td>Mode (assorted data)
i.e. sync w/data</td><td>Bus 0
Bus 1</td><td>0007
000F</td></tr>
</table></td></tr>
<tr><td>(Write only)</td><td>Trigger</td><td>XX2A</td><td>Triggers Bus Transaction.
Note: Command word(s) and transaction code must be loaded.</td></tr>
<tr><td>(Read only)</td><td>Status Word 1</td><td>XX3C</td><td>Returned status word for all transactions (first for RT to RT).
Note: This register is preset to FFFF at beginning of transaction and at reset.</td></tr>
<tr><td>(Read only)</td><td>Status Word 2
Returned Mode Data</td><td>XX3A</td><td>Second returned status word for RT to RT transfers, also preset to FFFF. Also returned mode data, such as vector word and last command.</td></tr>
</table>

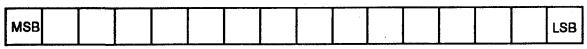
SUMMARY OF I/O COMMANDS (CONTINUED)

RTU I/O	ADDRESS CODE	DESCRIPTION
(Read only) Command Word	XX36	Received command word for all transactions; i.e. transmit, receive* and mode. *Use XX38.
(Read only) Receive Command Word	XX38	Double Buffered version of above for valid receive commands (provides more I/O time).
(Read or Write) Vector Word	XX02	Mode data - to be transmitted - same register as CW #2
(Read only) Sync Word	XX3E	1. Mode data - to be reached 2. Same as returned mode data in BC mode.

Both RTU and BC I/O	ADDRESS CODE	DESCRIPTION
(Write only) Reset 1	XX2E	Resets CT1611 interface only.
(Write only) Reset 2	XX2C	Resets CT1611 and CT1610 front end, will also reset bits in returned status word such as "TF" flag. Same as hard wired master reset used on power up.
(Read or Write) Operation Word	XX0A	Defines BC mode and RTU mode data. FFF0 = RTU FFF1 = BC

COMMAND WORD AT ADDRESS $0A_H$

OPERATION REGISTER



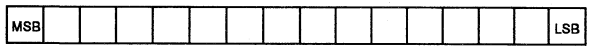
BIT # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1. Power up and reset to busy RTU.
2. Used to define operating mode of 1553 interface for both BC and RTU modes.
3. Select Code = $00101X_{LSB}$ 001010 $XX0A_H$ $\overline{DS} = 0$

REG BIT	NAME	DEFINITION
0	RTBC	Terminal Mode 0 = RTU Mode 1 = BC Mode
1	POE	Poll Operation Enable Enables polling operation in BC Mode. 0 = Not enabled 1 = Enabled
2	CONT POLL	Continuous Poll Operation Enable Causes polling operation to continuously loop when enabled and active 0 = Not enabled (If this bit is reset during an active polling loop, poll will end at completion of polling frame.) 1 = Enabled
3	PFO	Poll Fault Overide When not enabled, poll operation will halt immediately after a transaction failure, (Invalid Transfer Interrupt Generated). Note: Poll can be restarted with last (failed transaction) or next transaction. When enabled, poll will continue even if transaction failed. 0 = Not enabled 1 = Enabled
4	–	Reserved (set to 1).

COMMAND WORD AT ADDRESS $0A_H$

OPERATION REGISTER



BIT # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

REG BIT	NAME	DEFINITION
5,6	TEST	FIFO Loop Tests A. 1553 Side Loop 1) No DMA. B. Subsystem (Microprocessor) Side Loop 1) 1553 Side Set Busy. 2) FIFO exercised via I/O Test Trig Load CMD and I/O Test Trig Unload CMD.
7-9	–	Reserved (set to 1).
10	DBCACC	RTU Dynamic Bus Control Acceptance When set in RTU Mode, RTU will accept bus control request as per MIL-STD-1553B. 0 = Not set 1 = Set
11	SSERR	Set subsystem error flag in returned status word (RTU Mode only).
12	BUSY	Sets busy bit in returned status word, inhibits DMA (RTU Mode only).
13	–	Reserved (set to 1).
14-15	SERVRQ	Sets Service Request in returned status word (RTU Mode only).

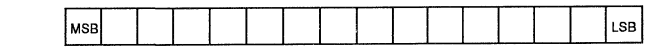
Bit 6	Bit 5	Test
0	0	Reset
0	1	Test A
1	0	Test B
1	1	Not valid

Bit 15	Bit 14	FLAG
0	0	Not set.
0	1	Set until vector word transmitted.
1	0	Set until reset.
1	1	Set until reset*.

*Bit 14 is always reset after vector word is transmitted.

COMMAND WORD AT ADDRESS $0C_H$

TRANSACTION WORD REGISTER



Used only in BC mode. Contains information not explicitly contained in command word.

Defines:

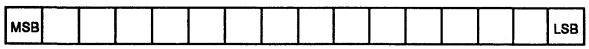
1. Type of transfer.
2. Selection of bus (selects 1 of 4).
   Note: Most systems are only dual redudant.
3. Continue, for continuous poll operation.
4. Conditions for defining an invalid transfer via Bit masks for returned status words.
5. Continue/last control bit for framing poll operations.

This register is loaded via I/O Command. It is also loaded during a Polling Operation, via DMA from the polling command stack.

<table>
<tr><th>REG BIT</th><th>NAME</th><th>DEFINITION</th></tr>
<tr><td>0-2</td><td>TRANS TYPE</td><td>Specifies Transaction Type
<table>
<tr><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Transaction</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Normal receive or transmit.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RT to RT.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Mode without data.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Mode with returned data.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Mode with associated data.</td></tr>
</table>
Note: Codes 010, 100, 110 are reserved.</td></tr>
<tr><td>3-4</td><td>BUS</td><td>Selection of Bus
<table>
<tr><th>Bit 4</th><th>Bit 3</th><th>Bus</th></tr>
<tr><td>0</td><td>0</td><td>“0” or “A”</td></tr>
<tr><td>0</td><td>1</td><td>“1” or “B”</td></tr>
<tr><td>1</td><td>0</td><td>“2” or “C”</td></tr>
<tr><td>1</td><td>1</td><td>“3” or “D”</td></tr>
</table></td></tr>
<tr><td>5</td><td>DMA3RD</td><td>Polling Sequence Option (Polling Mode only)
For use with RT to RT transfers and mode with associated data transfers. When set, during polling sequence the second command word (for RT to RT transfers) or the data word (for mode with associated data transfers) is loaded from the command stack.
Othewise the last entry in the second command and register will be used in transfer.
0 = Not set
1 = Set</td></tr>
</table>

COMMAND WORD AT ADDRESS $0C_H$

TRANSACTION WORD REGISTER

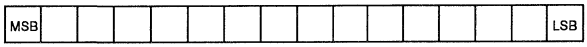


REG BIT	NAME	DEFINITION
6	POLL CONT	Poll Operation Continue (Polling Mode only) When set, polling operation will continue with next command in the command stack. When not set, polling operation will terminate after transaction is complete. Last transfer in polling sequence must have this bit cleared. 0 = Not set 1 = Set
7-15	MASK BITS	Returned Status Word Bit Masks 0 = Not masked 1 = Masked When a non-masked bit in the returned status word(s) is set, the transaction is declared not valid.

Bit	Status Bit Name
7	Terminal Flag
8	Dyanmic Bus Control Acceptance
9	Subsystem Flag
10	Busy Bit*
11	Broadcast Command Received
12	Reserved Bits (any or all of 3)
13	Service Request Bit
14	Instrumentation Bit
15	Message Error Bit

*Note: Setting the Busy Bit mask will not mask a busy response (i.e. declare it valid) when data is not returned in response to a transmit command.

ERROR REGISTER AT ADDRESS 32_H



BIT # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

The Error Register is reset by:
- I/O error reset Command.
- I/O reset command.
- power on reset (master reset).
- initiation of transfer in BC mode.

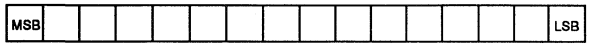
Note: To manually reset the Error Register, write an arbitrary command word to address &H26.

REG BIT	NAME	INDICATION
0*	RTADER	RTU Address Error Parity
1*	PARER	Parity Error in command or data word.
2*	ERROR	1. Any waveform encoding error in received data. 2. Bad Manchester, Parity, or Data Sync. 3. Non contiguity of Data.
3*	LTFAIL	1. Encoding error in terminal's transmission. 2. Includes RT address parity.
4	HSFAIL	Subsystem has not acknowledged DMA request in sufficient time.
5	TXTO	Transfer Time Out error Indicates 1553 transmitter has transmitted in excess of 680 uS (or 1553B maximum of 800 uS) and that terminal fail-safe time-out has turned off the transmitter. This bit will also be set if the terminal time-out hardware fails the self-test mode command (initiate self-test).
6	DMA TO	DMA Time Out Indicates failure in data transfer between CT1611 and subsystem. If DMA takes longer than 80 uS, this flag will be set and DMA will be terminated.
7	DBCACC	Dynamic Bus Control Acceptance Active only in RTU mode. Indicates RTU has accepted bus controller request. RTU must switch to BC mode.

* Additional information for interpretation of register bits 0-3.

Reg Bits				Indication
3	2	1	0	
0	1	0	0	Waveform encoding error (Manchester)
0	1	1	0	Data parity error
1	X	X	1	RTU address error

ERROR REGISTER AT ADDRESS 32_H



BIT # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

REG BIT	NAME	INDICATION
8	TRANS TO	Transaction Time Out Active only in BC mode. Indicates BC transfer has failed due to loop-mouthing RTU or non functioning transceive in BC. Occurs approximately 780 uS after transfer is triggered.
9	GBR	Good Block Received Active only in BC mode. Indicates valid message has been received by BC, will be set even if transaction is otherwise not valid.
10	RMD	Received Mode Data Active only in BC mode. Indicates valid more data has been returned from RT. This bit is set even if transaction is otherwise not valid.
11	BIT SET	Bit(s) Set in returned status word(s) Active only in BC mode. Indicates non masked bits in status word(s) are set. Masked bits are masked in the Transaction Word register. Bits include: Message error bit, Instrumented bit, Service Request, Reserved bit(s) (3 bits), Subsystem Flag, Broadcast Cmd Received bit, Terminal Flag, Busy bit, Dynamic Bus Control Acceptance bit
12	AD ERR	Address in status word(s) Error Active only in BC mode. Indicates RTU address in returned status word(s) is incorrect.
13-14	SW CNT	Returned Status Word Count Active only in BC mode. Two bit non roll-over counter for returned status word(s).
15	BUS ACT ERR	Bus Activity Error Active only in BC mode. This bit is set if the bus is active when it should be quiet following: 1. Returned mode data (indicates word count high). 2. After status in normal receive, mode without data, or non broadcast RT to RT.

Bit 14	Bit 13	Word Count
0	0	None returned
0	1	One returned
1	0	Two returned
1	1	Three or greater returned

RAM ADDRESS LOCATIONS FOR THE ON BOARD DUAL PORT RAM

RECEIVE RAM			
SUBADDRESS	BEGINNING ADDRESS	SUBADDRESS	BEGINNING ADDRESS
0*	&H00	16	&H200
1	&H20	17	&H220
2	&H40	18	&H240
3	&H60	19	&H260
4	&H80	20	&H280
5	&HA0	21	&H2A0
6	&HC0	22	&H2C0
7	&HE0	23	&H2E0
8	&H100	24	&H300
9	&H120	25	&H320
10	&H140	26	&H340
11	&H160	27	&H360
12	&H180	28	&H380
13	&H1A0	29	&H3A0
14	&H1C0	30	&H3C0
15	&H1E0	31*	&H3E0

TRANSMIT RAM			
SUBADDRESS	BEGINNING ADDRESS	SUBADDRESS	BEGINNING ADDRESS
0*	&H400	16	&H600
1	&H420	17	&H620
2	&H440	18	&H640
3	&H460	19	&H660
4	&H480	20	&H680
5	&H4A0	21	&H6A0
6	&H4C0	22	&H6C0
7	&H4E0	23	&H6E0
8	&H500	24	&H700
9	&H520	25	&H720
10	&H540	26	&H740
11	&H560	27	&H760
12	&H580	28	&H780
13	&H5A0	29	&H7A0
14	&H5C0	30	&H7C0
15	&H5E0	31*	&H7E0

*Subaddress not used by 1553 bus, reserved for Mode codes.

POLL PAGE RAM (ADVANCED POLL PAGE MODE OF CT1611)

RAM address: &H800 - &HFFF

```
DECLARE SUB INIT (X%)

        REM ********************************************************
        REM *      SOFTWARE DRIVERS FOR CT2600                     *
        REM *      PC TO 1553 BOARD                                *
        REM *                                                      *
        REM *      WRITTEN BY JOHN LAU         7/8/88              *
        REM *           CIRCUIT TECHNOLOGY INC.                    *
        REM ********************************************************
        REM *      SUBROUTINES USED :                              *
        REM *                                                      *
        REM * WRADDR(IX1%) = WRITES AN ADDRESS WORD IN             *
        REM * WRCMD(IX1%)  = WRITES A COMMAND WORD IN              *
        REM * RDCMD(IX1%)  = READS A COMMAND WORD OUT              *
        REM * WRDATA(IX1%) = WRITES A DATA WORD IN                *
        REM * RDDATA(IX1%) = READS A DATA WORD OUT               *
        REM * RDSTAT(IX1%) = READS A STATUS WORD OUT            *
        REM * WRRTADR(IX1%) = WRITES RT ADDRESS                 *
        REM *                                                    *
        REM * DSCRN1(IX)  = PUTS UP INITIAL SCREEN               *
        REM * DECWD(IX,ARRY(),ADDR) = DECODES A WORD INTO AN ARRAY*
        REM * INIT (X%) = INITIALIZATION SUBROUTINE             *
        REM ********************************************************

        REM ********************************************************
        REM *                                                      *
        REM *     THIS PROGRAM WILL OPERATE THE CT2600 IN          *
        REM *     THE BUS CONTROLLER MODE                          *
        REM *                                        2/10/89 JL    *
        REM ********************************************************

        DIM WD%(15)
        COLOR 7, 1                      `WHITE LETTERS ON BLUE BACKGROUND
        CLS
        IADDR% = 0
        CALL DSCRN1(IADDR%)

        GOTO 900
        CALL INIT(X%)
        INPUT X$


900     IX2% = &H1                      `LOADS IN AN ARBITRARY VALID
        CALL WRRTADR(IX2%)              `ADDRESS


1000    IADDR% = &H2C                   `WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             `RESET TRIGGER II
        IX2% = &H1
        CALL WRCMD(IX2%)                `RESET OPERATION FOR FRONT END

        IADDR% = &H2E                   `WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             `RESET TRIGGER I
        IX2% = &H1
        CALL WRCMD(IX2%)                `RESET OPERATION FOR SUBSYSTEM


1010    IADDR% = &HA                    `WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             `OPERATION REGISTER
        IX2% = &H1
        CALL WRCMD(IX2%)                `SETS UP FOR BC OPERATION
        IX2% = &HFFFF
1015    CALL RDCMD(IX2%)                `READS THE OPERATION REGISTER
        CALL DECWD(IX2%, WD%())         `DISPLAYS THE CONTENTS OF REG.
```

Listing 1: Bus Controller Mode Program

```
                                                    'VERIFY THE STATUS OF CT2600
        LOCATE 6, 2: PRINT ''OPERA WORD =>''; IX2%
        IF IX2% <> 1 THEN GOTO 1010
        LOCATE 6, 40: INPUT ''STOPPED  HIT <CR> TO CONTINUE'', X$

1020    IADDR% = &HC                        'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)                 'TRANSACTION REGISTER
        IX2% = &HFF80
        CALL WRCMD(IX2%)                    'SETS UP FOR BC TO RT OPERATION
        IX2% = &H0
        CALL RDCMD(IX2%)                    'READS THE TRANSACTION REGISTER
        CALL DECWD(IX2%, WD%())             'DISPLAYS THE CONTENTS OF REG.
                                            'VERIFY THE STATUS OF CT2600
        LOCATE 6, 2: PRINT ''TRANS WORD => ''; IX2%
        IF IX2% <> &HFF80 THEN GOTO 1020
        LOCATE 6, 40: INPUT ''STOPPED  HIT <CR> TO CONTINUE'', X$

1030    IADDR% = &H0                        'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)                 'COMMAND WD REGISTER
        IX2% = &H2021
        CALL WRCMD(IX2%)                    'SETS UP FOR TRANSFER
        IX2% = &H0
        CALL RDCMD(IX2%)                    'READS THE COMMAND WD REGISTER
        CALL DECWD(IX2%, WD%())             'DISPLAYS THE CONTENTS OF REG.
                                            'VERIFY THE STATUS
        LOCATE 6, 2: PRINT ''COMMAND WORD =>''; IX2%
        LOCATE 6, 40: INPUT ''STOPPED  HIT <CR> TO CONTINUE'', X$
        LOCATE 21, 40: PRINT ''TRANSMIT TO RT ADDRESS => 4''

        REM ****************************************************
        REM *  BUS CONTROLLER MODE INITIALIZATION COMPLETE     *
        REM ****************************************************

        IADDR% = &H420                      'ADDRESS FOR DATA SUBADDRESS 1
        CALL WRADDR(IADDR%)
        IX2% = &H745                        'WRITE A WORD INTO RAM
        CALL WRDATA(IX2%)
        LOCATE 6, 40: PRINT ''DATA WRITTEN INTO BUFFER IS =>''; IX2%

        IADDR% = &H420                      'ADDRESS FOR DATA SUBADDRESS 1
        CALL WRADDR(IADDR%)
        IX2% = &H0                          'READ A WORD FROM RAM
        CALL RDDATA(IX2%)
        LOCATE 7, 40: PRINT ''DATA READ IS =>''; IX2%
        INPUT '' PAUSE'', X$



1050    IX2% = 0
        IADDR% = &H2A                       'ADDRESS FOR TRIGGER TRANSACTION
        CALL WRADDR(IADDR%)
        CALL WRCMD(IX2%)                    'TRIGGERS TRANSACTION

1100    IX2% = 0
        CALL RDSTAT(IX2%)                   'SCAN ROUTINE TO VALIDATE
        CALL DECWD(IX2%, WD%())             'TRANSMISSION
        LOCATE 6, 2
        PRINT ''STATUS WORD   ''

        ZXSTAT% = IX2% AND &H1F             'READ INTERRUPT STATUS
        IF ZXSTAT% <> &H1 THEN
                LOCATE 9, 40
                PRINT ''MESSAGE BAD   ''
                BEEP
```

Listing 1: Bus Controller Mode Program (continued)

```
        GOTO 1050
END IF

LOCATE 9, 40
PRINT ``MESSAGE OK       ``
IF INKEY$ = ``E'' OR INKEY$ = ``e'' THEN
        LOCATE 12, 40
        PRINT ``                                    ``
        LOCATE 13, 40
        PRINT ``                                    ``

        LOCATE 12, 40
        INPUT ``ENTER NEW SUBADDRESS =>'', ISUBADR%
        IX2% = &H2001
        IX2% = IX2% + (ISUBADR% * 32)
        IADDR% = &H0                    `WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             `COMMAND WD REGISTER
        CALL WRCMD(IX2%)                `SETS UP FOR TRANSFER

        LOCATE 13, 40
        INPUT ``ENTER NEW DATA =>'', IX1%
        IADDR% = &H400
        IADDR% = IADDR% + (ISUBADR% * 32)
        CALL WRADDR(IADDR%)
        CALL WRDATA(IX1%)
        LOCATE 7, 40
        PRINT ``DATA SENT =>''; IX1%; ``        ``
END IF

GOTO 1050                               `LOOP BACK

STOP

SUB INIT (X%) STATIC
FOR I = 6 TO 23
LOCATE I, 2
PRINT STRING$(78, 32)
NEXT I
LOCATE 7, 4
INPUT ``ENTER RT ADDRESS =>'', IX1%
CALL WRRTADR(IX1%)

IADDR% = &H2C


END SUB
```

Listing 1: Bus Controller Mode Program (continued)

```
        REM ******************************************************
        REM *      SOFTWARE DRIVERS FOR CT2600                   *
        REM *      PC TO 1553 BOARD                              *
        REM *                                                    *
        REM *      WRITTEN BY JOHN LAU         7/8/88            *
        REM *          CIRCUIT TECHNOLOGY INC.                   *
        REM ******************************************************
        REM *      SUBROUTINES USED :                            *
        REM *                                                    *
        REM * WRADDR(IX1%) = WRITES AN ADDRESS WORD IN           *
        REM * WRCMD(IX1%)  = WRITES A COMMAND WORD IN            *
        REM * RDCMD(IX1%)  = READS A COMMAND WORD OUT            *
        REM * WRDATA(IX1%) = WRITES A DATA WORD IN              *
        REM * RDDATA(IX1%) = READS A DATA WORD OUT              *
        REM * RDSTAT(IX1%) = READS A STATUS WORD OUT           *
        REM * WRRTADR(IX1%) = WRITES THE RT ADDRESS            *
        REM *                                                  *
        REM * DSCRN1(IX)  = PUTS UP INITIAL SCREEN             *
        REM * DECWD(IX,ARRY(),ADDR) = DECODES A WORD INTO AN ARRAY*
        REM ******************************************************

        REM ******************************************************
        REM *                                                    *
        REM *     THIS PROGRAM WILL OPERATE THE CT2600 IN        *
        REM *             REMOTE TERMINAL MODE                   *
        REM *                                       10/13/88 JL  *
        REM ******************************************************

        DIM WD%(15)
        COLOR 7, 1                      'WHITE LETTERS ON BLUE BACKGROUND
        CLS
        IADDR% = 0
        CALL DSCRN1(IADDR%)

        IX2% = &H4                      'RT TERMINAL ADDRESS = 4
        CALL WRRTADR(IX2%)

1000    IADDR% = &H2C                   'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             'RESET TRIGGER II
        IX2% = &H1
        CALL WRCMD(IX2%)                'RESET OPERATION FOR FRONT END
        IADDR% = &H2E                   'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             'RESET TRIGGER I
        IX2% = &H1
        CALL WRCMD(IX2%)                'RESET OPERATION FOR SUBSYSTEM

1010    IADDR% = &HA                    'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             'OPERATION REGISTER
        IX2% = &H1000
        CALL WRCMD(IX2%)                'SETS UP FOR RT OPERATION
        IX2% = &HFFFF
        CALL RDCMD(IX2%)                'READS THE OPERATION REGISTER
        CALL DECWD(IX2%, WD%())         'DISPLAYS THE CONTENTS OF REG.
                                        'VERIFY THE STATUS OF CT2600
        LOCATE 6, 2: PRINT ``OPERA WORD =>''; IX2%
        LOCATE 6, 40: INPUT ``STOPPED  HIT <CR> TO CONTINUE'', X$

1030    IADDR% = &HA                    'WRITES THE ADDRESS FOR THE
        CALL WRADDR(IADDR%)             'OPERATION REGISTER
        IX2% = &H0
        CALL WRCMD(IX2%)                'SETS UP FOR NOT BUSY RT OPERATION
        IX2% = &HFFFF
        CALL RDCMD(IX2%)                'READS THE OPERATION REGISTER
```

Listing 2: Remote Terminal Mode Program

```
        CALL DECWD(IX2%, WD%())          'DISPLAYS THE CONTENTS OF REG.
                                         'VERIFY THE STATUS OF CT2600
        LOCATE 6, 2: PRINT ``OPERA WORD =>''; IX2%
        LOCATE 6, 40: INPUT ``STOPPED  HIT <CR> TO CONTINUE'', X$

        REM ********************************************************
        REM * INITIALIZATION FOR RT MODE COMPLETE                  *
        REM ********************************************************
        K = 1
1100    IX2% = 0
        FOR J = 1 TO 2000
        CALL RDSTAT(IX2%)                'NO ADDRESS NEEDED

        IX3% = IX2% AND 1

        IF INKEY$ = ``Q'' THEN
                BEEP
                STOP
        END IF

        IF IX3% = 1 THEN
                GOTO 1150
                ELSE GOTO 1120
        END IF
1120    NEXT J
        GOTO 1100

1150    IADDR% = &H38                    'ADDRESS FOR COMMAND REGISTER
        CALL WRADDR(IADDR%)
        CALL RDCMD(IX2%)                 'READ COMMAND REGISTER
        ZXCMD% = IX2%                    'STORE COMMAND WORD
        CALL DECWD(IX2%, WD%())
        LOCATE 6, 2
        PRINT ``RCVD CMD WORD  ``

        ZXWDS% = IX2% AND &H1F           'DECODE WORD COUNT
        LOCATE 10, 40
        PRINT ``# WORDS =>''; ZXWDS%     'PRINT WORD COUNT

        ZXSUB% = IX2% AND &H3E0          'DECODE SUBADDRESS
        ZXSUB% = (ZXSUB% / 32)
        LOCATE 9, 40
        PRINT ``SUBADDRESS =>'', ZXSUB%;  'PRINT THE SUBADDRESS LOCATION

        IADDR% = ZXSUB% * 32             'ADDRESS FOR RECEIVE BLOCK RAM
                                         'AT SUBADDRESS 1
        CALL WRADDR(IADDR%)
        IX2% = 0
        CALL RDDATA(IX2%)
        LOCATE 7, 40
        PRINT ``DATA #1 =>''; IX2%
        GOTO 1100                        'LOOP BACK AND SCAN AGAIN
        STOP
```

Listing 2: Remote Terminal Mode Program (continued)

ADVANCE DATA
DS3081-1.3 October 1991

CT2605

MIL-STD-1553 TO MIL-STD-1773 TRANSPARENT GATEWAY BOARD

FEATURES

- MIL-STD-1553 to 1773 Interface
- Bidirectional Converter
- Transparent Gateway
- Minimal signal delay through converter
- Compatible with 1553A and B
- Uses SMA fibre optic Connectors for easy serviceability
- 1 Mb/s Through Put Rate Standard
- Ruggedised version available, please consult Customer Services

GENERAL DESCRIPTION

The CT2605 is a board level product that will transmit and receive MIL-STD-1553 electrical signals and convert them to 1773 compatible fibre optic signals. It is designed to introduce minimal delay in the retransmission of signals and, unlike other bus extenders which use additional start and stop bits for the fibre optic signal, can be used singularly to provide a gateway or in pairs to extend a 1553 stub hundreds of feet. The fibre optic driver and receiver operate at a 835nm wavelength typically and use 100/140um fibre with SMA type connectors. The board is 5 x 6 inches and has four mounting holes so that the user can put it into the desired enclosure. Connection points are provided on the board for the power requirements of ±12V and +5V DC.

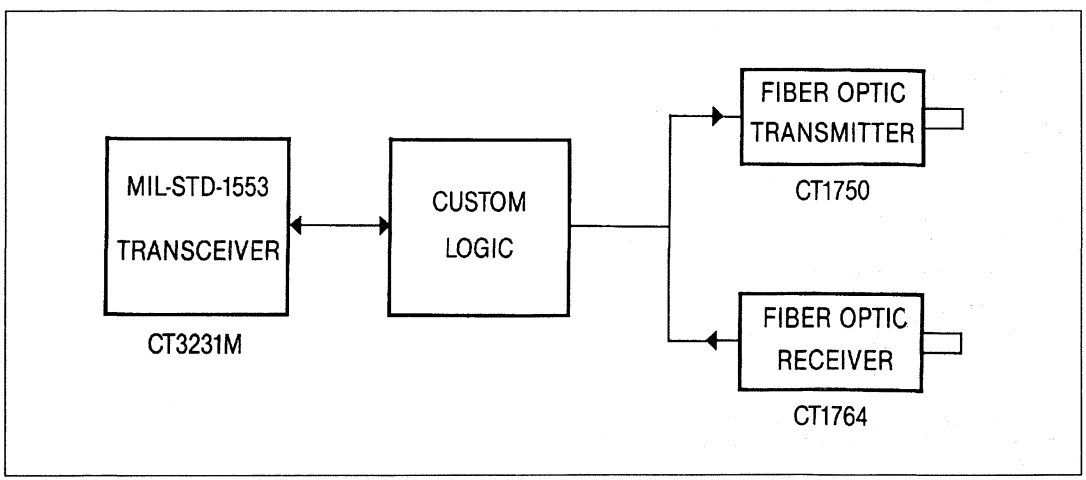


Figure 1: Functional Diagram - CT2605

APPLICATIONS EXAMPLES

AVIONICS TESTING

On aircraft production lines, the technician is often faced with having to position his MIL-STD-1553 Data Bus Tester a great distance from the aircraft, where reflections on his cables can cast uncertainty over his test results. Inserting the CT2605 can extend a stub length hundreds of feet, allowing the test equipment to be placed at a remote location if desired.

ENGINEERING FACILITIES

In many cases during the developmental phase of a program, one MIL-STD-1553 Data Bus is being shared by people on different floors or in labs that are far apart. Here are two potential problems that can be avoided by using the CT2605:

1) TEMPEST - government contractors are forced to pay strict attention to security leaks. All fiber optic cabling systems are immune to such leaks.

2) The physical limit of the MIL-STD-1553 Data Bus when shielded twisted pair cable is used. In this case the CT2605 can extend the length of the data bus hundred of feet, allowing it to be extended vertically or horizontally within a building.

ELECTRICAL CHARACTERISTICS

POWER SUPPLY CURRENT (MAX)			
CONDITIONS	+5V	+12V	−12V
STANDBY	200mA	50mA	85mA
@25% DUTY CYCLE			
Transceiver Receiving Fiber Optic Transmitting	215mA	50mA	85mA
Transceiver Transmitting, Fiber Optic Receiving	200mA	75mA	120mA

PROPAGATIONAL DELAYS (TYP)	
Electrical Transceiver Receiving To Fiber Optic Output (t_1)	250nS
Fiber Optic Input to Electrical Transceiver Output (t_2)	500nS
Total Delay Using Two Boards To Convert Electrical To Fiber and Back to Electrical MIL-STD-1553 Signal	750nS

For further information concerning individual components consult CT3231M, CT1750 & CT1764 Data Sheets.

FIBRE OPTICS			
PARAMETER	MIN	MAX	UNIT
Peak Output Signal	200	-	µW
Optical Input Power	1	150	µW

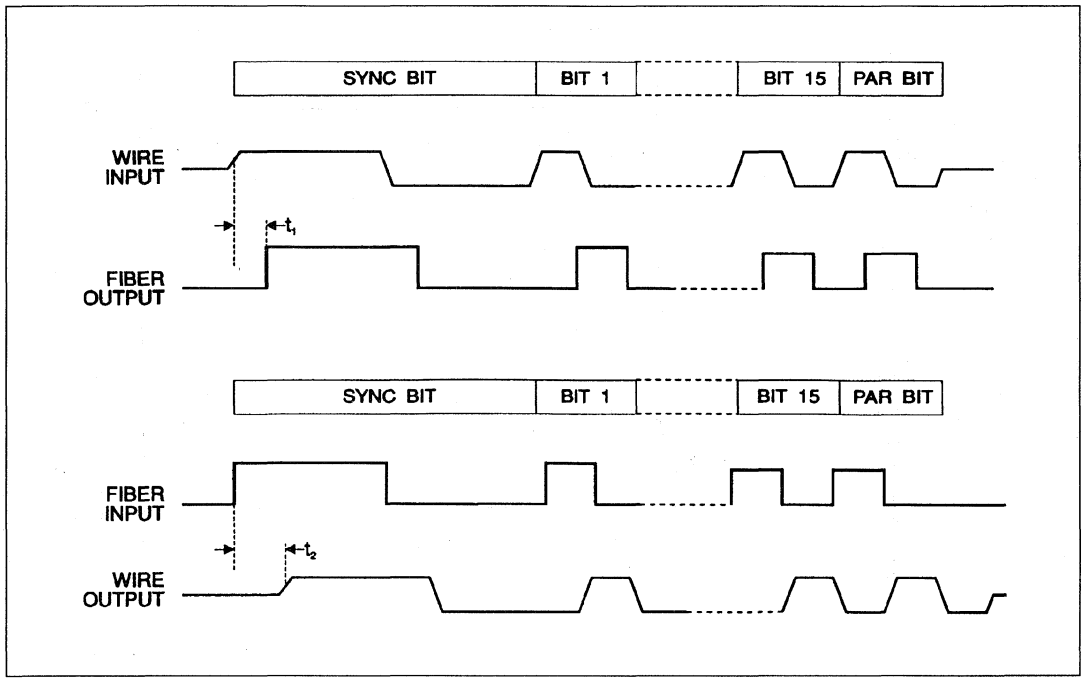


Figure 2: Timing Diagram - CT2605

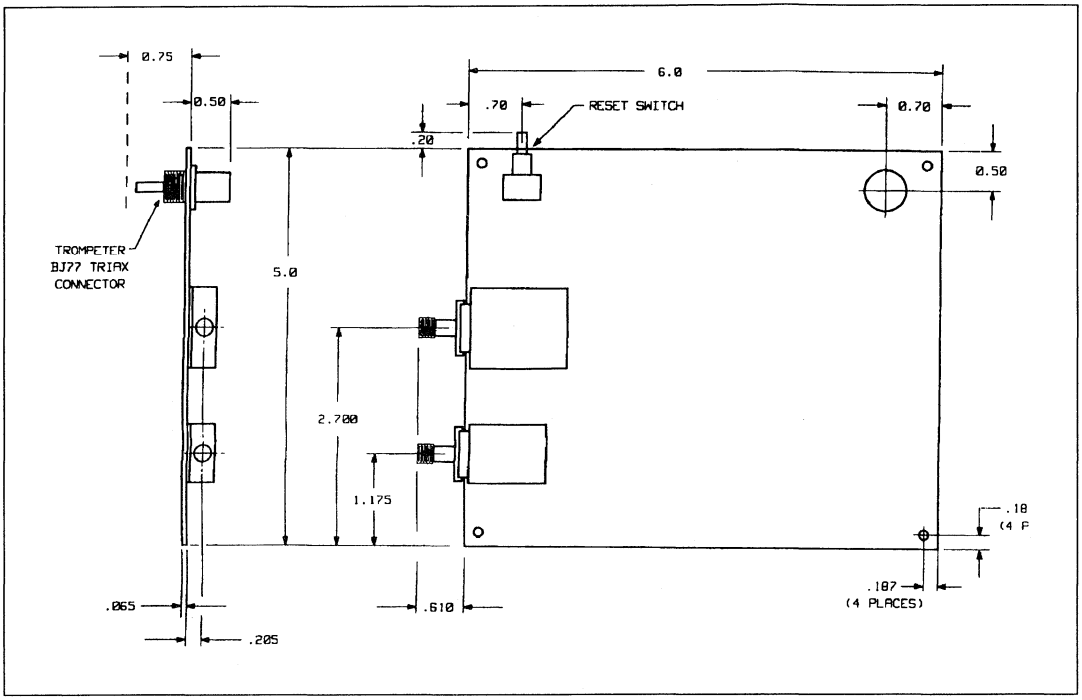


Figure 3: Mechanical Outline Drawing - CT2605
(Militarized versions available, please consult Customer Services.)

Section 8

Mil-Std-1397

3082-1.3 October 1991

CT1698

MIL-STD-1397 TYPE E 10MHZ LOW LEVEL SERIAL INTERFACE

FEATURES

- Optional transformer isolation
- Internally set threshold
- Matched to 50 ohm system impedance power on and off
- Operates with ±5 volt supplies
- Power management
- External output level adjustment
- Accepts synchronous input data
- Unique Manchester decoder requires no clock
- Generates one clock per received bit
- May be used for serial decoding of indefinite word lengths
- Interfaces directly to the CT2500 protocol device
- Other Wire and Fiber Optic types available

GENERAL DESCRIPTION

The CT1698 is a single hybrid micro-circuit which incorporates a serial encoder, transceiver, and Manchester decoder in one package. The encoder accepts serial NRZ data in conjunction with two synchronous clocks.

The CT1698 receiver section accepts bipolar Manchester encoded signals and passes level detected signals to the serial decoder.

The CT1698 has a power management function and a variable drive level option. The transmitter standby mode is available to reduce the overall power consumption of the CT1698. The variable drive level output is externally programmable for testing purposes.

GPS (Farmingdale) is a MIL-STD-1772 Certified Manufacturer.

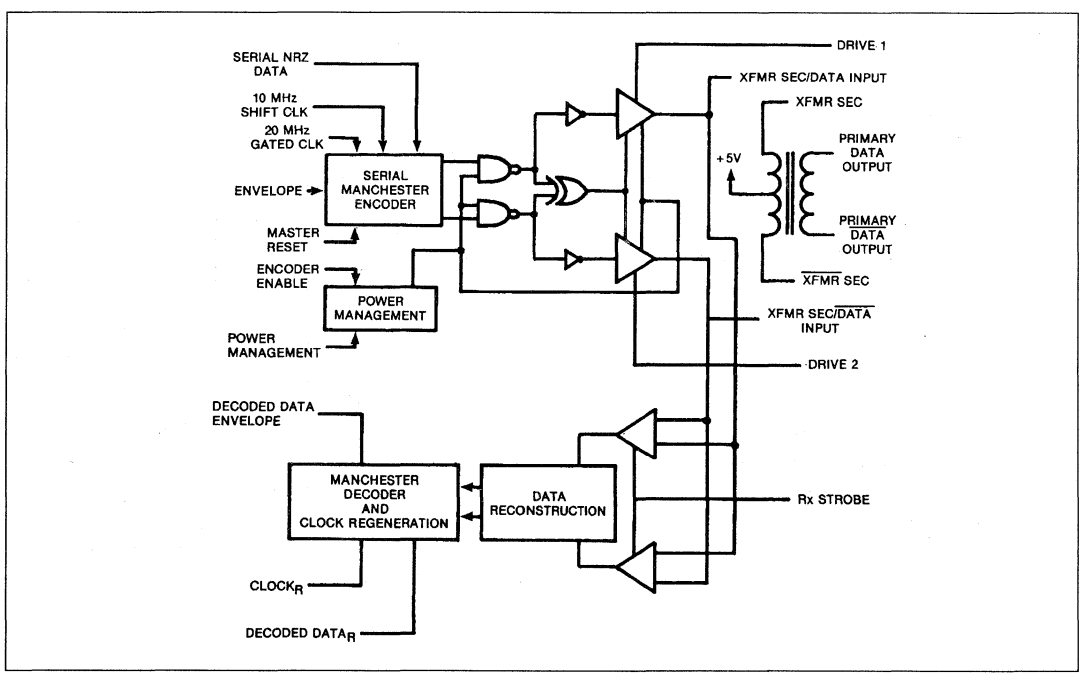


Figure 1: CT1698 Block Diagram

TRANSMISSION

The CT1698 accepts synchronous NRZ Data in conjunction with two clocks signals. The NRZ data stream is then converted to Manchester code which is transformer coupled to a 50 ohm Tri-axial cable for transmission up to 1000 ft. The synchronous transfer of data allows the separation of the CT1698 from the parallel to serial data buffer circuitry.

The transmitter may be placed into standby condition. This reduces power consumption by approximately 600mW. Power management is made available via two standard TTL input pins. The Receiver is always active and is not affected by the power management circuitry.

The drive level of the transmitter may be changed by adding external resistors to the drive pins. These pins allow the designer to externally program the transmitter output level from 0.7 to 2.8 Volts peak to peak.

The transceiver is matched for 50 ohm operation over a wide band of frequencies. This condition is maintained with power on and off.

RECEPTION

The CT1698 receiver section accepts a bipolar signal which is level detected and passed to the serial decoder. The decoder section reconstructs the data and strips the clock from the serial stream. An NRZ decoded data stream is then produced synchronously with a recovered clock. The receiver is designed to meet the MIL-STD-1397 Type E requirements.

ELECTRICAL REQUIREMENTS

The specification detailed herein encompasses a hybrid Transceiver/Encoder-Decoder designed to meet the requirements of the MIL-STD-1397 Type E. The transceiver is transformer coupled to the specified triaxial cable.

See Figure 1 for Block Diagram. Inputs and Outputs are all Synchronous NRZ DATA STREAMS. The transformer is internal to the package with its use being optional.

ENCODING TIMING/TRANSMITTER SPECIFICATIONS

SYMBOL	PARAMETER/CONDITION	MIN	TYP	MAX	UNIT
Encode timing					
t_1	Input data set-up time	10		40	ns
t_2	Encode clock set-up time	10		40	ns
t_3	Encode envelope set-up time	10		40	ns
t_4	Encode envelope turn-off time	10		35	ns
t_5	Transmitter activation set-up time	100			ns
t_6	Transmitter deactivation hold-time	50			ns
t_{w1}	20 MHz gated ck pulse width high	20		30	ns
t_{w2}	Encoder shift ck pulse width high	45		55	ns
Output signals					
Va	Output amplitude (see figure 2)	0.45	0.7	0.8	V
T	Pulse period	97	100	103	ns
Ts	Width of 1st positive half bit	45		65	ns
Te	Width of last half bit	47		65	ns
T/2	Half pulse period	47	50	53	ns
Tr	Pulse rise time	0.05		0.3	V/ns
Tf	Pulse fall time	0.05		0.3	V/ns
Vs	Voltage overshoot			100	mV
Tos	Offset Voltage 2T after last zero crossing			30	mV
Tdtx	Delay from 20 MHz clock input to data output on TXFMR. Secondary		20	55	ns
Zo	Output impedance	45	50	55	ohms

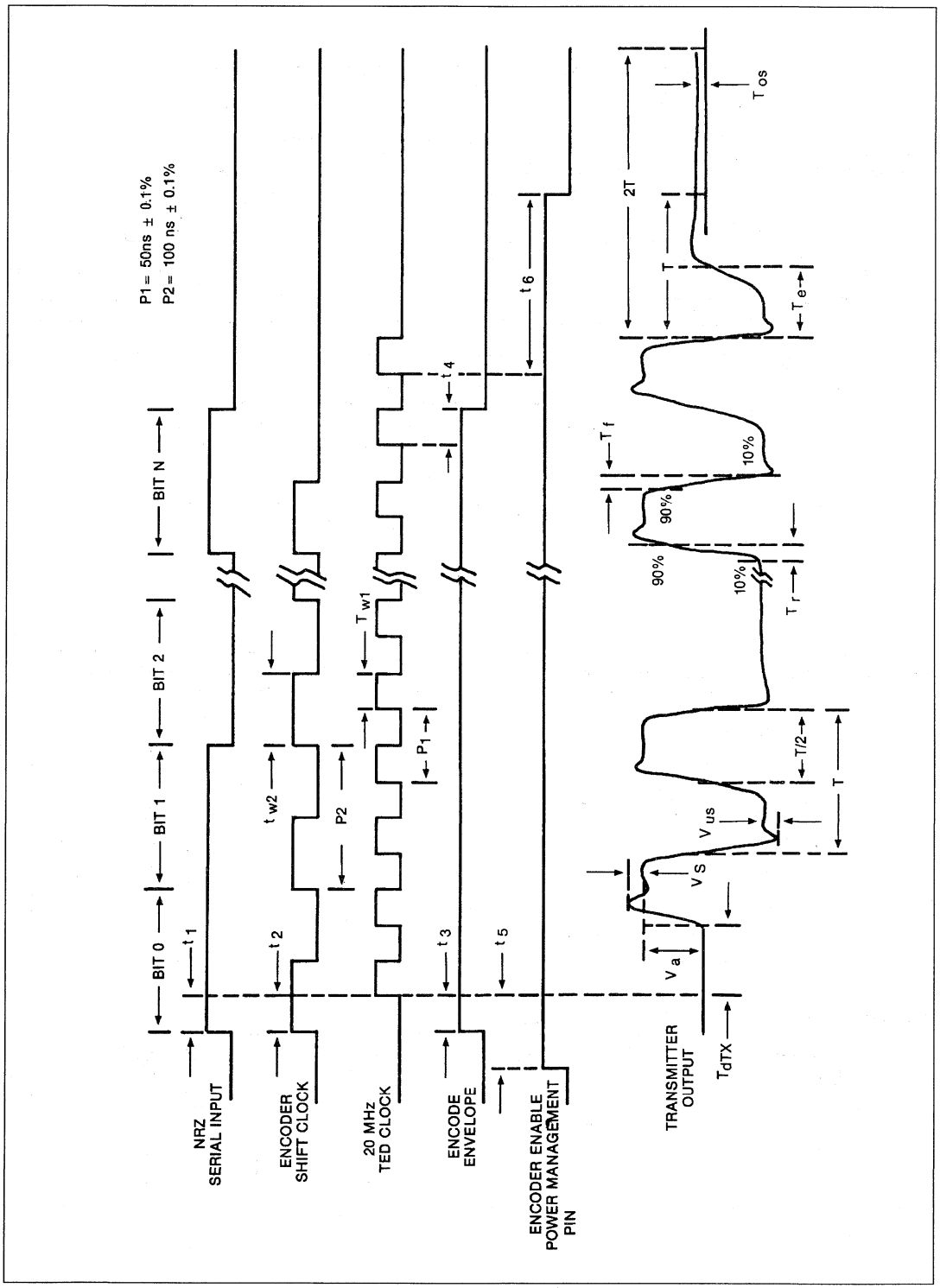


Figure 2: Encoder - Transmitter Timing

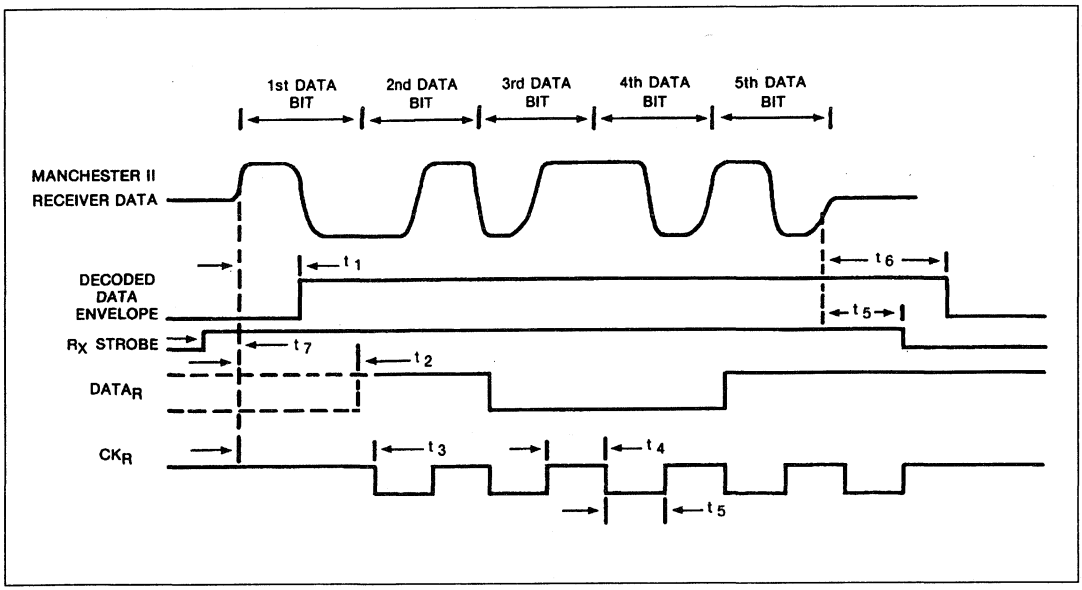


Figure 3: CT1698 Receive/Decode Timing

SYMBOL	PARAMETER/CONDITION	MIN	NOM	MAX	UNITS
t_1	Envelope delay time	-	-	100	nsec
t_2	Data decode delay	-	115	125	nsec
t_3	Clock low transition delay	-	130	-	nsec
t_4	Clock $_R$ high time	35	50	65	nsec
t_5	Clock $_R$ low time	35	50	65	nsec
t_6	Envelope off delay	120	-	270	nsec
t_7	Receiver strobe enable to input data set-up time	5			nsec
t_8	Receiver strobe disable to input data hold-time	20			

POWER MANAGEMENT FUNCTIONAL TABLE

ENCODER ENABLE (PIN 10)	POWER MANAGEMENT INPUT (PIN 9)	RECEIVER STATUS	TRANSMITTER STATUS
0	0	active	standby
x	1	active	active
1	x	active	active

Power management timing see Figure 2.

DRIVE LEVEL CONTROL PINS

External Resistors may be connected from pins 5 and 6 to V_{EE} or GND to change the Transmitter Output Level. If pins 5 and 6 are left open the CT1698 operates within the MIL-STD-1397 Type E specification. Resistors connected from pins 5 and 6 to V_{EE} or Ground must be equal. Unequal resistors will result in a transmitter output offset level.

The formula for peak to peak transmitter output swing with resistors connected between 5 and 6 to V_{EE} is:

$$V_{OUT}_{pk\text{-}pk} = 1.39 + \frac{125}{R_{EXT}} \pm 15\% \text{ VOLTS} \qquad R_{EXT} \geq 90 \text{ ohms}$$

The formula for peak to peak transmitter output swing with resistors connected between pins 5 and 6 to ground is:

$$V_{OUT}_{pk\text{-}pk} = 1.39 - \frac{50\,(V_{EE} - 2.5)}{R_{EXT}} \pm 15\% \text{ VOLTS} \qquad R_{EXT} \geq 180 \text{ ohms}$$

FUNCTIONAL DESCRIPTION AND PINOUTS

PIN #	PIN NAME	FUNCTION	LOAD OR DRIVE
1	XFMR primary/TX data output	Transformer lead for connection to center conductor of tri-axial cable	
2	XFMR secondary	Secondary isolated winding, same phase as center conductor	
3	XFMR secondary/ RX data input	Transmitter-receiver I/O pin	
4	No connection		
5	Drive 2	Output level adjustment selected by resistor to GND or V_{EE}	
6	Drive 1	Output level ajustment selected by resistor to GND or V_{EE}	
7	–5 Volts		
8	R_X strobe	Low level disables receiver	3 S loads
9	Power management input	Controls transmitter power consumption in conjunction with pin 10	1 S load
10	Encoder enable	Controls transmitter power consumption in conjunction with pin 9	1 S load
11	Case/signal GND		
12	Case/signal GND		
13	Decoded data envelope	High after reception of first half bit; goes low after reception of last half bit (normally low in inactive state).	4 S drive
14	TP3 test point	Alignment point: no electrical connection permitted	
15	TP1 test point	Alignment point: no electrical connection permitted	
16	TP2 test point	Alignment point: no electrical connection permitted	
17	–5 Volts		
18	TP4 Test point	Alignment point: no electrical connection permitted	
19	$Clock_R$	Reconstructed clock; one clock pulse per input bit received	3 S drive
20	no connection		

PIN #	PIN NAME	FUNCTION	LOAD OR DRIVE
21	decoded $data_R$	NRZ reconstructed data. Sampled on $clock_R$ rising edge	3 S drive
22	no connection		
23	+5 volts		
24	+5 volts		
25	10 MHz encoder shift clock	One cycle required per data bit. Must be high in first half of bit cell.	1 S load
26	NRZ serial input data	Serial input to be Manchester encoded with the 20 MHz gated CK.	1 S load
27	Encode envelope	Must be high to enable transmission; must go low before reception of last 20 MHz positive edge to complete transmission	1 S load
28	20 MHz Gated clock (encoder)	Each bit to be encoded requires two positive edges of the 20 MHz CK. These edges must occur at 25 ns and 75 ns into the bit cell. The end of transmission requires an additional edge in conjunction with a logic low on the encode envelope. t_R, $t_F \leq 5$ nsec.	1 S load
29	$\overline{\text{master reset}}$ reset pulse ≤15 nsec	Logic low resets encoder	2 S load
30	no connection		
31	no connection		
32	XFMR secondary/RX $\overline{\text{DATA}}$ input	Transmitter-receiver I/O pin	
33	$\overline{\text{XFMR}}$ secondary	Secondary isolated winding, same phase as outer conducter	
34	$\overline{\text{XFMR}}$ primary/TX $\overline{\text{DATA}}$ output	Transformer lead for connection to outer conductor of tri-axial	

LOAD AND DRIVE DEFINITIONS

1 S load: requires

I_{IL} = –2mA max., V_{IL} = 0.8V max

I_{IH} = 50uA max., V_{IH} = 2.5V min C_{IN} < 15 pf

1 S drive:

I_{OH} = 50uA min., V_{OH} = 2.5V min

I_{OL} = –2 mA min., V_{OL} = 0.5V max

CT1698 POWER CONSUMPTION

	Current (mA)	
	Typ	Max
I_{CC} standby mode	325	450
I_{EE} standby mode	85	105
I_{CC} 100% transmission	380	510
I_{EE} 100% transmission	125	160

ABSOLUTE MAXIMUM RATINGS

V_{CC} (Pins 23, 24) +7 Volts Max

V_{EE} (Pins 7, 17) –7 Volts Max

Logic Input Voltage Applied:

Logic Low –1.2V @ 10mA Max

Logic High +5.5 Volts

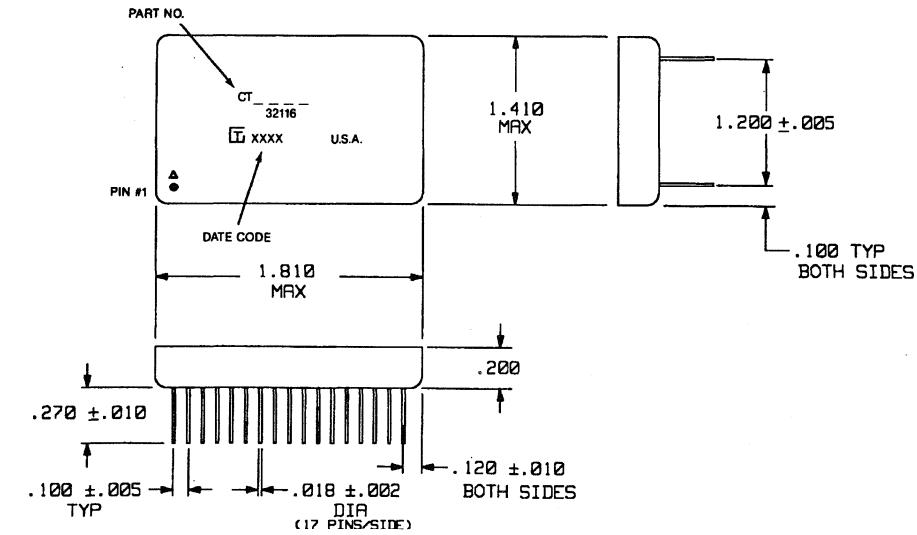
When used with the internal transformer, the CT1698 will not be damaged by cable open circuits or by short circuits of the following types:

- Line-to-line
- Line-to-ground
- To voltage sources of 0 to 115 volts alternating current, 60 hertz, line-to-ground

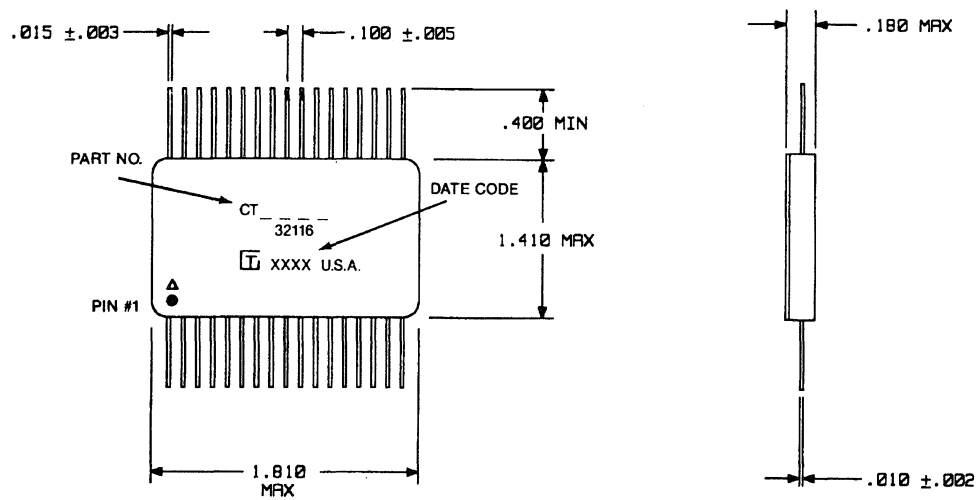
ENVIRONMENTAL PARAMETERS

Operating temperature –55°C to +100°C Case

Storage temperature –65°C to +150°C



PLUG-IN



FLAT PACK

PACKAGE OUTLINES

*Lower Packages Available, Please Contact Factory.

Figure 4: CT1698 Package Outline

3086-1.3 October 1991

CT1750

FIBRE OPTIC TRANSMITTER FOR MIL-STD-1773 & MIL-STD-1397 TYPE J

FEATURES

- Operates from DC-10MHz
- Compatible with Manchester encoded protocols such as MIL-STD-1553 and MIL-STD-1397
- No preamble needed for biasing
- Small size, hermetically sealed metal package
- 820nm wavelength
- SMA connectors for easy serviceability
- Compatible with CT1760 and CT1763 Receivers
- Compatible with all GPS MIL-STD-1553 and MIL-STD-1397 protocol units

GENERAL DESCRIPTION

The CT1750 Transmitter is designed to convert a serial TTL data stream to optical pulses. This unit couples 200µW of optical energy into a 100/140µm fiber with 0.3 N.A. The optical energy is generated by an LED source which is output stabilized over the temperature range of –55°C to +85°C. The transmitter contains a power management function which typically reduces consumption by 1 watt.

GPS (Farmingdale) is a MIL-STD-1772 Certified manufacturer.

APPLICATIONS INFORMATION

The CT1750 Transmitter is ideally suited to applications requiring the use of Manchester encoded waveforms, such as the MIL-STD-1553 and MIL-STD-1397 protocols. Standard unipolar TTL data signals are directly accepted by the CT1750 with no modification for transmission. Consequently, it is not necessary to alter the data with the addition of preamble bits. When light data is received and reconstructed during operation, the signal becomes compatible with virtually all available protocol chips – a feature that makes the CT1750 an ideal choice for implementing MIL-STD-1773 and MIL-STD-1397 Type J communication links.

A complete dual-redundant 1773 Bus Controller/Remote Terminal would consist of two CT1750 Transmitters, two CT1763 Receivers, and one CT2529 Protocol/Interface hybrid. See Figure 4.

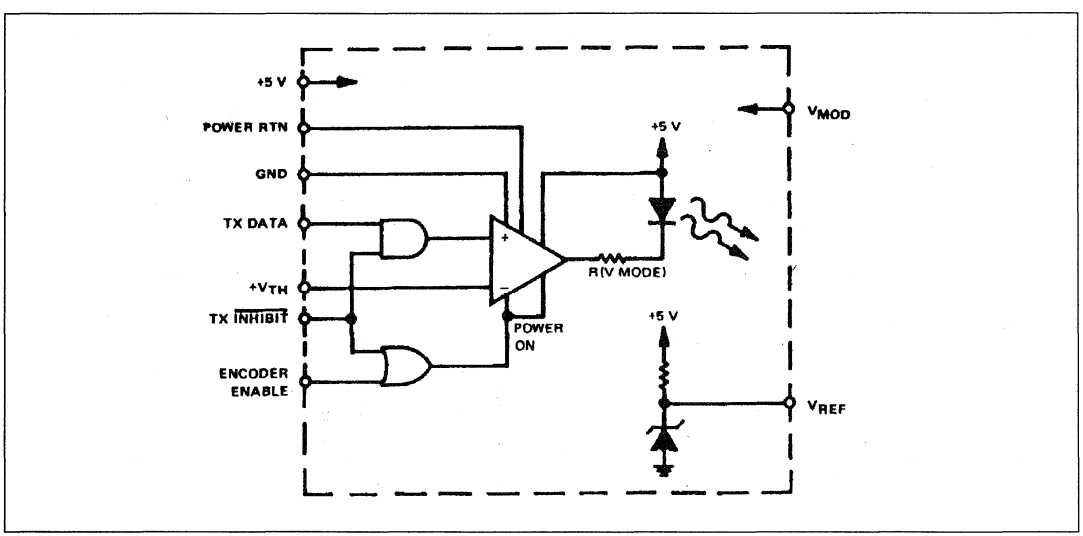


Figure 1: Functional Diagram - CT1750

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

DC Voltage	Tolerance	Current (mA)	
		Nominal	Max
+5V	±10%	250	290

POWER MANAGEMENT

Power	Current (mA)	
	Nominal	Max
+5V Standby	60	80
+5V 100% Transmission	250	290

TRANSMITTER SPECIFICATIONS (SEE FIGURE 2)

Symbol	Parameter/Condition	Min	Type	Max	Unit
	Output Signals				
TP_o	Peak Output Signal	100		300	µW
TP_r	Peak Residual Power			0.5	µW
T_r	Pulse Rise Time			12	ns
T_f	Pulse Fall Time			12	ns
λp	Peak Wavelength of Emission		820		nM
Δλ	Spectral Width (50% Points)		40		nM
ΔTP_o	Peak Power Output Change –55 to +85°C		2.5dB		
V_s	Combined Optical Overshoot and Undershoot		15	%	

OUTPUT/POWER MANAGEMENT FUNCTION TABLE

Data	TX $\overline{INH}$	ENC ENA	Output	Power State
X	0	0	Off	Standy
1	1	1	On	Active
0	1	1	Off	Active
X	0	1	Off	Active

LOAD LIMITS

	Voltage	Current
Data, Enc.	V_{ih}=2.4V	I_{ih}=40µA
Enable	V_{il}=0.4V	I_{il}=–2mA
	C_{in}=7pF	
TX $\overline{INHIBIT}$	V_{ih}=2.4V	O_{ih}=80µA
	V_{il}=0.4V	I_{il}=–4mA

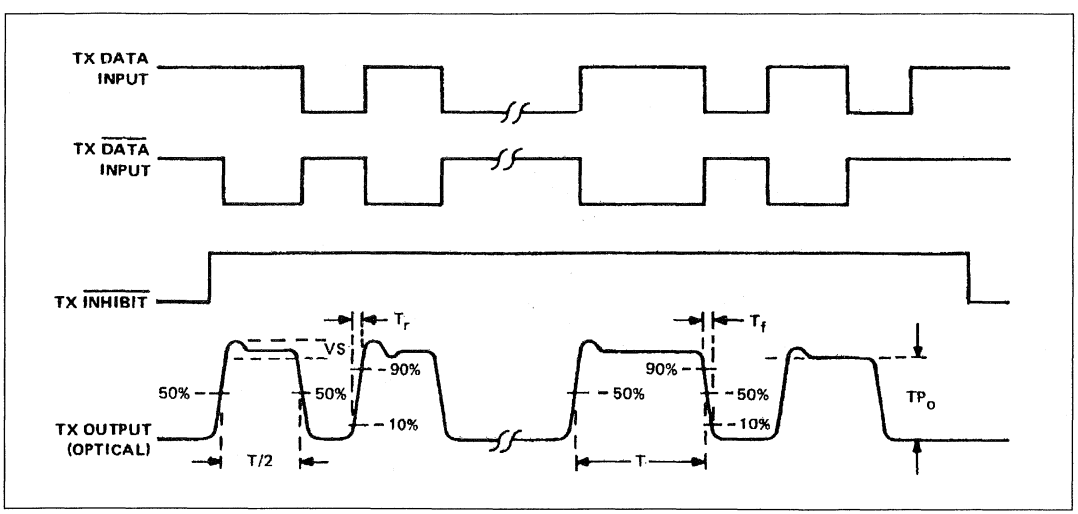


Figure 2: CT1750 Transmitter Waveforms

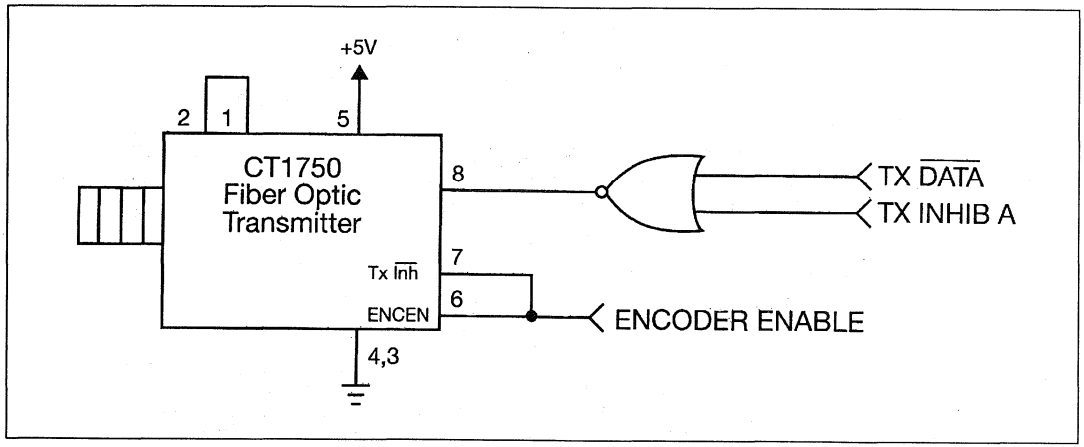


Figure 3: CT1750 Typical Transmitter Configuration

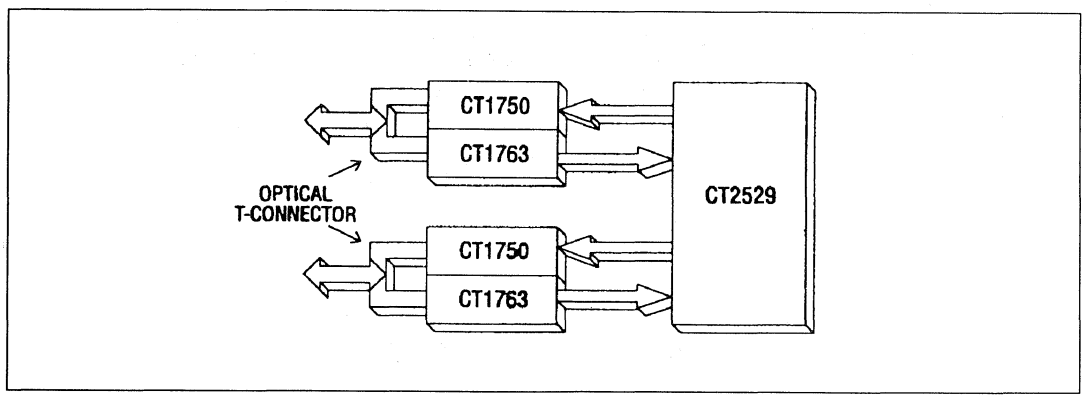


Figure 4: A 1773 Terminal Configuration

PIN ASSIGNMENTS

1 – VOLTAGE REFERENCE	5 – +5V
2 – VOLTAGE DRIVE	6 – ENC ENABLE
3 – CURRENT RETURN POINT	7 – TX $\overline{\text{INH}}$
4 – GND	8 – DATA

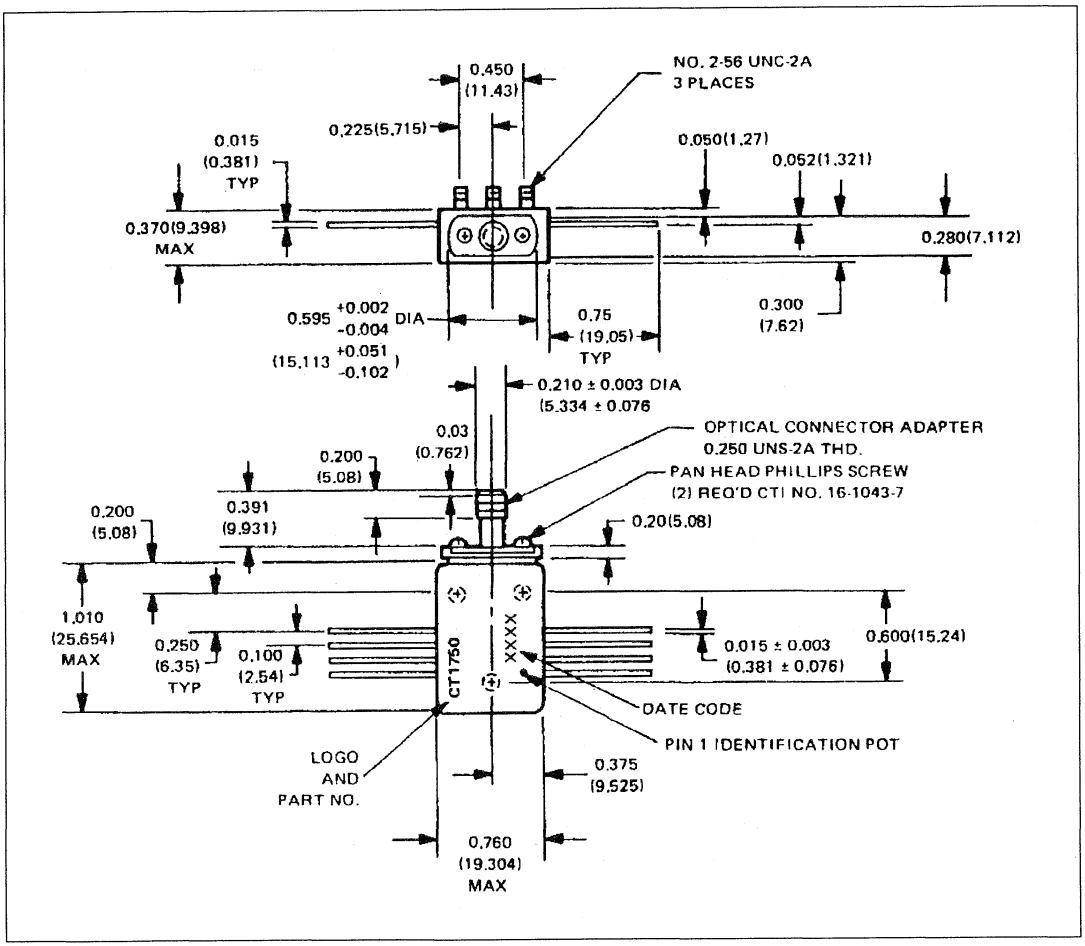


Figure 5: Package Outline - CT1750

3083-1.2 September 1991

CT1760

10MHZ FIBRE OPTIC RECEIVER FOR MIL-STD-1397 TYPE J

FEATURES

- Tuned for 10MHz operation
- Compatible with existing MIL-STD-1397 protocols
- Small size, hermetically sealed metal package
- 820nm wavelength
- SMA connectors for easy serviceability
- Compatible with CT1750 optical outputs

GENERAL DESCRIPTION

The CT1760 Receiver is designed to convert an optical input stream to TTL digital data and operates with data rates of up to 10Mb/sec Manchester. Differential and adaptive circuits are utilized for gain control under burst type transmissions which are common to multi-terminal bus configurations. The Receiver automatically synchronizes to the first data bit and does not require preamble bits to bias the unit. This feature allows the user to implement a MIL-STD-1397 Type J fiber optic channel with mo modifications to the existing protocol circuitry.

GPS (Farmingdale) is a MIL-STD-1772 Certified manufacturer.

APPLICATIONS INFORMATION

The CT1760 is ideally suited to implement a MIL-STD-1397 Type J channel. It is tuned specifically for 10MHz operation. Its TTL outputs can be readily reconstructed to the Manchester waveform requirement for all existing protocol chips, thus allowing for convenient compatibility with Type E and Type J applications. See Figure 3.

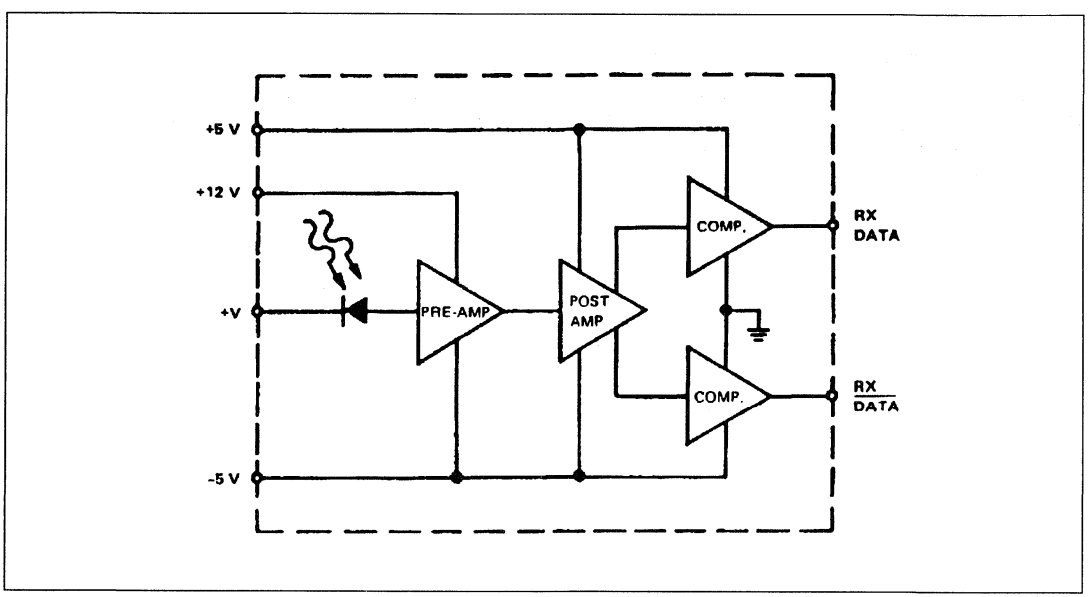


Figure 1: Functional Diagram - CT1760

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

DC Voltage	Tolerance	Power (mA)	
		Typical	Max @ 100%
+5V	±10%	70	96
–5V	±10%	50	64
+12V	±10%	25	33

DRIVE LIMITS

	Voltage	Current	
Data and $\overline{\text{Data}}$	V_{OH}=2.4V	I_{OH}>–80 µA	C_L=15pF
	V_{OL}=0.4V	I_{OL}>4mA	C_L=15pF

TRANSMITTER SPECIFICATIONS (SEE FIGURE 2)

Symbol	Parameter/Condition	Min	Max	Unit
Input Signals				
RP_0	Peak Optical Input Power (See Note)	1	150	µW
T	Input Pulse Period	93	107	ns
T/2	Half Pulse Period	43	57	ns
T_r	Input Optical Rise Time		20	ns
T_f	Input Optical Fall Time		20	ns
Output Signals				
T_0	DATA or $\overline{\text{DATA}}$ Pulse Width Output	10		ns

Note: Exit power from a 100/140um fiber with cladding modes stripped. Sensitivity is benchmarked for unipolar 10Mb/sec Manchester code.

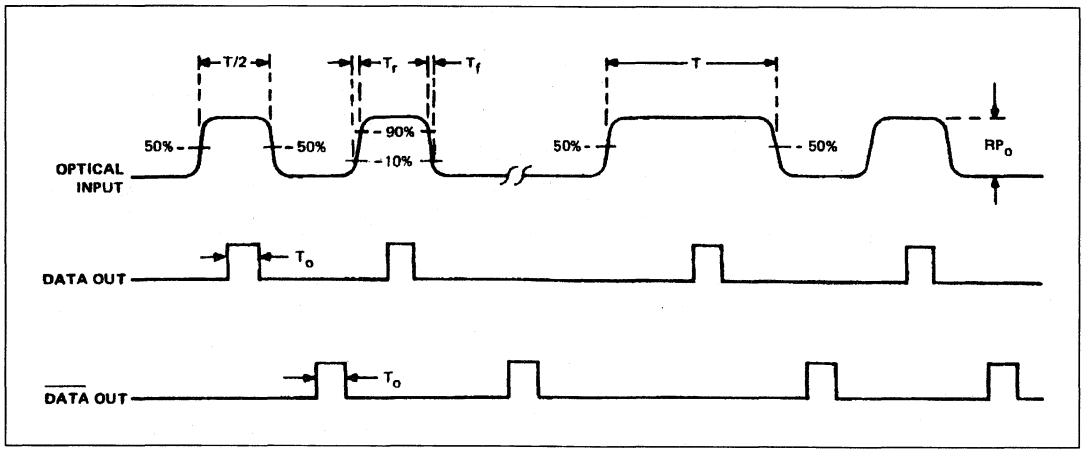


Figure 2: CT1760 Receiver Waveforms

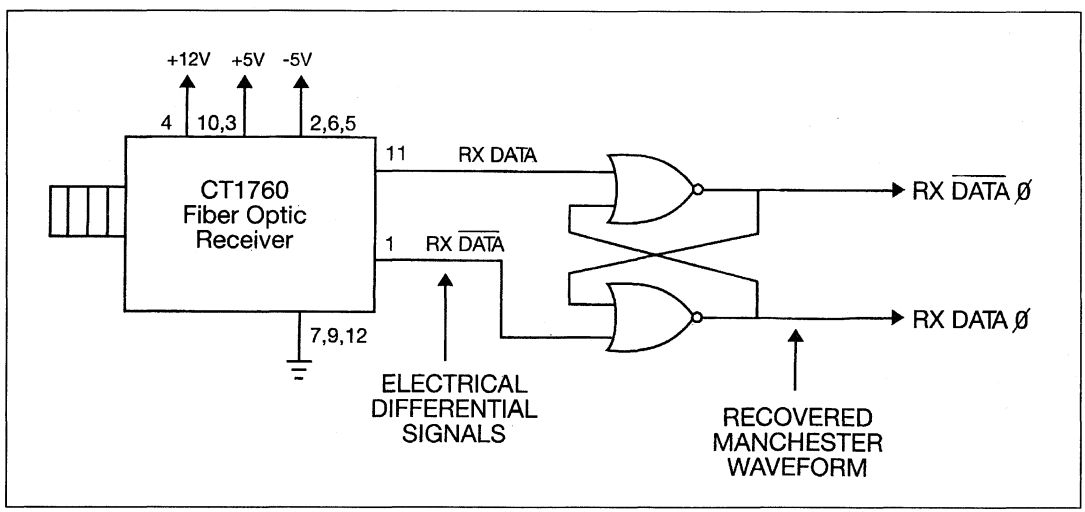


Figure 3: CT1760 Manchester Waveform Recovery

PIN ASSIGNMENTS

1 – $\overline{\text{DATA}}$	5 – –5V	9 – GND
2 – –5V	6 – –5V	10 – +5V
3 – +5V	7 – GND	11 – DATA
4 – +12V	8 – LEVEL OUTPUT	12 – GND

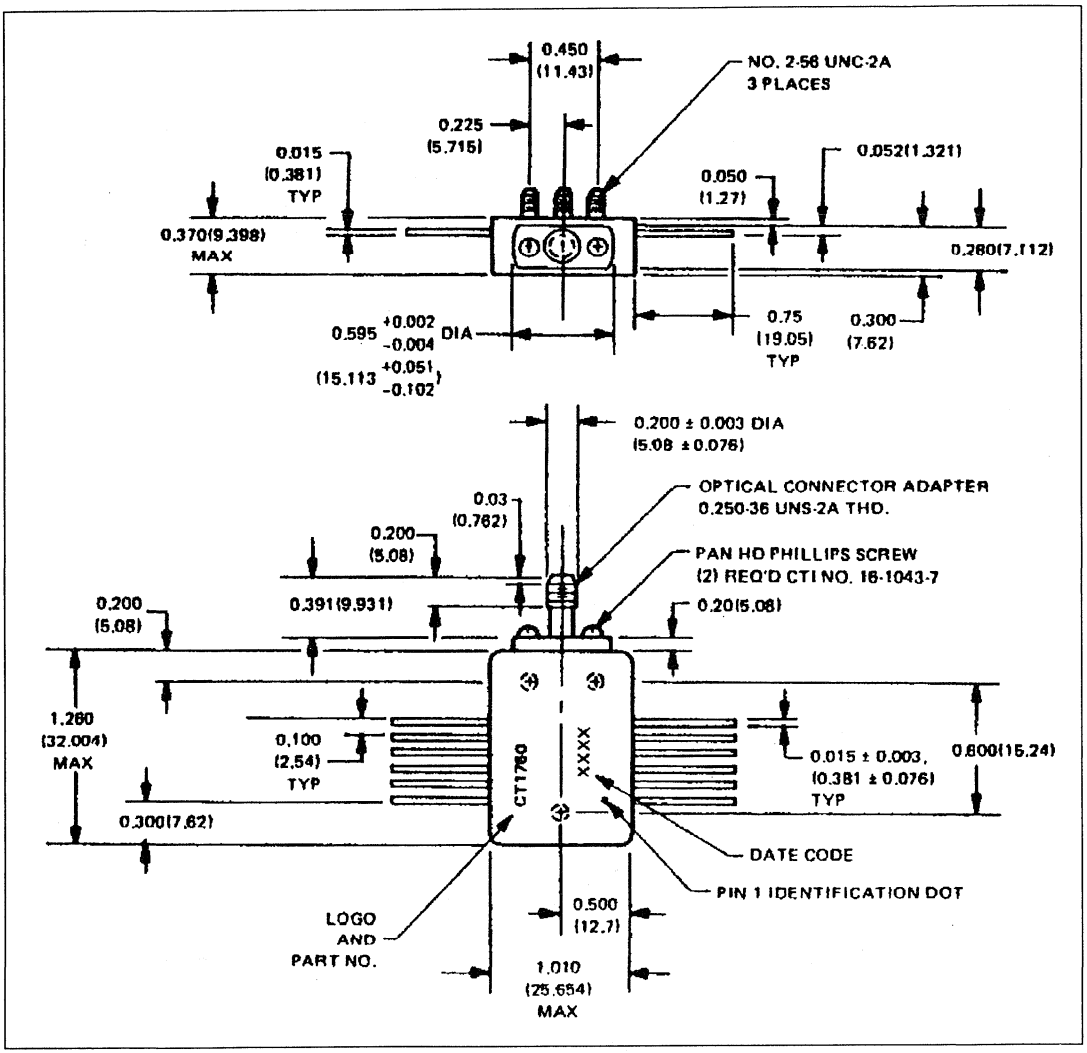


Figure 4: Package Outline - CT1760

DS3085-1.3 October 1991

CT1815

10MHz LOW LEVEL SERIAL INTERFACE FOR MIL-STD-1397 TYPE D

FEATURES

- Internally set threshold
- Matched to 75 ohm system impedance power on and off
- Operates with ±5 volt supplies
- Power management
- Accepts synchronous input data
- Unique Manchester decoder requires no clock
- Generates one clock per recieved bit
- May be used for serial decoding of indefinite word lengths
- Other Wire and Fiber Optice types available

GENERAL DESCRIPTION

The CT1815 is a single hybrid micro-circuit which incorporates a serial encoder, transceiver, and Manchester decoder in one package. The encoder accepts serial NRZ data in conjunction with two synchronous clocks. This data stream is then Manchester encoded and transformer coupled to a 75 ohm tri-axial cable for transmission through up to 1000 feet of cable.

The CT1815 receiver section accepts bipolar Manchester encoded signals and passes level detected signals to the serial decoder. The serial decoder reconstructs an NRZ data stream with derived clock. This allows the data to be processed by our CT2500 monolithic protocol chip for MIL-STD-1397 serial interfaces. All the input and output signals of the CT1815 are completely compatible with the CT2500.

The CT1815 has a power management function. A transmitter standby mode is available to reduce the overall power consumption of the CT1815.

GPS (Farmingdale) is a MIL-STD-1772 Certified manufacturer.

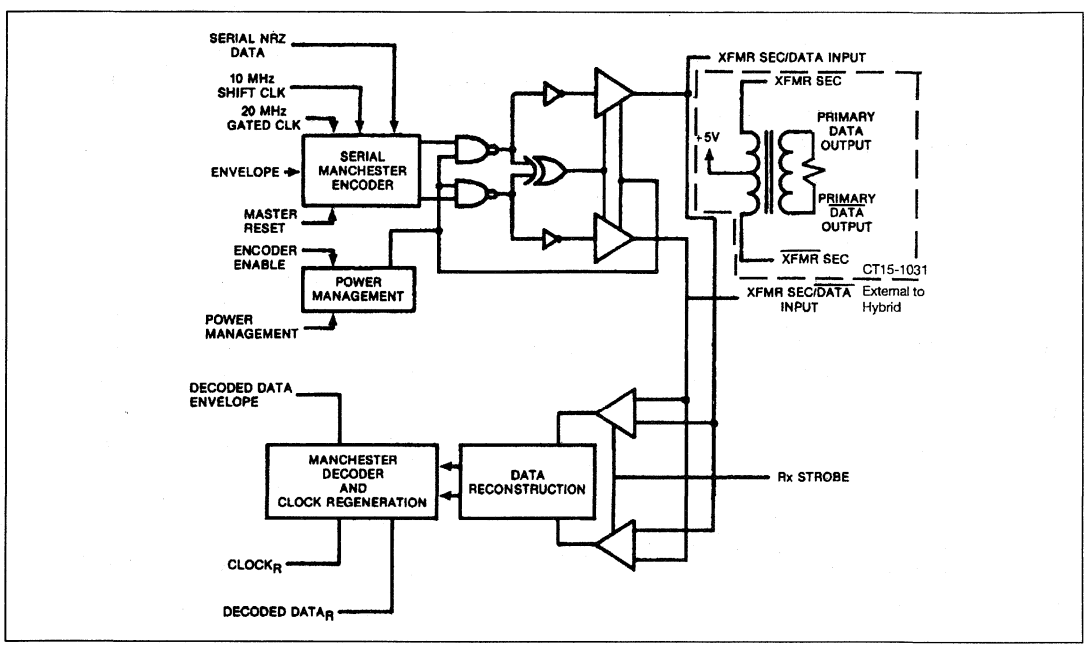


Figure 1: CT1815 Block Diagram

TRANSMISSION

The CT1815 accepts synchronous NRZ Data in conjunction with two clocks signals. The NRZ data stream is then converted to Manchester code which is transformer coupled to a 75 ohm Tri-axial cable for transmission up to 1000 ft. The synchronous transfer of data allows the separation of the CT1815 from the parallel to serial data buffer circuitry.

The transmitter may be placed into a standy condition. This reduces consumption by approximately 600mW. Power managment is made available via two standard TTL input pins. The Receiver is always active and is not affected by the power management circuitry.

The transceiver is matched for 75 ohm operation over a wide band of frequencies. This condition is maintained with power on and off.

RECEPTION

The CT1815 receiver section accepts a bipolar signal which is level detected and passed to the serial decoder. The decoder section reconstructs the data and strips the clock from the serial stream. An NRZ decoded data stream is then produced synchronously with a recovered clock. The receiver is designed to meet the MIL-STD-1397 Type D requirements.

ELECTRICAL REQUIREMENTS

The specification detailed herein encompasses a hybrid Transceiver/Encoder-Decoder designed to meet the requirements of the MIL-STD-1397 Type D. The transceiver is transformer coupled to the specified triaxial cable and is screened to MIL-STD-883 Method 5008.1

See Figure 1 for Block Diagram. Inputs and Outputs are all Synchronous NRZ DATA STREAMS.

TRANSFORMER ISOLATION

The CT1815 is connected with pin 3 and pin 32 to the CT 15-1031 transformer secondary winding. The center tap of the secondary winding is connected to +5 Volts. For matching 75Ω load operation, a 78Ω resistor must be placed across the primary winding of the transformer.

ENCODER TIMING/TRANSMITTER SPECIFICATIONS

SYMBOL	PARAMETER/CONDITION	MIN	TYPE	MAX	UNIT
	Encode Timing				
t_1	Input Data Set-up Time	10		40	ns
t_2	Encode Clock Set-up Time	10		40	ns
t_3	Encode Envelope Set-up Time	10		40	ns
t_4	Encode Envelope Turn-off Time	10		35	ns
t_5	Transmitter Activation Set-up Time	150			ns
t_6	Transmitter Deactivation Hold-time	50			ns
t_{w1}	20MHz Gated CK Pulse Width High	20		30	ns
t_{w2}	Encoder Shift CK Pulse Width High	45		55	ns
	Output Signals				
Va	Output Amplitude (See Figure 2)	2.75	3.25	3.75	Volts
T	Pulse Period	97	100	103	ns
Ts	Width of 1st Positive Half Bit	45		65	ns
Te	Width of Last Half Bit	47		65	ns
T/2	Half Pulse Period	47	50	53	ns
Tr	Pulse Rise Time			2.0	V/ns
Tf	Pulse Fall Time			2.0	V/ns
Vs	Voltage Overshoot			350	mV
Tos	Offset Voltage 2T After Last Zero Crossing			150	mV
Tdtx	Delay From 20 MHz Clock Input to Data Output on Transformer Secondary		20	55	ns
Zo	Output Impedance	70	75	80	ohms

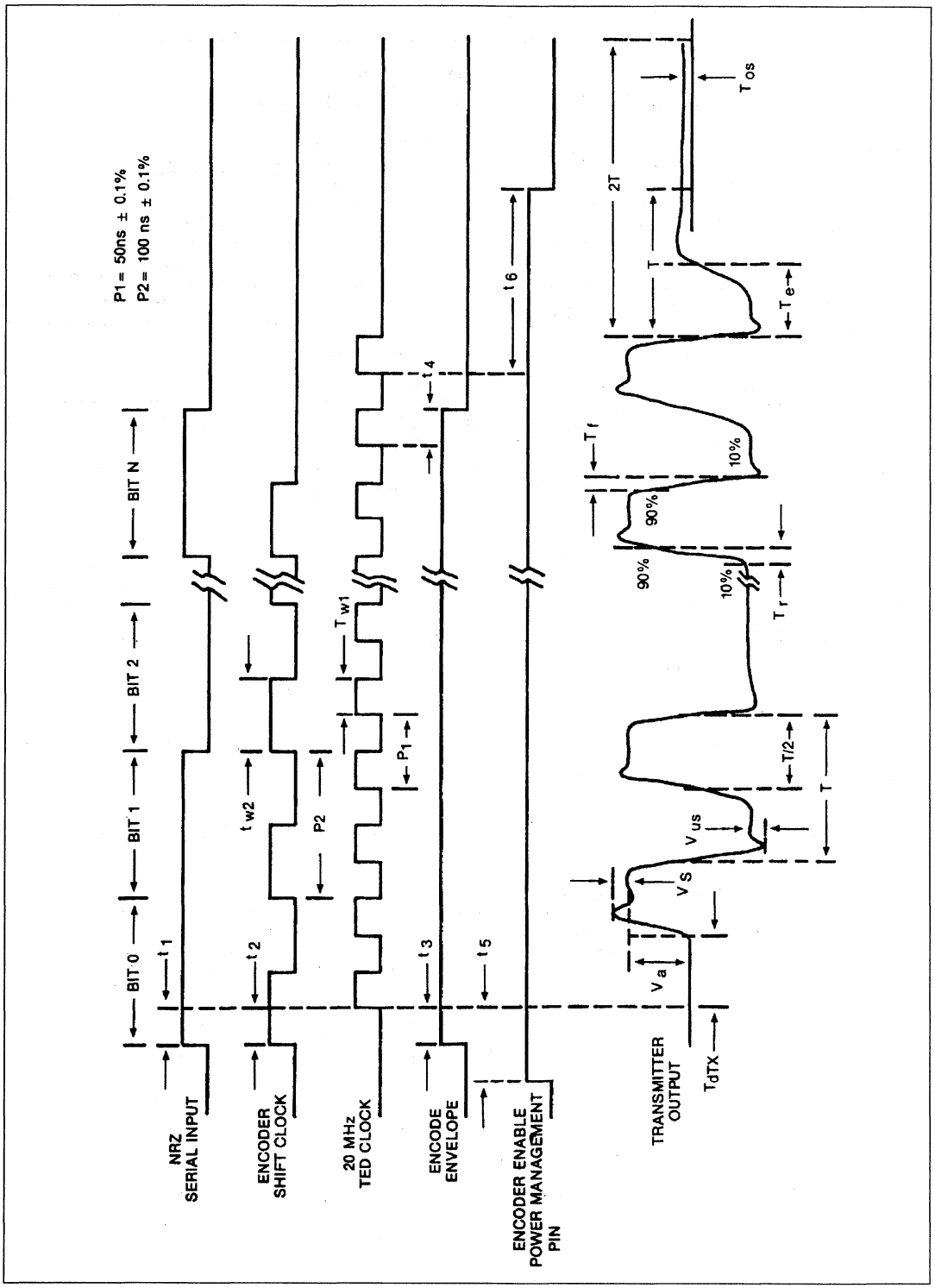


Figure 2: Encoder - Transmitter Timing

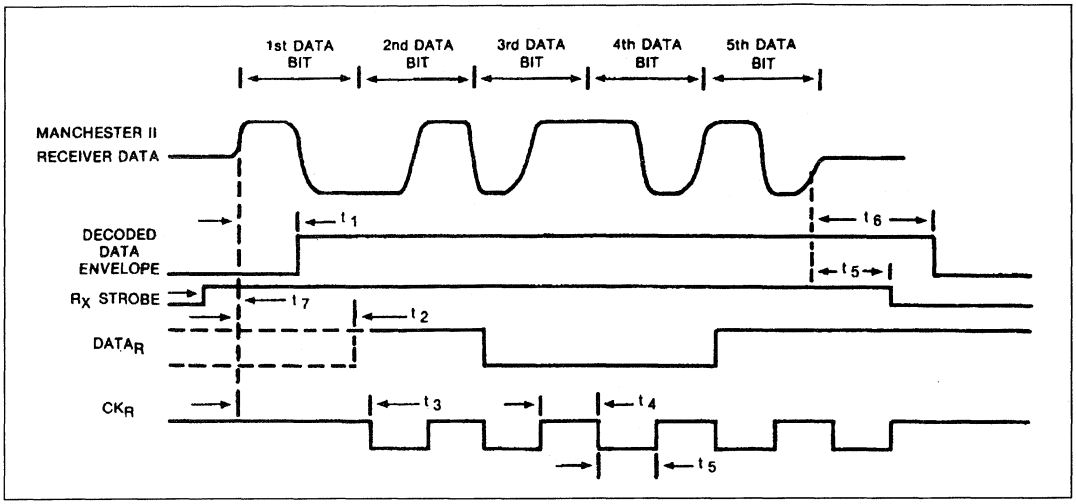


Figure 3: CT1815 Receive/Decode Timing

Symbol	Parameter/Condition	Min	Nom	Max	Units
t1	Envelope Delay Time		45	100	ns
t2	Data Decode Delay		115	125	ns
t3	Clock Low Transition Delay		130		ns
t4	$Clock_R$ High Time	35	50	65	ns
t5	$Clock_R$ Low Time	35	50	65	ns
t6	Envelope Off Delay	120		270	ns
t7	Receiver Strobe Enable to Input Data Set-Up Time	5			ns
t8	Receiver Strobe Disable to Input Data Hold-Time	20			

POWER MANAGEMENT FUNCTIONAL TABLE

Encoder Enable (PIN 10)	Power Management Input (PIN 9)	Receiver Status	Transmitter Status
0	0	Active	Standby
X	1	Active	Active
1	X	Active	Active

Power Management Timing See Figure 2.

FUNCTIONAL DESCRIPTION AND PINOUTS

Pin #	Pin Name	Function	Load or Drive
1	No Connection		
2	No Connection		
3	XFMR Secondary/ RX Data Input	Transmitter-Receiver I/O Pin	
4	No Connection		
5	No Connection		
6	No Connection		
7	–5 Volts		
8	R_X Strobe	Low Level Disables Receiver	3 S Loads
9	Power Management Input	Controls Transmitter Power Consumption In Conjunction With Pin 10	1 S Load
10	Encoder Enable	Controls Transmitter Power Consumption In Conjunction With Pin 9	1 S Load
11	Case/Signal GND		
12	Case/Signal GND		
13	Decoded Data Envelope	High After Reception of First Half Bit; Goes Low After Reception of Last Half Bit (Normally Low in Inactive State)	4 S Drive
14	TP3 Test Point	Alignment Point: No Electrical Connection Permitted	
15	TP1 Test Point	Alignment Point: No Electrical Connection Permitted	
16	TP2 Test Point	Alignment Point: No Electrical Connection Permitted	
17	–5 Volts		
18	TP4 Test Point	Alignment Point: No Electrical Connection Permitted	
19	$Clock_R$	Reconstructed Clock; One Clock Pulse Per Input Bit Received	3 S Drive
20	No Connection		
21	$Decoded\ Data_R$	NRZ Reconstructed Data. Sampled on $Clock_R$ Rising Edge.	3 S Drive
22	No Connection		
23	+5 Volts		
24	+5 Volts		
25	10 MHz Encoder Shift Clock	On Cycle Required Per Data Bit. Must Be High in First Half Of Bit Cell	1 S Load
26	NRZ Serial Input Data	Serial Input To Be Manchester Encoded With The 20 MHz Gated Ck.	1 S Load
27	Encode Envelope	Must be High to Enable Transmission. Must Go Low Before Reception Of Last 20 MHz Positive Edge To Complete Transmission	1 S Load
28	20 MHz Gated Clock (Encoder)	Each Bit To Be Encoded Requires Two Positive Edges Of The 20 MHz Ck. These Edges Must Occur At 25 ns And 75 ns Into The Bit Cell. The End of Transmission Requires An Additional Edge In Conjunction With A Logic Low On The Encode Envelope. t_R, $t_F \leq 5$ ns.	1 S Load
29	$\overline{\text{Master Reset}}$	Logic Low Resets Encoder Reset Pulse ≥ 15 ns.	2 S Load
30	No Connection		
31	No Connection		
32	XFMR Secondary/ RX $\overline{\text{Data}}$ Input	Transmitter-Receiver I/O Pin	
33	No Connection		
34	No Connection		

LOAD AND DRIVE DEFINITIONS

1 S Load: Requires	I_{IL} = –2 mA Max., V_{IL} = 0.8V Max	
	I_{IH} = 50 uA Max., V_{IH} = 2.5V Min	C_{IN}<15pf
1 S Drive:	I_{OH} = 50 uA Min., V_{OH} = 2.5V Min	
	I_{OL} = –2 mA Min., V_{OL} = 0.5V Max	

CT1815 POWER CONSUMPTION

	Current (mA)	
	Typ	**Max**
I_{CC} Standby Mode	235	305
I_{EE} Standby Mode	75	100
I_{CC} 100% Transmission	447	585
I_{EE} 100% Transmission	242	315

ABSOLUTE MAXIMUM RATINGS

VCC (Pins 23, 24) +7 Volts Max
VEE (Pins 7,17) –7 Volts Max

Logic Input Voltage Applied:
Logic Low –1.2V @ 10mA Max
Logic High +5.5 Volts

Damage will not result from cable open circuits or short circuits (on the transformer primary) of the following types:

- Line-to-line
- Line-to-ground
- 120V AC 60Hz common mode signal

ENVIRONMENTAL PARAMETERS

Operating Temperature –55°C to +100°C Case
Storage Temperature –65°C to +150°C
Screened per MIL-STD-883B Method 5008 except as outlined here.
Burn-in: 168 hours at +100°C case temperature.

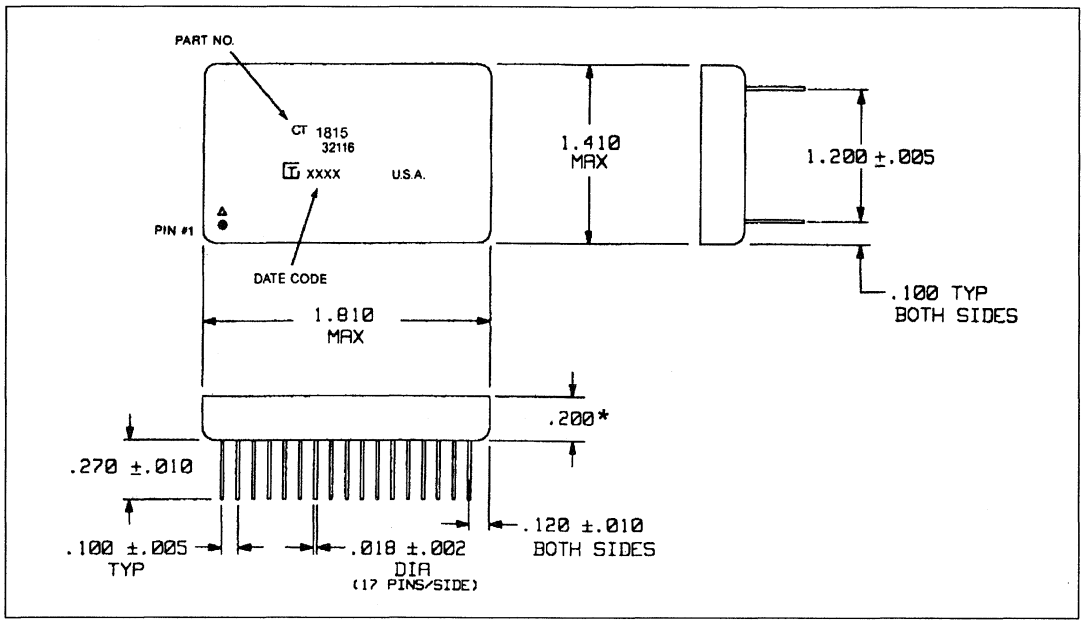


Figure 4: Plug-In Package Outline - CT1815

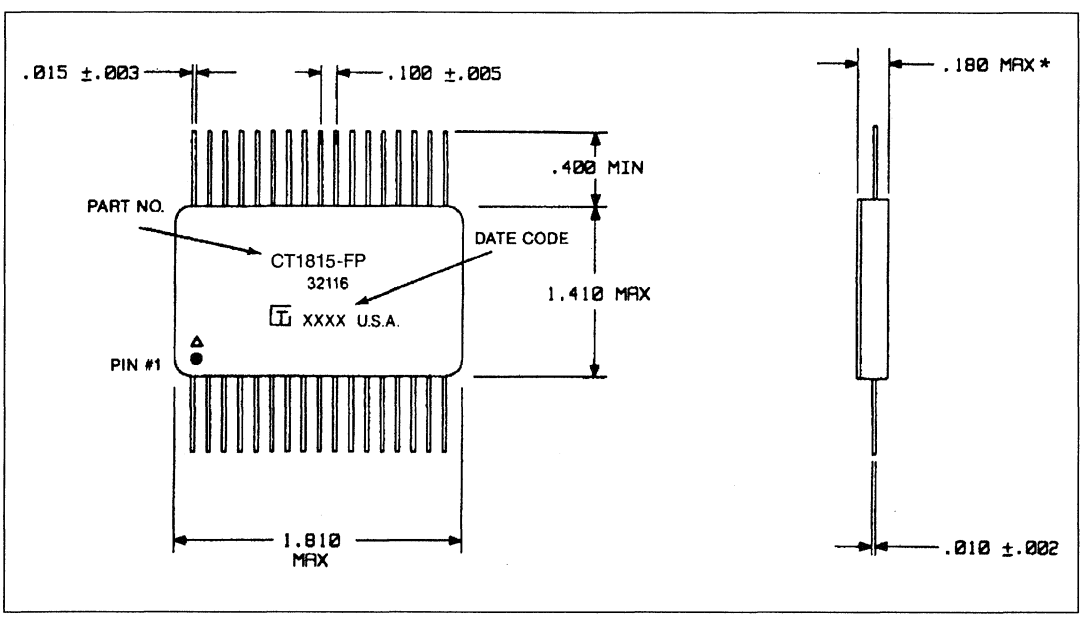


Figure 5: Flatpack Package Outline - CT1815

3084-1.3 October 1991

CT2500

MIL-STD-1397 TYPE D & E LOW LEVEL SERIAL INTERFACE PROTOCOL CHIP

FEATURES

- Performs Source and Sink functions
- Implements Type D&E protocols
- Burst Mode Capability
- Build in System Integrity Features
- Double Buffered Communications
- Low power CMOS
- Available in PGA or JEDEC type C LCC Package (CT2500-1)
- Operates over full Military temperature range –55°C to +125°C

GENERAL DESCRIPTION

The CT2500 provides a complete interface between the MIL-STD-1397 transceiver chip set (CT1698) and most microprocessor based systems. The unit is monolithic and fabricated in CMOS technology, thereby having very low power requirements. The unit handles all protocols of Type D&E interfaces including Burst Mode Data and forced EF functions. This unit is available screened to the individual test methods of MIL-STD-883C Method 5004.

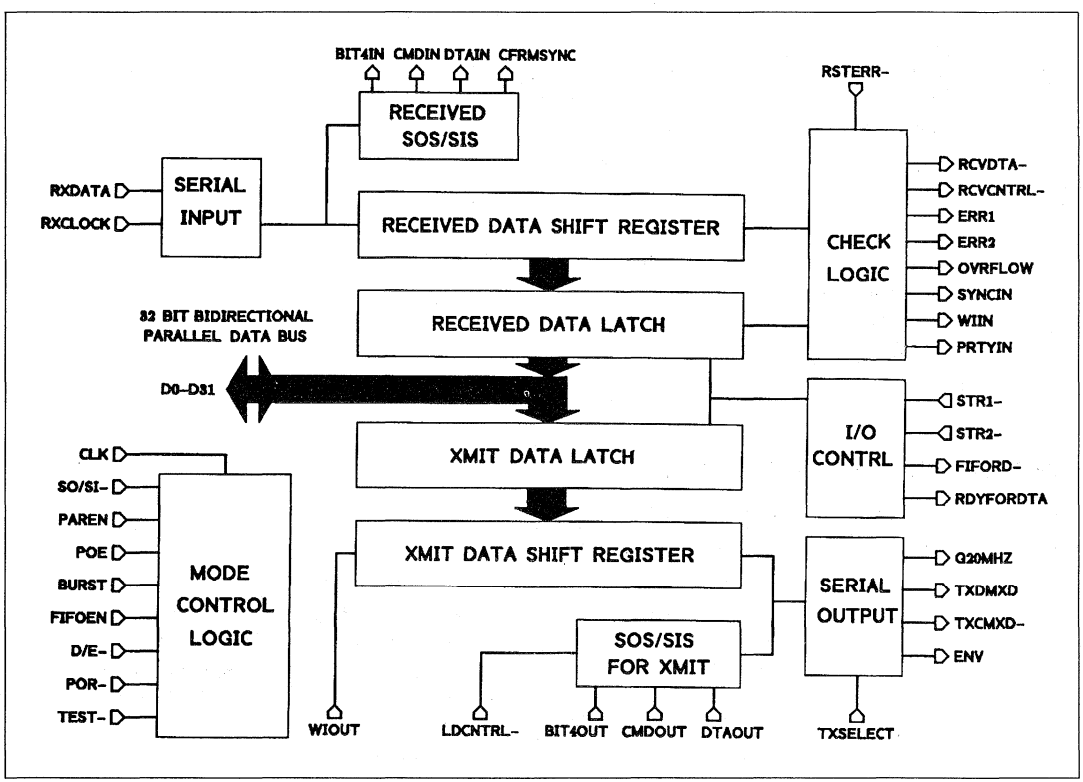


Figure 1: Functional Block Diagram - CT2500

I/O CONTROL

The CT2500 is very flexible in it's I/O architecture. The unit can handle 16 bit and 32 bit data and command word loading. In addition, data words can be preloaded into a FIFO and the unit will load data words from the FIFO directly without subsystem intervention. Similarly, data can be received and automatically loaded into a FIFO. This frees up the subsystem until the data transfer is complete. These options are desirable especially when operating under burst mode transmissions. Control frames are sent by strobing LDCNTRL and data is sent by strobing STR2.

DATA TRANSFERS

The CT2500 is built to send and receive Type D and E Control frames. It can transmit and receive 32-bit command and data word. All 32-bit communications are double buffered for maximum flexibility. This allows the subsystem to respond with less critical timing constraints. Burst mode data transmission can be initiated by setting the "Burst Mode" pin high. Automatic FIFO operation is enabled by setting "FIFOEN" pin high. The serial data out is automatically formatted for the CT1698 to send out along the cable.

SOURCE AND SINK MODES

Both Source and Sink Mode operations are available in the CT2500. Selection of modes is accomplished through the Source/Sink pin. In the Source Mode, the unit will transmit control frames, 32 bit command and data words including burst mode data. It will receive control frames only. In Sink Mode, the unit will transmit control frames only and receive control frames, 32 bit command and data words, and burst mode data.

SYSTEM INTEGRITY FEATURES

The CT2500 has built in system integrity features. The unit can generate and send parity with all 32 bit transmissions. For reception of 32 bit words, the unit can check for parity, frame, overrun sync, and bit errors.

CT2500 DEVICE SPECIFICATION

D.C. ELECTRICAL CHARACTERISTICS (–55 DEG. C TO +125 DEG. C)

SYMBOL	PARAMETER	LIMIT (VDD = 5V ±10%)
Idd	Quiescent current	100uA max
Pds	Power Dissipation	200mW max
Iin	Input leakage	10uA max
Ioz	Tri-state leakage	10uA max
Vih	Input high level	2.0V min
Vil	Input low level	0.8V max
Voh	Output high level	2.4V min @ Ioh = –4mA
Vol	Output low level	0.4V max @ Iol = 4mA

CT2500 DEVICE I/O FUNCTION LISTING

NAME	I/O	DESCRIPTION
SO/SI–	**I**	**Source / Sink Mode Select**
		Determines the overall Functioning Mode of the Device
		"1" = Source emulation. This mode enables the chip to send control frames, single command and data words and burst data. It is able to receive control frames.
		"0" = Sink emulation. In this mode, the chip can only send control frames. It can receive control frames, command words, single data words and burst data.
DO–D31	**I/O**	**Parallel Bi-directional Data Bus** (Internal Pullups)
		Source Mode: Input to 32 bit transmit data latch
		Sink Mode: Tri-state output from 32 bit received data latch

CT2500 DEVICE I/O FUNCTION LISTING, Cont'd.

NAME	I/O	DESCRIPTION
D/E–	I	**Type D / Type E Control Frame Length Select** (Internal Pulldown) "1" = Three bit control frames are transmitted and the received control frame is checked for a proper three bit length. "0" = Four bit control frames are transmitted and the received control frame is checked for a proper four bit length.
PAREN	I	**Parity Enable** (Internal Pullup) "1" = Parity bit is generated in Source mode and checked for in Sink mode. "0" = No parity is generated or checked for.
POE	I	**Parity Odd or Even Select** (Internal Pullup) "1" = Odd parity "0" = Even parity
CLK	I	**System Clock** 20 megahertz with 50% duty cycle
BURST	I	**Burst Mode Select** "1" = Data transmission and Reception can be done in Burst mode "0" = Normal operation Source Mode: Data words loaded during the transmission of another will be concatenated to the transmission without addition of SYNC or WI bits. The first word will have a SYNC bit of "1" and and a WI bit, which must be set to "0". The Burst line must remain stable for the entire duration of the loading and transmission of the data. Sink Mode: During a Burst data reception, after the SYNC and WI bits, data words are picked off at bit count multiples of 32, or 33 with parity enabled, and loaded into the output latch. The transmission is considered ended when a gap is detected. The line must be stable during the entire reception.
STR1– and STR2–	I	**Strobe One Bar and Strobe Two Bar** Control Strobes for Reading and Writing the Parallel I/O data Latches Source Mode: STR1– loads data present on DO–D15 into the lower 16 bit input latch and STR2– loads data on D16–D31 into the upper 16 bit input latch. Upon completion of STR2–, a sequence is initiated to load the entire 32 bits into a shift register and start a transmission. The lower 16 bits must be loaded prior to or during the load of the upper 16 bits. For a 32 bit load, STR1– and STR2– can be tied together. Sink Mode: STR1– enables the lower 16 bits of a received word to be output on D0–D15. STR2– enables the upper 16 bits of a received word to be output on D16–D31. The entire 32 bits of data must be read before another data reception or it will be overwritten. If this occurs, the overflow flag, OVRFLOW, will go high. The data is considered completely read upon the completion of STR2–.
CMDIN	O	**Command In** Third bit of the Received Control Frame. Valid during RCVCNTRL–.
DTAIN	O	**Data In** Second bit of the Received Control Frame. Valid during RCVCNTRL–.
RCVCNTRL–	O	**Received Control Bar** Pulses low upon reception of a Control Frame in both Sink and Source modes.
RCVDTA–	O	**Received Data/Command Word Bar** Pulses low upon reception of a Data or Command word

CT2500 DEVICE I/O FUNCTION LISTING, Cont'd.

NAME	I/O	DESCRIPTION
ERR1, ERR2	O	**Error Bit One and Error Bit Two** ERR2 ERR1 0 0 No Error 0 1 Bit Error in Received Data/Command word or Control Frame 1 0 Parity Error in Received Data 1 1 Sync Error in Received Data/Command word or Control Frame
OVRFLOW	O	**Overflow Error** "1" = Overflow occurred in the Received Data Latch. Data not read in time.
RSTERR–	I	**Reset Error Flags Bar (Internal Pullup)** A low pulse on this line resets the ERR1, ERR2 and OVRFLOW error flags.
POR–	I	**Power on Reset Bar** A Master reset. A low pulse on this line resets the internal sequences and error flags. It does not reset the I/O Data latches.
WIOUT	I	**Word Identifier Bit Out** The value on this line is latched during STR2– for the WI bit position in the word to be transmitted. A "0" indicates a Data word and a "1" indicates a Command/Interrupt word.
WIIN	O	**Word Identifier Bit In** The WI bit of the received word is present on this line during RCVDTA– and indicates whether the word is a Data word or a Command/Interrupt word. The value is latched at the first RCVDTA– for an entire Burst Mode reception.
CMDOUT	I	**Command Out** Third bit of the transmitted Control Frame.
DTAOUT	I	**Data Out** Second bit of the transmitted Control Frame.
LDCNTRL–	I	**Load Control Frame Bar** This loads the status of CMDOUT, DTAOUT and BIT4OUT into the Control Frame to be transmitted. Transmission will commence when the loading is completed. This applies to both Sink and Source modes.
FIFOEN	I	**FIFO Enable** Source Mode: When FIFOEN is held high ("1"), FIFORD-'s (FIFO Read Bars) will be generated when the input data latch is empty (RDYFORDTA=1). During the FIFORD-, data presented to the parallel bus will be loaded into the input data latch and transmitted when ready. In a non-burst (single word) condition, FIFOEN must be removed before RDYFORDTA comes back. A positive pulse of 100 ns duration satisfies this requirement. Sink Mode: The parallel data bus goes active during RCVDTA- and will hold for approximately 25 ns after its rising edge. With a FIFO directly connected to the data bus, RCVDTA- can be used to load all received words into the FIFO. Gating RCVDTA- with WIIN selects only the data words for loading.
FIFORD-	O	**FIFO Read Bar** When the device is configured as a Source, this output pulses low during FIFOEN mode enabling data from a FIFO to be loaded into the input data latch for transmission.
RDYFORDTA	O	**Ready For Data** This signal is high when the input data latch is available for new data to be loaded in. When the data is loaded, RDYFORDTA goes low until the word is dumped into the output shift register.
ENV	O	**Envelope** This output envelopes the serial output data by being high during transmission.
TXDMXD	O	**Transmit Data / Manchester Data** Serial NRZ data out or Manchester Data out depending on the TXSELECT mode.

CT2500 DEVICE I/O FUNCTION LISTING, Cont'd.

NAME	I/O	DESCRIPTION
TXCMXD–	O	**Transmit Clock / Manchester Data Bar** Output shift clock or Manchester Data Bar depending on the TXSELECT mode.
G20MHZ	O	**Gated 20 Mhz** A gated 20 Mhz clock used in conjunction with Transmit Data, Transmit Clock and Envelope to generate Manchester data using other MCTC encoders.
TXSELECT	I	**Transmit Mode Select.** (Internal Pulldown) "1" = Serial output format is Manchester Data and Data Bar. "0" = Output will be NRZ Data and Shift Clock.
RXDATA	I	**Received Data** Received serial NRZ Data in.
RXCLOCK	I	**Received Clock** Received Shift Clock In.
TEST–	I	**Test Mode Bar** (Internal Pullup) A low on this pin puts the device into an internal wrap-around test mode. Transmit Data and Transmit Clock are internally connected to Received Data and Received Clock. The circuit must be in Source mode and only 32 bit data loads and reads are allowed. In this mode, STR2- loads the full 32 bits for transmission. When this word is wrapped back, RCVDTA- will pulse low indicating reception of a data or command word. STR1- enables the received data latch to be read out. Transmission of control frames can also be tested in this mode using the regular LDCNTRL- and RCVCNTRL signals.
BIT4IN	O	**Bit Four In** Fourth bit of received Type E control frame.
BIT4OUT	I	**Bit Four Out (Internal Pullup)** Fourth bit of Type E control frame to be transmitted.
SYNCIN	O	**Sync In** Sync position of the Received Data Latch.
CFRMSYNC	O	**Control Frame Sync In** Sync position of the Received Control Frame Latch
PRTYIN	O	**Parity In** Parity bit position of the Received Data Latch.

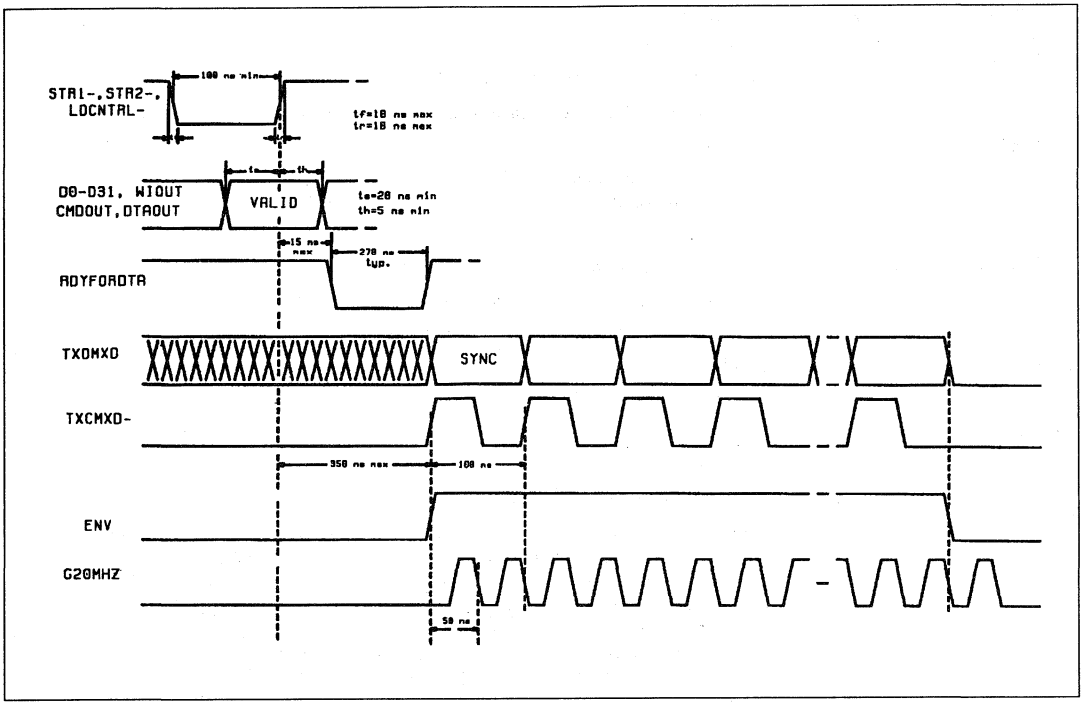


Figure 2: Transmit Timing Diagram - CT2500

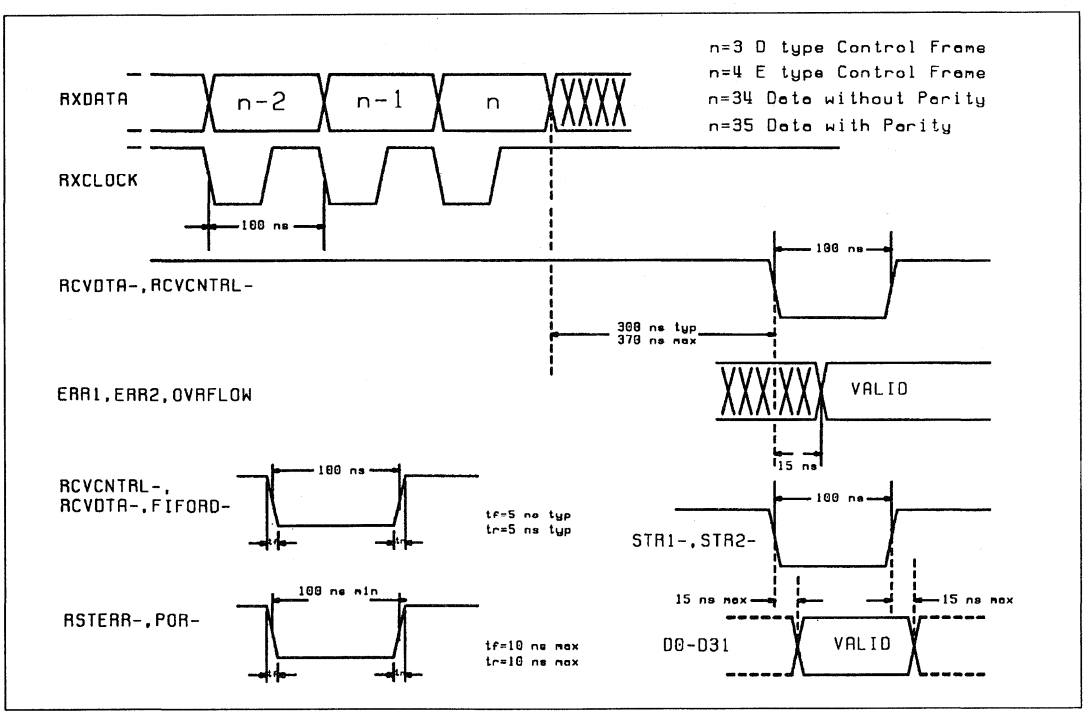


Figure 3: Receive Timing Diagram - CT2500

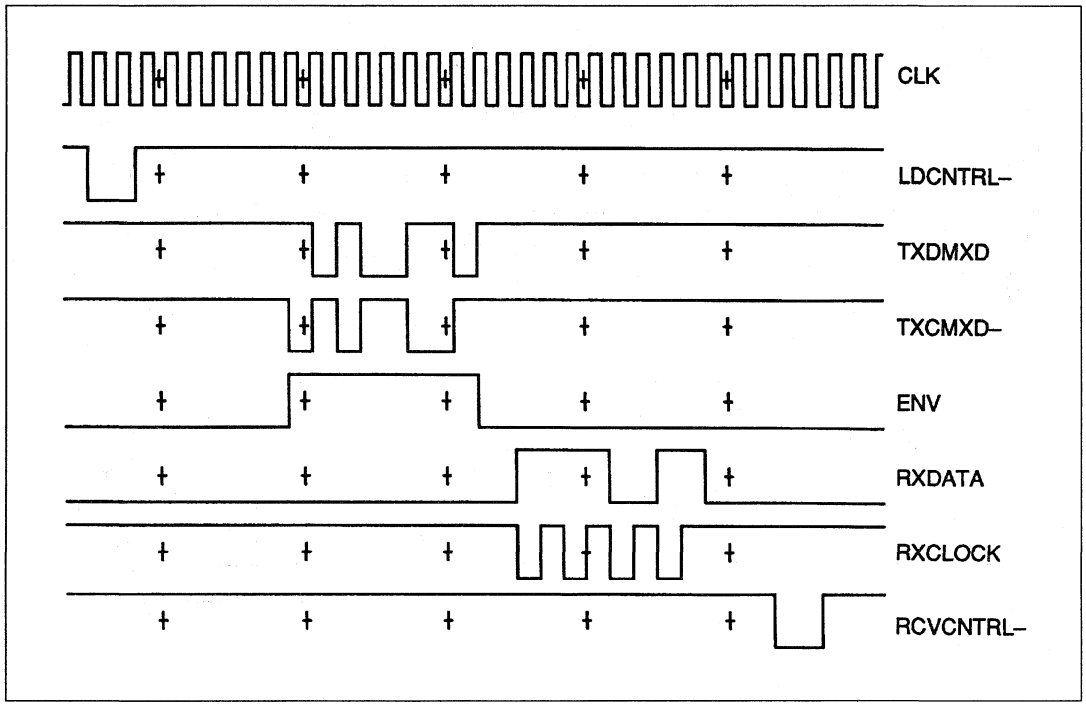


Figure 4: Control Frame Transfer Diagram - CT2500

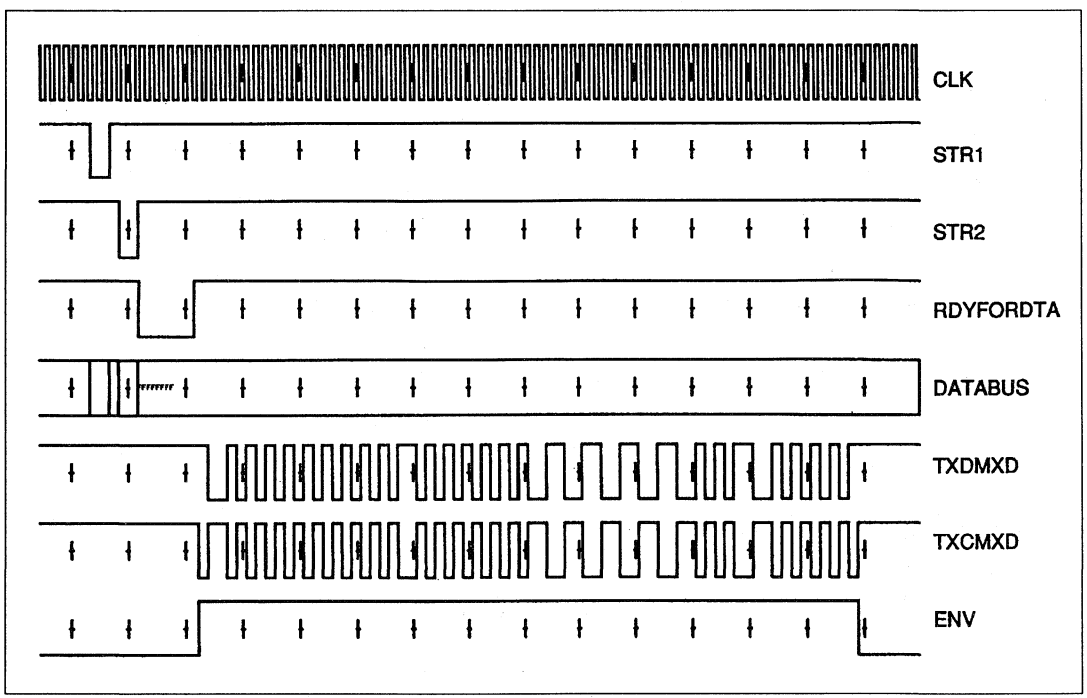


Figure 5: Source Data Frame Example Diagram - CT2500

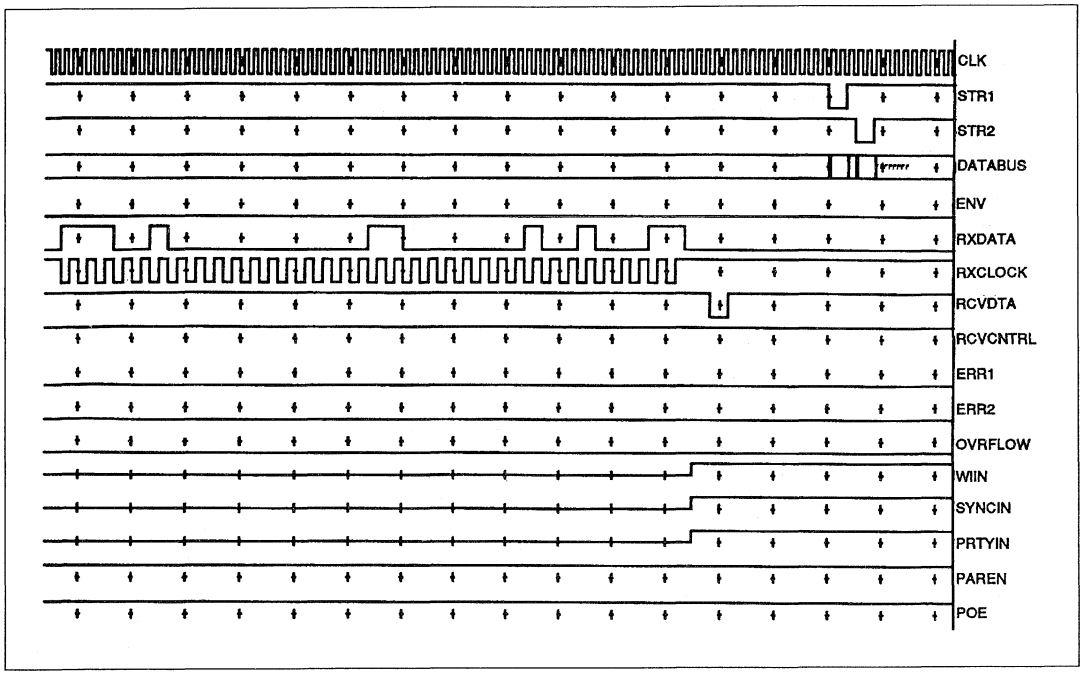


Figure 6: Sink Data Frame Example Diagram - CT2500

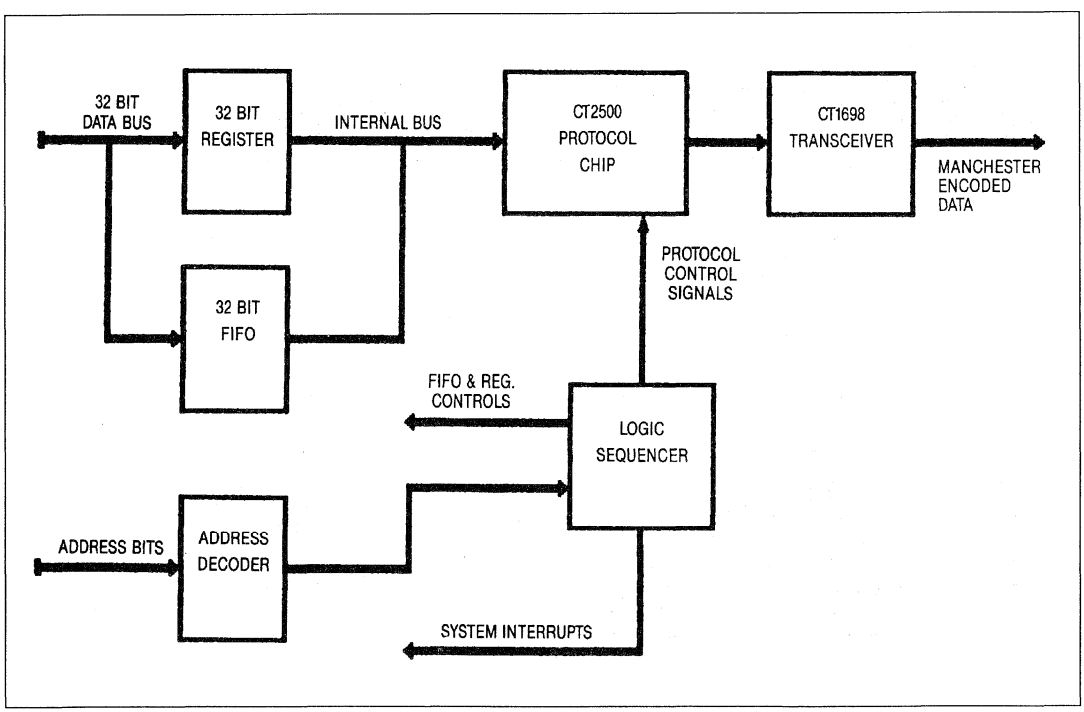
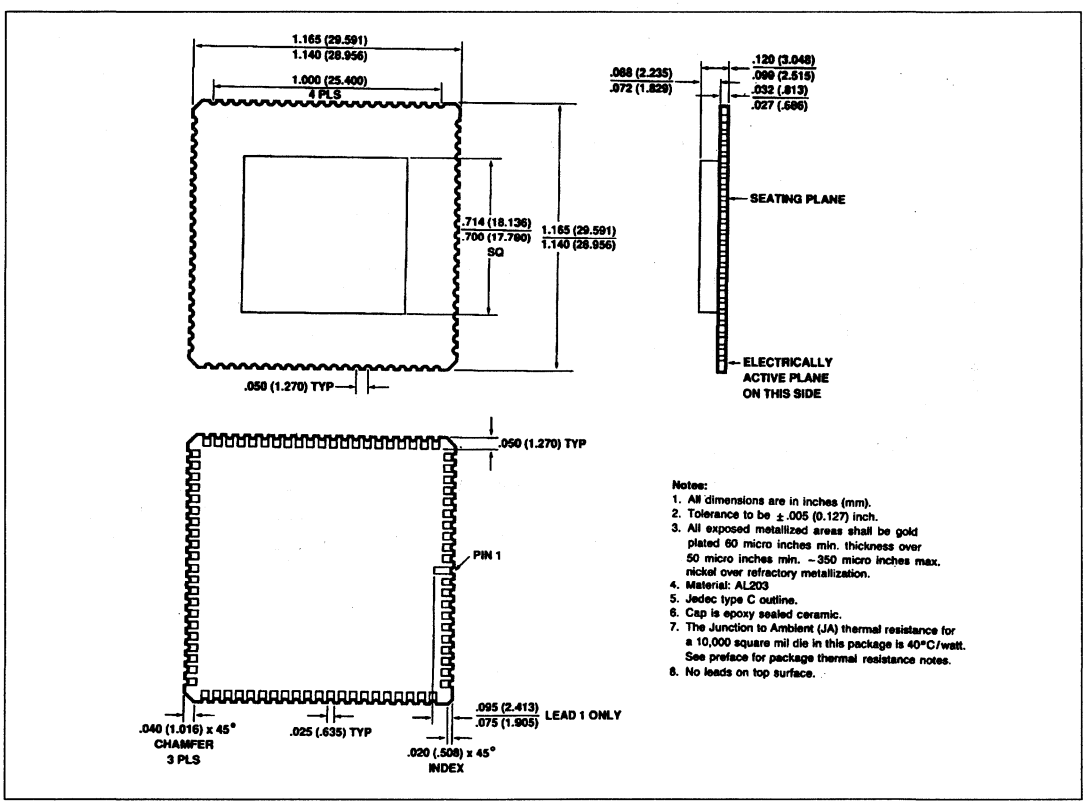


Figure 7: Typical I/O Board Configuration (Source and Sink Mode) - CT2500

CT2500-1 PINOUTS (84 LLCCC, JEDEC TYPE C)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	22	VDD [+5 VOLTS]	43	GND	64	VDD [+5 VOLTS]
2	D8	23	TXSELECT	44	SYNCIN	65	VDD [+5 VOLTS]
3	D7	24	OVRFLOW	45	RXCLOCK	66	D23
4	D6	25	REVCNTRL–	46	RXDATA	67	D22
5	D5	26	RCVDTA–	47	SO/SI–	68	D21
6	D4	27	RCYFORDTA	48	STR1–	69	D20
7	D3	28	TXCMXD	49	STR2–	70	D19
8	D2	29	TXDMXD	50	TEST–	71	D18
9	D1	30	WIIN	51	WIOUT	72	D17
10	PRTYIN	31	G20MHZ	52	D31	73	D16
11	VDD [+5 VOLTS]	32	GND	53	CFRMSYNC	74	GND
12	VDD [+5 VOLTS]	33	BURST	54	VDD [+5 VOLTS]	75	GND
13	D/E–	34	CLK	55	PAREN	76	POE
14	DO	35	CMDOUT	56	D30	77	D15
15	CMDIN	36	DTAOUT	57	D29	78	D14
16	DTAIN	37	BIT4OUT	58	D28	79	D13
17	ENV	38	RSTERR–	59	D27	80	D12
18	ERR1	39	FIFOEN	60	D26	81	D11
19	ERR2	40	LDCNTRL–	61	D25	82	D10
20	FIFORD–	41	POR–	62	D24	83	D9
21	VDD [+5 VOLTS]	42	GND	63	BIT4IN	84	GND

CT2500-1 84-LEAD LEADLESS CERAMIC CHIP CARRIER, JEDEC TYPE C, MECHANICAL OUTLINE



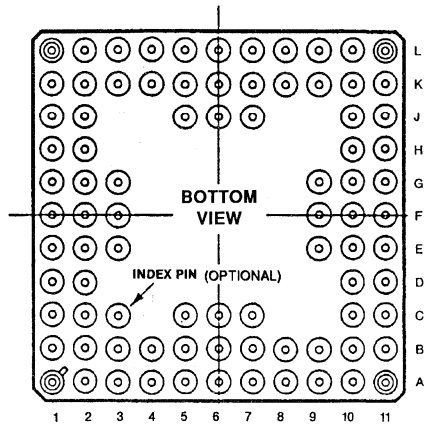
CT2500 PINOUTS (84 PGA)

PIN	SIGNAL	PIN	SIGNAL
B2	BURST	K10	GND
C2	CLK	J10	POE
B1	CMDOUT	K11	D15
C1	DTAOUT	J11	D14
D2	BIT4OUT	H10	D13
D1	RSTERR–	H11	D12
E3	FIFOEN	F10	D11
E2	LDCNTRL–	G10	D10
E1	POR–	G11	D9
F2	GND	G9	GND
F3	GND	F9	GND
G3	SYNCIN	F11	D8
G1	RXCLOCK	E11	D7
G2	RXDATA	E10	D6
F1	SO/SI–	E9	D5
H1	STR1–	D11	D4
H2	STR2–	D10	D3
J1	TEST–	C11	D2
K1	WIOUT	B11	D1
J2	D31	C10	PRTYIN
L1	CFRMSYNC	A11	VDD [+5 VOLTS]
K2	VDD [+5 VOLTS]	B10	VDD [+5 VOLTS]
K3	PAREN	B9	D/E–
L2	D30	A10	D0
L3	D29	A9	CMDIN
K4	D28	B8	DTAIN
L4	D27	A8	ENV
J5	D26	B6	ERR1
K5	D25	B7	ERR2
L5	D24	A7	FIFORD–
K6	BIT4IN	C7	VDD [+5 VOLTS]
J6	VDD [+5 VOLTS]	C6	VDD [+5 VOLTS]
J7	VDD [+5 VOLTS]	A6	TXSELECT
L7	D23	A5	OVRFLOW
K7	D22	B5	RCVCNTRL–
L6	D21	C5	RCVDTA–
L8	D20	A4	RDYFORDTA
K8	D19	B4	TXCMXD–
L9	D18	A3	TXDMXD
L10	D17	A2	WIIN
K9	D16	B3	G20MHZ
L11	GND	A1	GND

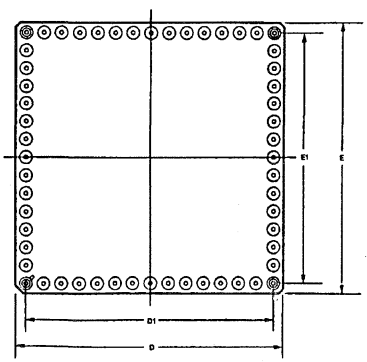
CT2500

PACKAGE INFORMATION

84-PIN CERAMIC PIN GRID ARRAY

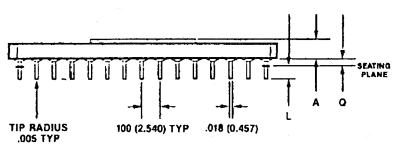


CT2500 84-PIN CERAMIC PIN GRID ARRAY, MECHANICAL OUTLINE



PACKAGE INFORMATION

CERAMIC PIN GRID ARRAY PACKAGE OUTLINE



Dimensions in Inches (Millimeters)

CERAMIC PIN GRID ARRAY

Pin Count	Matrix	Cavity Position	A		D (E)		D1 (E1)		Q	L
			Min	Max	Min	Max	Min	Max	Ref	Ref
84	11 x 11	Up	.0800 (2.032)	.1000 (2.540)	1.080 (27.43)	1.120 (28.45)	0.980 (25.15)	1.010 (25.65)	0.050 (1.270)	0.130 (3.302)

Section 9

Mil-Std-1773
Fibre Optic Products

3087-1.2 September 1991

CT1763

1MHZ FIBRE OPTIC RECEIVER FOR MIL-STD-1773

FEATURES

- Tuned for 1MHz operation
- Compatible with existing MIL-STD-1553/1773 protocols
- Small size, hermetically sealed metal package
- 820nm wavelength
- SMA connectors for easy serviceability
- Compatible with CT1750 optical outputs
- Compatible with all GPS MIL-STD-1553 protocol units

GENERAL DESCRIPTION

The CT1763 Receiver is designed to convert an optical input stream to TTL digital data and operates with data rates of up to 1Mb/sec Manchester. Differential and adaptive circuits are utilized for gain control under burst type transmissions which are common to multi-terminal bus configurations. The Receiver automatically synchronizes to the first data bit and does not require preamble bits to bias the unit. This feature allows the user to implement a MIL-STD-1773 fiber optic channel with no modifications to the existing protocol circuitry.

GPS (Farmingdale) is a MIL-STD-1772 Certified manufacturer.

APPLICATIONS INFORMATION

The CT1763 is ideally suited to implement a MIL-STD-1773 fiber optic channel. It is tuned specifically for 1MHz operation. Its TTL outputs can be readily reconstructed to the Manchester waveform requirement for all existing protocol chips, thus allowing for convenient compatibility with MIL-STD-1553 protocol applications. See Figure 3. A complete dual-redundant 1773 Bus Controller/Remote Terminal would consist of two CT1763 Receivers, two CT1750 Transmitters, and one CT2529 Protocol/Interface hybrid. See Figure 4.

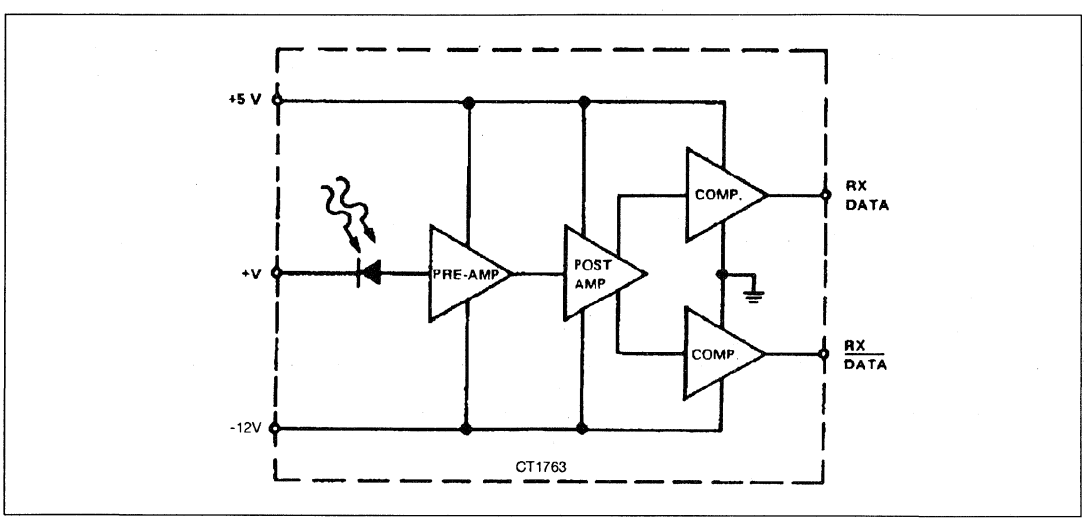


Figure 1: Functional Diagram - CT1763

ELECTRICAL CHARACTERISTICS

POWER REQUIREMENTS

DC Voltage	Tolerance	Power (mA)	
		Typical	Max @ 100%
+5V	±10%	38	45
−12V	±10%	32	45

DRIVE LIMITS

	Voltage	Current	
Data and $\overline{\text{Data}}$	V_{OH}=2.4V	I_{OH}>−80 µA	C_L=15pF
	V_{OL}=0.4V	I_{OL}>4mA	C_L=15pF

TRANSMITTER SPECIFICATIONS (SEE FIGURE 2)

Symbol	Parameter/Conditions	Min	Max	Unit
	Input Signals			
RP_0	Peak Optical Input Power (See Note)	1	150	µW
T	Input Pulse Period	930	1070	ns
T/2	Half Pulse Period	430	570	ns
T_r	Input Optical Rise Time		200	ns
T_f	Input Optical Fall Time		200	ns
	Output Signals			
T_0	DATA or $\overline{\text{DATA}}$ Pulse Width Output	200		ns

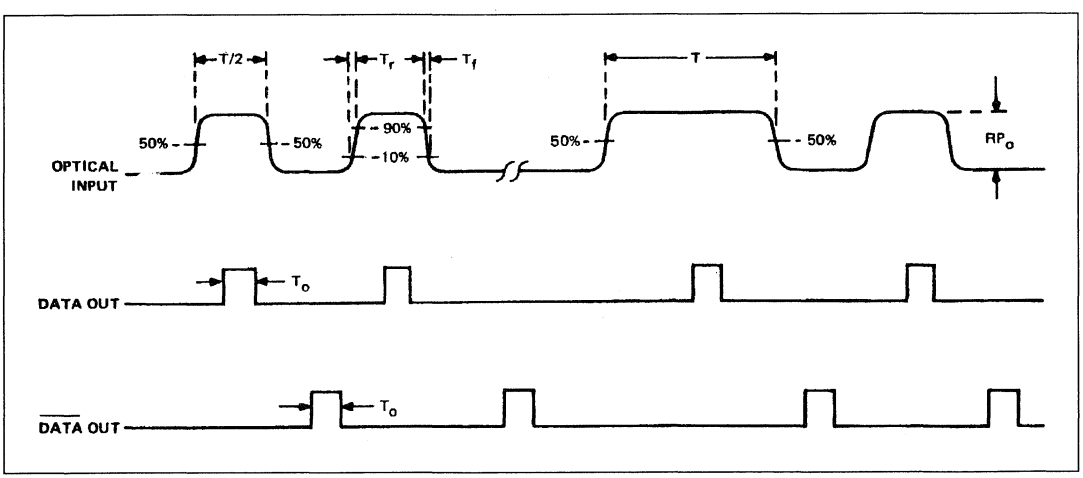


Figure 2: CT1763 Receiver Waveforms

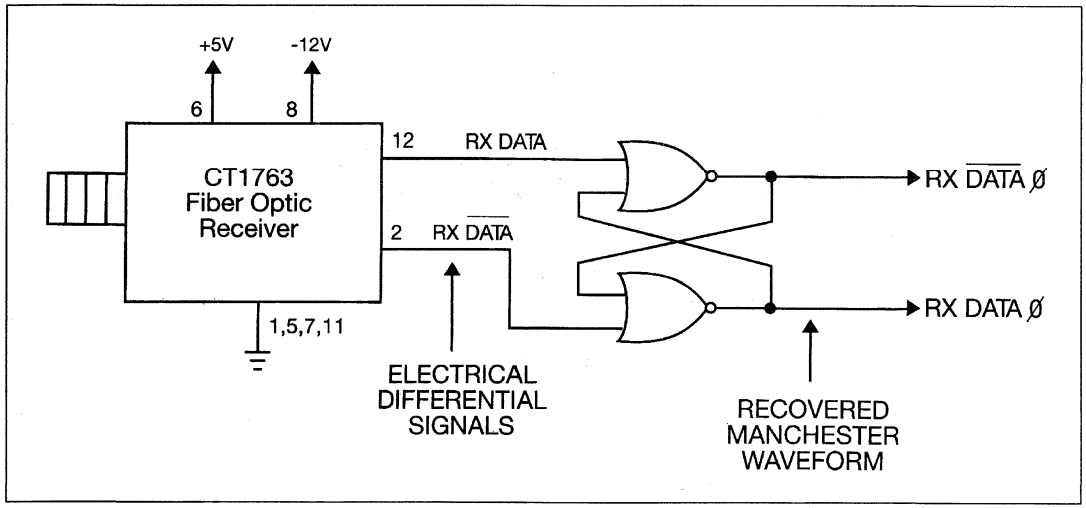


Figure 3: CT1763 Manchester Waveform Recovery

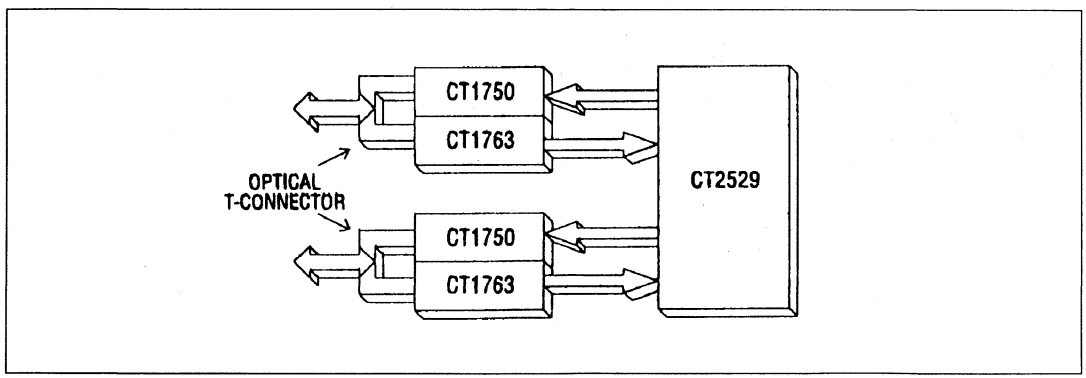


Figure 4: A 1773 Terminal Configuaration

PIN ASSIGNMENTS

1 – GND	5 – CASE GND	9 – DATA A FTP*
2 – $\overline{\text{DATA}}$ OUT	6 – +5V	10 – DATA B FTP*
3 – $\overline{\text{DATA}}$ B FTP*	7 – GND	11 – GND
4 – $\overline{\text{DATA}}$ A FTP*	8 – –12V	12 – DATA OUT

*FTP – Factory Test Point

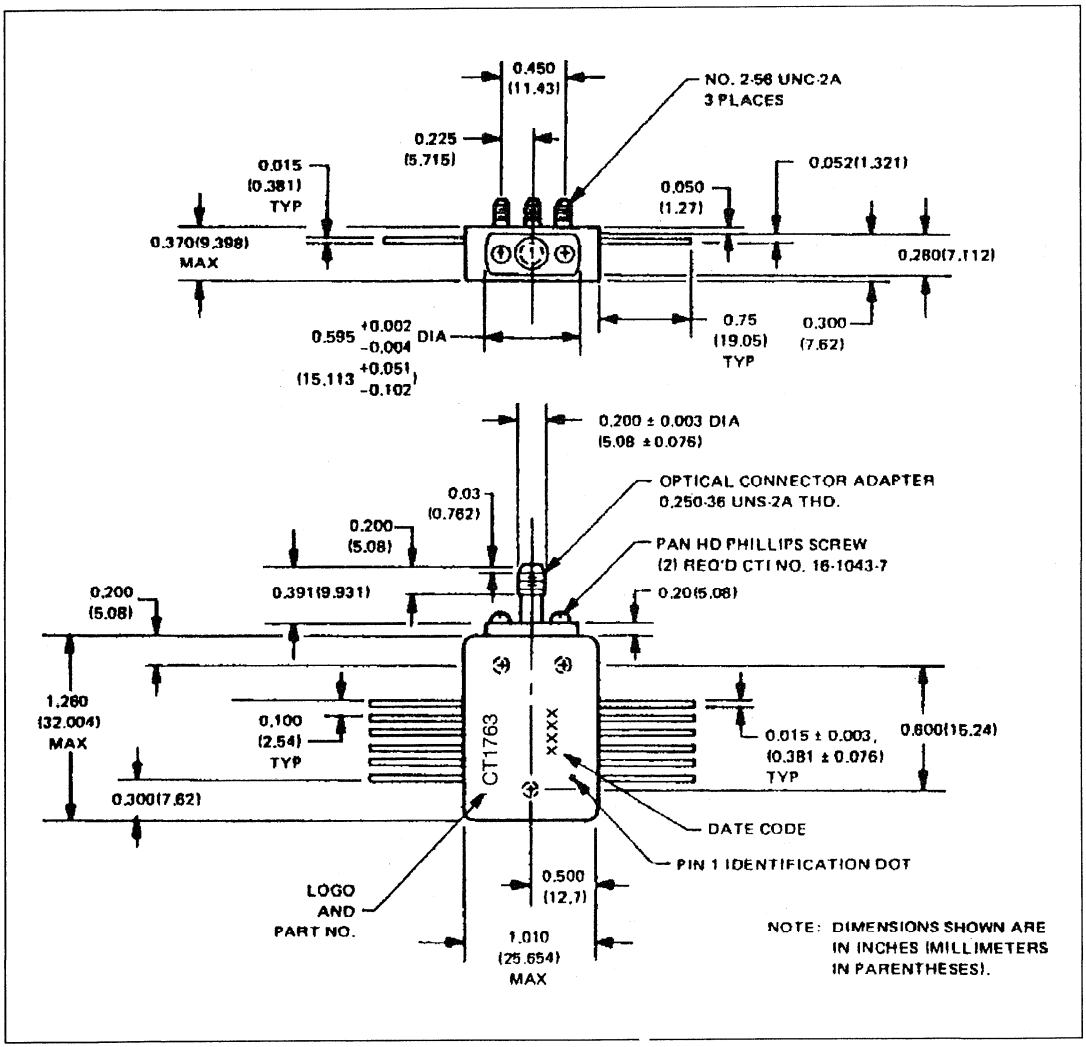


Figure 5: Package Outline - CT1763

Section 10
Locations

HEADQUARTERS OPERATIONS

UNITED KINGDOM — Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom.
Tel: (0793) 518000 Tx: 449637 Fax: 0793 518411

NORTH AMERICA — Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA.
Tel:(408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES

FRANCE & BENELUX — Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France.
Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07 Tx: 602 858 F

GERMANY, AUSTRIA and SWITZERLAND — Ungererstraße 129, 8000 Munchen 40, Germany.
Tel: 089/36 0906-0. Fax: 089/360906-55 Tx: 523980

ITALY — Viale Certosa, 49 20149 Milano. Tel: (02) 33 00 10 44/45. Fax: (GR3) 31 69 04. Tx: 331347

JAPAN — Nichiyo Building 6F, 11-12, Kanda - Mitoshirocho, Chiyoda-ku, Tokyo 101.
Tel: (03) 3296-0281. Fax: (03) 3296-0228

NORTH AMERICA — **Integrated Circuits**
Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA.
Tel: (408) 438 2900 ITT Tx: 4940840 Fax: (408) 438 7023
SOS, Microwave and Hybrid Products
160 Smith Street. Farmingdale, NY11735, USA. Tel: (516) 293 8686 Fax: (516) 293 0061.

SOUTH EAST ASIA — 152 Beach Road, #04-05 Gateway East, Singapore 0718.
Tel: 2919291. Fax: 2916455

SWEDEN — Ostmästargränd 4, GS-12173 Johanneshov. Tel: 46 8 7228690 Fax: 46 8 7227879

UNITED KINGDOM and SCANDINAVIA — Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts SN2 5AY, U.K.
Tel: (0793) 518510. Tx: 444410 Fax: (0793) 518582.

WORLD-WIDE AGENTS

AUSTRALIA and NEW ZEALAND — **GEC George Brown Electronics,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia.
Tel: 612 638 1888. Fax: 612 638 1798.

EASTERN EUROPE — **CTL Empexion Ltd..** Falcon House, 19 Deer Park Road, London SW19 3WX, U.K.
Tel: (081) 543 0911. Tx: 928472. Fax: (081) 540 0034.
FA Bernhart GmbH, Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany. Tel: 80 41 41 676
Fax: 80 41 71 504 Tx: 526246 FABD.

HONG KONG — **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kolk Street,Tsuen Wan,
N.T. Hong Kong. Tel: 4144241-6. Tx: 36590. Fax: 4136078.

INDIA — **Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 India
Tel: 11 3312110 Fax: 11 3712155.

JAPAN — **Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku. Tokyo 103.
Tel: 3 272 5771. Tx: 24874. Fax: 3 271 1479.
Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550.
Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850.
Microtek Inc., Itoh Bldg, 7-9-17 Nishishinijuku. Tokyo 160. Tel: 3 371 1811. Tx: 27466. Fax: 3 369 5623.

KOREA — **KML Corporation,** 3rd Floor, Bang Bae Station Building, 981-15 Bang Bae, 3-Dong Shucho-Gu, Seoul, Korea,
CPO Box 7981. Tel: 2 588 2011/6. Tx: K25981. Fax: 2 588 2017.

MALAYSIA — **Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens, 88 Jalan Raya Chulan, 50200 Kualar Lumpur,
Malaysia. Tel: 2423522. Fax: 2423264.

SCANDINAVIA: Denmark — **Scansupply A/S,** 18 Nannasgade, DK-2200 Copenhagen N. Tel: 31 83 50 90. Tx: 19037. Fax: 31 83 25 40.
Scansupply A/S, Marselisborg Havnevej 36, 8000 Arhus C. Tel: 45 86 12 77 88. Fax: 45 86 12 77 18.

Finland — **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 98 0550 002. Tx: 122214. Fax: 98 0551 117.

Norway — **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50. Tx: 71963 Fax: 2 643443.

TAIWAN — **King and King's Technology Ltd.,** 4, Alley 6, Lane 118, Sec 2, Ho Ping East Road, Taipei 106, Taiwan.
Tel: (886-2) 732-6170. Fax: (886-2) 738-9146.

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ICC:
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Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40. Tx: 571224 F.
Bretagne-9, Rue du Général Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311 F.
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Est-27, Rue Kleber, 68000 Colmar. Tel: 89 41 15 43. Tx: 870569 F.
Midi-Pyrénées, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38. Tx: 530957 F.
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Provence/Cote d'Azur, Avenue Donadei, Bat.B-06700 Staint. Laurent-du-Var. Tel: 93 07 77 67. Tx: 461481 F.
Rhône-Alpes, 101, Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29. Tx: 305301 F.
Aquitech:
Aquitech, 73 Avenue du Château d'Eau 33700 Merignac. Tel: 56 55 10 30. Tx: 550529. Fax: 56 47 53 20.
Aquitech, 25 Rue de la Chalotais 35000 Rennes. Tel: 99 78 31 32. Fax: 99 79 21 80.
Aquitech, 2 Rue Alexis de Toqueville 92189 Antony. Tel: (1) 40 96 94 94. Tx: 550529. Fax: (1) 40 96 93 00.
Rhonalco, 3 Rue Berthelot, 69627 Villeurbanne. Tel: 33 78 53 00 25. Tlx: 380284. Fax: 33 72 34 67 72.

GERMANY
AS Electronic Vertriebs GmbH, In den Garten 2, 6380 Bad Homburg 6. Tel: 06172 458931. Fax: 06172 42000.
Astronic GmbH, Gruenwalderweg 30, 8024 Deisenhofen. Tel: 089 6130303. Tx: 5216187. Fax: 089 6131668.
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Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47. Tx: 822538. Fax: 0231 57 75 14.

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ITALY
Adelsi Spa, Via Novara 570, 20153 Milan. Tel: 2 3580641. Tlx: 332423. Fax: 2 3011988.
Alpha Microonde SNC, Via Aselli 11, 20133 Milano. Tel: 06 66 35 273 Fax: 06 66 35 268.
Con Systems SRL, Via Gramsci 156, 20037 Padereno Dugnano, Milano. Tel: 02 99 04 19 77 Fax: 02 99 04 1981.
(Also: Viale Egeo 24, 00144 Roma)
Eurelettronica SpA, Via E. Fermi 8, 20090 Assago Milan. Tel: 2 4880022. Tlx: 350037. Fax: 2 4880275.
Fanton SRL., Milano-Bologna. Firenze, Roma, Padova. Torino. Tel: 2 3287312. Tlx: 350853. Fax: 2 3287948.

JAPAN
Nissho Iwai Aerospace Corp., 5-3 Akasaka & Chome, Minato-Ku, Tokyo-107. Tel: 3 588 2111 Fax: 3 588 4787.
Yamada Corporation, PO Box Tokyo Akasaka No. 120, Tokyo. Tel: 3 475 1121 Fax: 3 479 1789.

NETHERLANDS
Heynen B.V., Postbus 10, 6590 AA Gennep. Tel: 8851-96111 Tx: 37282 Fax: 8851 96200.
Tekelek Airtronic BV., PO Box 63, NL 2712 LB Zoetermeer, Netherlands. Tel:79 310100 Fax:79 417504

PORTUGAL
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SPAIN
Anatronic SA, Avda de Valladolid 27, 28008 Madrid. Tel: 91 542 4455/6. Fax: 91 2486975.
Anatronic SA, Bailen, 176, Estresuelo 1°, 08037 Barcelona. Tel: 93 258 1906/7. Fax: 93 258 7128.
Master Electronica SA, Angel Muñoz 18 Bis, 28043 Madrid. Tel: 91 5194342 Tx: 49085 Fax: 91 5193163.

SWEDEN
Pronesto AB, Hemsvärnsgatan 15, Box 1358, S-17126 Solna. Tel: (08) 733 9300 Fax: (08) 764 5009.

SWITZERLAND
Basix für Electronik AG, Hardturmstr 181, CH-8010 Zurich. Tel: 01 2761111 Tx: 822966 Fax: 01 2761199
Elbatex AG., Hardstr 72, CH-5430 Wettingen. Tel: 41 56 27 51 11. Tx: 826300. Fax: 41 56 27 19 24.

TAIWAN
King and King's Technology Ltd., 4, Alley 6, Lane 118, Sec 2, Ho Ping East Road, Taipei 106, Taiwan.
Tel: (886-2) 732-6170. Fax: (886-2) 738-9146.

TURKEY
Empa, Refik Saydam Cad No.89 Kat 5, 80050 Sishane, Istanbul. Turkey. Tel: 0 143 621213. Fax: 0 143 6549.

UNITED KINGDOM
Celdis Ltd., 37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171. Tx: 848370. Fax: 0734 509933.
Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU.
Tel: 0532 790101. Tx: 55147. Fax: 0532 633404.
Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY.
Tel: 0734 788878, 787848. Tx: 847571. Fax: 0734 776095.
Gothic Crellon Ltd., P.O.Box 301, Elizabeth House, 22 Suffolk Street, Queensway, Birmingham B1 1LZ.
Tel: 021 643 6365. Tx: 338731. Fax: 021 633 3207.
Macro, Burnham Lane, Slough SL1 6LN. Tel: 0628 604383. Fax: 0628 66873.
Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street Yiewsley, West Drayton, Middlesex UB7 7XB
Tel: (0895) 445522. Tx: 21958. Fax: (0895) 422044.
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Tel: 0279 626777. Tlx: 818801. Fax: 0279 441687.
2001 Electronic Components Ltd, Woolners Way, Stevenage, Herts SG1 3AJ.
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Tel: (0438) 312393. Tx: 825637. Fax: (0438) 318711.

UK EXPORT

(To countries other than those listed)
GEC Plessey Semiconductors , Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts, UK SN2 5AY. Tel: (0793) 518510. Tx: 444410. Fax: (0793) 518582.
Whiteaway Laidlaw (Overseas) Ltd., PO Box 93, Ambassador House, Devonshire Street North, Manchester M60 6BU Tel: 061 273 3228 Fax: 061 274 3757

AMERICAN DESIGN CENTRES

CANADA
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COLORADO
Analog Solutions, 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.

ILLINOIS
Frederikssen & Shu Laboratories, Inc., 531 West Golf Rd., Arlington Heights, IL 60005. Tel: (312) 956-0710.

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DIXIE	41 Milton Ave. #104, Alpharetta, GA 30201. Tel: (404) 343-9904. Fax: (404) 343-9972.
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NORTH AMERICAN REPRESENTATIVES

ALABAMA	**Electramark, Inc.,** 4950 Corporate Drive, Huntsville, AL 35805 Tel: (205) 830-4400 Fax: (205) 830-4406
ARIZONA	**Fred Board Associates,** 7353 E, 6th Avenue, Scottsdale, AZ 85251 Tel: (602) 994-9388. Fax: (602) 994-9477
CALIFORNIA	**Select Electronics,** 14730 Beach Blvd. Bldg., F #106, La Mirada, CA 90638. Tel: (714) 739-8891 Fax: (714) 739-1604
	Select Electronics, 2106 Waterby, Westlake Village, CA 91361. Tel: (805) 496-8877
	Select Electronics,2109 Brookfield Drive, Thousand Oaks, CA 91362. Tel: (805) 492-2007
FLORIDA	**DHR Marketing, Inc.,** 2300 W.Sample Road, Suite 307, Pompano, FL 33073.Tel: (305) 972-9157 Fax: (305) 972-9164
	DHR Marketing, Inc., 417 Whooping Loop, Suite 1747, Altamonte Springs. FL 32701.
	Tel: (407) 331-1199. Fax: (407) 331-1263.
	DHR Marketing, Inc., 2907 State Road 590, STE. 11,Clearwater, FL 34619.
	Tel: (813) 725-5262/725-5347Fax: (813) 725-1724
GEORGIA	**Electramark, Inc.,** 6030-H Unity Drive, Norcross, GA 30071. Tel: (404) 446-7915 Fax: (404) 263 6389
ILLINOIS	**Micro Sales, Inc.,** 901 West Hawthorn Drive, Itasca, IL 60043. Tel: (708) 285-1000 Fax: (708) 285-1008
INDIANA	**Leslie M. DeVoe,** 4371 E. 82nd St., Suite D, IN 46250. Tel: (317) 842-3245. Fax: (317) 845-8440
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666. Fax: 319-377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8645 College Blvd., Suite 220, Overland Park, KS 66210.
	Tel: (913) 469-1312. Fax: (913) 469-1238.
	Lorenz Sales, Inc., 1530 Maybelle, Wichita, KS 67212. Tel: (316) 721-0500. Fax: (316) 721-0566.
MARYLAND	**Walker Associates,** 1757 Gable Hammer Road, Westminster, MD 21157.
	Tel: (301) 876-9399 Fax: (301) 876-9285.
	Walker Associates, 16904 Queen Anne Bridge Road, Mitchellville, MD 20716.
	Tel: (301) 249-7145 Fax: (301) 249-7145
MASSACHUSETTS	**Stone Components,** 2 Pierce Street. Framingham, MA 01701. Tel: (508) 875-3266. Fax: (508) 875-0537.
	Stone Components, 10 Atwood Street, Newburyport, MA 01950. Tel: (508) 875-3266. Fax: (508) 465-3544.
	Stone Components, 11 Blueberry Hill Rd., Longmeadow, MA 01106. Tel: (413) 567-9075. Fax: (413) 567-1019.
	Stone Components, P.O.Box 379, Canton, MA. Tel: (617) 828-6569 Fax: (617) 828-6734
MICHIGAN	**Greiner Associates Inc.,** 15325 E. Jefferson Avenue, Grosse Point Park, MI 48230.
	Tel: (313) 499-0188. Fax: (313) 499-0665.
MINNESOTA	**High Technology Sales,** 11415 Valley View Road, Eden Prairie, MN 55344. Tel: (612) 944--7274
	Fax: (612) 944--3229.
MISSOURI	**Lorenz Sales, Inc.,** 10176 Corporate Square Dr., Suite120, St. Louis, MO 63132.
	Tel: (314) 997-4558. Fax: (314) 997-5829.
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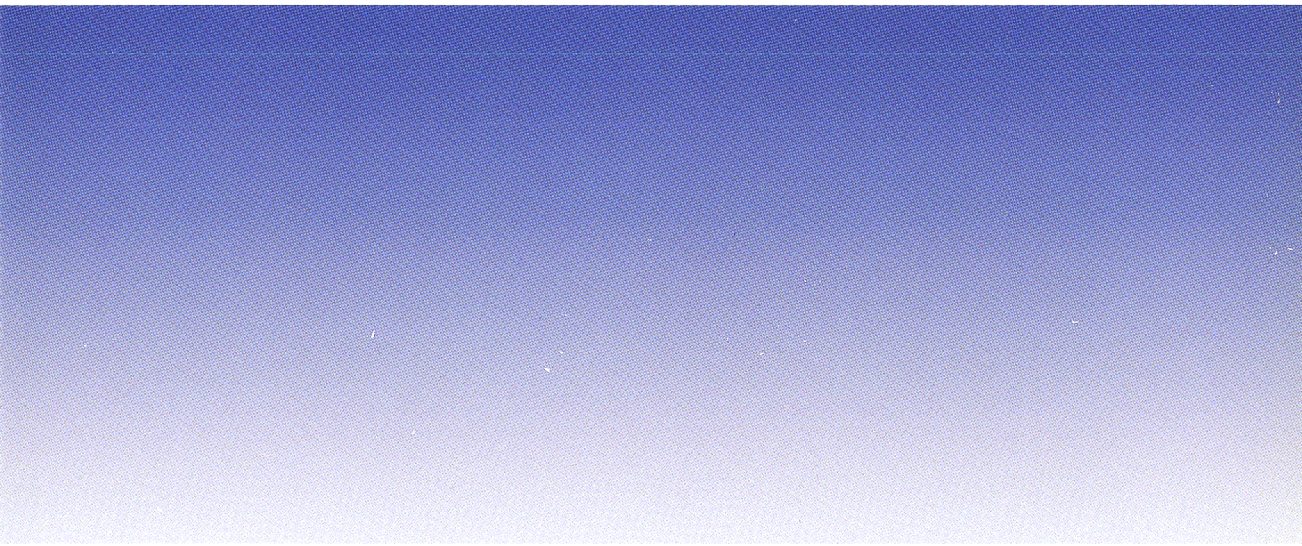

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